# SG500

## Low Jitter Spectrum Clock Generator for Power PC Designs

## Product Features

- Supports Power PC CPU's
- Supports simultaneous PCI and Fast PCI Buses.
- Uses external buffer to reduce EMI and Jitter
- PCI synchronous clock
- Fast PCI synchronous clock
- Separated 3.3 volt power supplies for reduced Jitter
- <500 pS skew between CPU and PCI clocks
- Programmable features:
    - Frequency selection
    - Margin testing frequency increases
    - Output enable for board level testing
    - CPU to PCI clock offset selection
- Independent VDD supplies for all output clocks
- 28 pin SOP 209 mil package
- Spread Spectrum Technology for EMI reduction
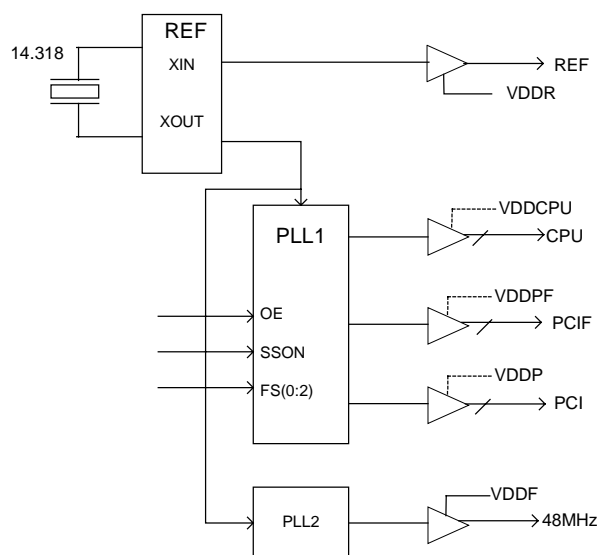- Internal Crystal Load Capacitors for 20pF parallel resonant crystal support.

## Frequency Table

| FS2 | FS1 | FS0 | CPU | PCI | PCIF |
|-----|-----|-----|-----|-----|------|
| 0 | 0 | 0 | 90 | 30.0 | 60.0 |
| 0 | 0 | 1 | 94.5(90+5%) | 31.5 | 63 |
| 0 | 1 | 0 | 66.6* | 33.3* | 66.6* |
| 0 | 1 | 1 | 70(66+5%)* | 35** | 70** |
| 1 | 0 | 0 | 100.0(99.6)* | 33.3* | 66.6* |
| 1 | 0 | 1 | 105.0** | 35.0** | 69.9** |
| 1 | 1 | 0 | 120.0(119.9) | 30.0 | 60.0 |
| 1 | 1 | 1 | 133.0** | 33.3** | 66.6** |

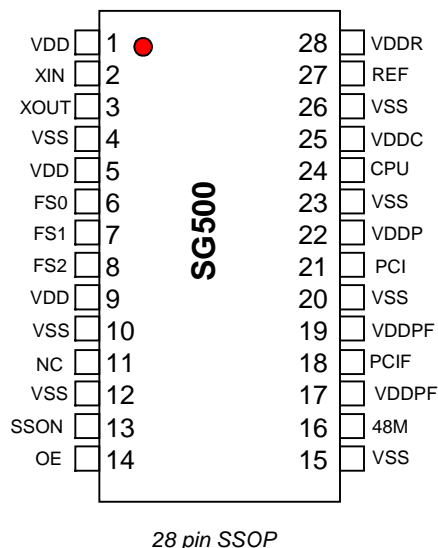\* Indicates 0.5% down spread spectrum capable

\*\* See Test Mode table for functional definition when SSON is low.

**(TEST MODE FUNCTIONALITY NOT GUARANTEED OVER FULL TEMPERATURE AND VOLTAGE)**

## Block Diagram



## Pin Configuration



*28 pin SSOP*

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## Pin Description

| Pin Number | Pin Name | PWR | I/O | Description |
|---|---|---|---|---|
| 2 | XIN | VDD | I | These pins form an on-chip reference oscillator when connected to terminals o an external parallel resonant crystal (nominally 14.318 MHz). XIN may also serve as input for an externally generated reference signal. If the external input is used, Pin 3 is left unconnected. |
| 3 | XOUT | VDD | O | |
| 18 | PCIF | VDDP | O | 66.6 Mhz FAST PCI clock rising edge synchronized to the CPU Clock |
| 21 | PCI | VDDP | O | 33.3 MHz PCI clock rising edge synchronized to the CPU clock. |
| 17 | VDDF | - | PWR | Power for 48 Mhz fixed clock buffer |
| 19 | VDDPF | - | PWR | Power for Fast PCI (66Mhz) clock buffer and PCIF (66 Mhz) clock buffer |
| 22 | VDDP | - | PWR | Power for PCI (33 Mhz) clock buffer and PCIF ( 66 Mhz) clock buffer |
| 24 | CPU | VDDC | O | CPU clock output. See table on page 1 for frequencies. |
| 13 | SSON | VDD | I PU | Spread Spectrum clock modulation pin. Enables Spread Spectrum EMI reduction when at logic low (0) level. Has an internal pull-up resistor. |
| 16 | 48M | VDDF | O | This pin is a fixed frequency 48 Mhz clock output. |
| 14 | OE | VDD | I | Output enable. When at logic level low causes all clock outputs to be in a Tri-State mode. Has internal pull-up resistor. |
| 27 | REF | VDD | O | This pin is a buffered output copy of the crystal reference frequency. |
| 6,7,8 | FS(0:2) | VDDPU | I | Frequency selection input pins. See table on page 1 for functionality. Contain internal pull-up resistors. |
| 4,10,12,15,20,23,26 | VSS | - | PWR | Ground pins for the chip. |
| 1,5,9 | VDD | - | PWR | Power supply pins for analog circuit and core logic. |
| 25 | VDDC | - | PWR | Power supply for CPU clock output buffer. |
| 28 | VDDR | - | PWR | Power supply for reference clock output buffer. |

*A bypass capacitor (0.1μF) should be placed as close as possible to each VDD pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance's of the traces.*

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## Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this product, the modulation is 1.0% down from the resting frequency.

### Down Spread
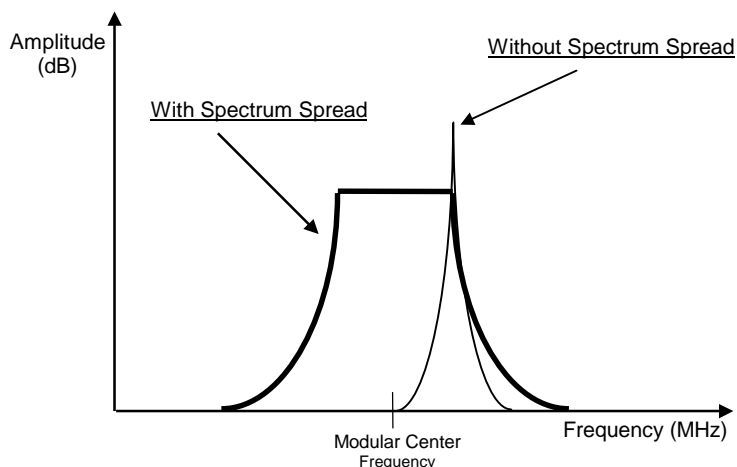


## Test Mode Control Table

| SSON | FS2 | FS1 | FS0 | CPU | PCI | PCIF | 48M | REF |
|------|-----|-----|-----|-----|-----|------|-----|-----|
| 0 | 0 | 0 | 0 | 90.0 | 30.0 | 60.0 | 48 | 14.318 |
| 0 | 0 | 0 | 1 | 94.5 | 31.5 | 63 | 48 | 14.318 |
| 0 | 0 | 1 | 0 | 66.6 | 33.3 | 66.6 | 48 | 140318 |
| 0 | 0 | 1 | 1 | Tri State | Tri State | Tri State | Tri State | Tri State |
| 0 | 1 | 0 | 0 | 100SS | 33.3 SS | 66.6 SS | 49 | 14.318 |
| 0 | 1 | 0 | 1 | T2* | T2* | T2* | T2* | T2* |
| 0 | 1 | 1 | 0 | 120 | 30 | 60 | 48 | 14.318 |
| 0 | 1 | 1 | 1 | XIN/2 | XIN/6 | XIN/3 | XIN | XIN |

Note: (All frequencies are in Mhz, XIN defines the clock applied to the XIN pin for testing purposes, and SS= Spread Spectrum_. T2 is a device test mode and is not intended for customers.

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## Low Jitter Spectrum Clock Generator for Power PC Designs

## Maximum Ratings

Voltage Relative to VSS:               -0.3V

Voltage Relative to VDD:              0.3V

Storage Temperature:       -65ºC to + 150ºC

Operating Temperature:      0ºC to +70ºC

Maximum Power Supply:           7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

## Electrical Characteristics

| Characteristics | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL | - | - | 0.8 | Vdc | - |
| Input High Voltage | VIH | 2.0 | - | - | Vdc | - |
| Input Low Current | IIL | | | -66 | µA | |
| Input High Current | IIH | | | 5 | µA | |
| Tri-State leakage current | Ioz | - | - | 10 | µA | |
| Dynamic Supply Current | Idd | - | - | TBD | mA | CPU = 100 Mhz |
| Static Supply Current | Issd | - | - | TBD | mA | OE= 0 (logic low) |
| Short Circuit Current | ISC | 25 | - | - | mA | 1output at a time-30 seconds |

## Switching Characteristics

| Characteristics | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Duty Cycle | - | 45 | 50 | 55 | % | Measured at 1.5V |
| Skew (CPU to CPU) | TSKEW1 | - | - | ±250 | pS | 30 pF Load Measured at 1.5 pF |
| Skew ( CPU to PCI or PCIF) | TSKEW1 | - | - | ±375 | pS | 30 pF Load Measured at 1.5 pF |
| Skew (PCI or PCIF to PCI) | TSKEW2 | - | - | ±250 | pS | 30 pF Load Measured at 1.5 pF |
| Δ Period Adjacent Cycles | Δ PA | - | - | ±250 | pS | |
| Jitter Spectrum Long Term | Δ PL | | - | ±500 | pS | Measured over 10 seconds |
| **VDD = VDDC =CVDDP = VDDPF = VDDF = VDDR = 3.15-3.45V,  TA = 0ºc TO +70ºC** | | | | | | |

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## TB4L1 BUFFER CHARACTERISTICS FOR CPU, PCI, PCIF, REF and 48M

| Characteristics | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $IOH_{min}$ | -33 | - | - | mA | Vout = 1.0 V |
| Pull-Up Current Max | $IOH_{max}$ | - | - | -33 | mA | Vout = 3.135 V |
| Pull-Down Current Min | $IOL_{min}$ | 30 | - | - | mA | Vout = 1.95 V |
| Pull-Down Current Max | $IOL_{max}$ | - | - | 38 | mA | Vout = .4 V |
| Rise/Fall Time Min between 0.4V and 2.4V | $TRF_{min}$ | 0.5 | - | - | nS | 15 pF Load |
| Rise/Fall Time Max between 0.4V and 2.4V | $TRF_{max}$ | - | - | 2.0 | nS | 30 pF Load |
| **VDD = VDDC =CVDDP = VDDPF = VDDF = VDDR = 3.15-3.45V,  TA = 0°c TO +70°C** | | | | | | |

## Crystal and Reference Oscillator Parameters

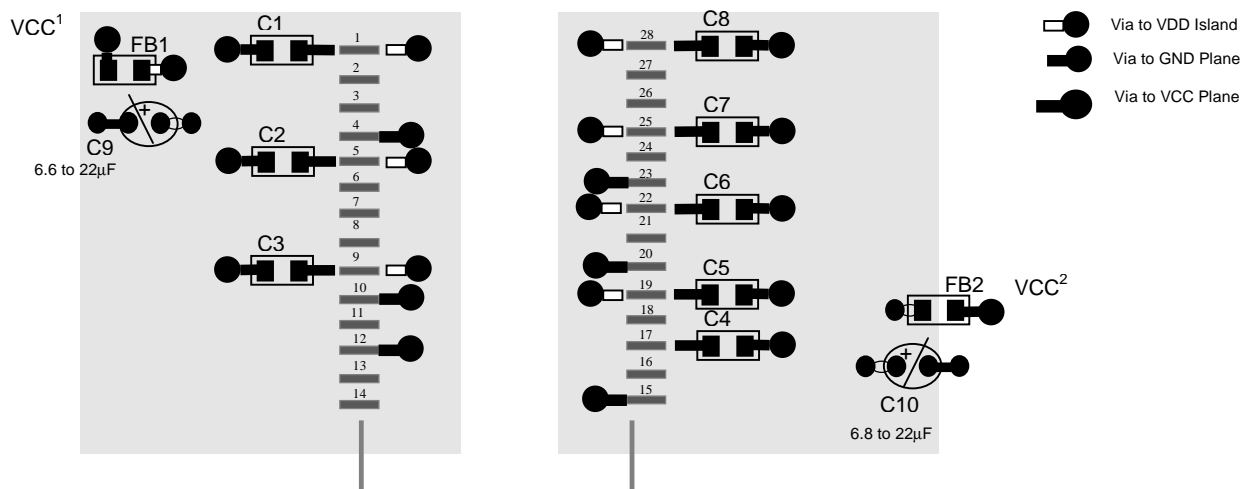| Characteristics | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Frequency | $F_o$ | 12.0 | 14.31818 | 16.00 | MHz | |
| Tolerance | TC | - | - | +/-100 | PPM | Calibration note 1 |
| | TS | - | - | +/-100 | PPM | Stability (Ta-10 to +60C) Note1 |
| | TA | - | - | 5 | PPM | Aging ( First year@ 25C) note 1 |
| Mode | OM | - | - | - | | Parallel Resonant |
| Pin Capacitance | CP | | 36 | | pF | Capacitance of XIN and XOUT pins to ground ( Each) |
| DC Bias Voltage | $V_{Bias}$ | 0.3Vdd | Vdd/2 | 0.7Vdd | V | |
| Start up time | Ts | - | - | 30 | μS | |
| Load Capacitance | CL | - | 20 | - | pF | The crystals rated load note 1 |
| Effective Series Resistance (ESR) | R1 | - | - | 40 | Ohms | |
| Power Dissipation | DL | - | - | 0.10 | mW | Note 1 |
| Shunt Capacitance | CO | - | - | 8 | pF | Crystals internal package capacitance ( total) |
| For maximum accuracy, the total circuit loading capacitance should be equal to CL.  This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors. Budgeting Calculations: Typical trace capacitance, ( <half inch) is 4 pF,  Load to the crystal is therefore  =   2.0 pF Clock generator internal pin capacitance of 36 pF, load to the crystal is therefore = 18.0 pF The total parasitic capacitance would therefore be                                                  = 20.0 pF | | | | | | |

Note 1.  It is recommended but not mandatory that a crystal meets these specifications.

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## PCB Layout Suggestion



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C3, C4, C35, C36, C37, C38, C39 and C40 (all are 1.0µf) should always be used and placed as close as possible to their VDD pins.

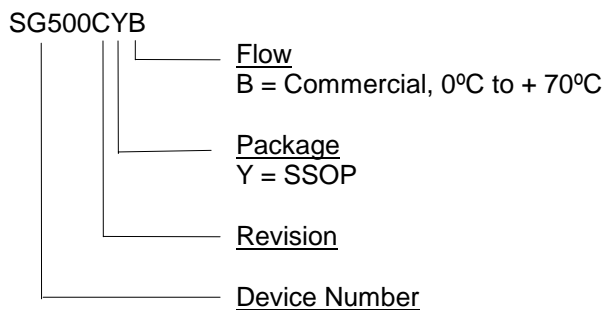## Package Drawing and Dimensions
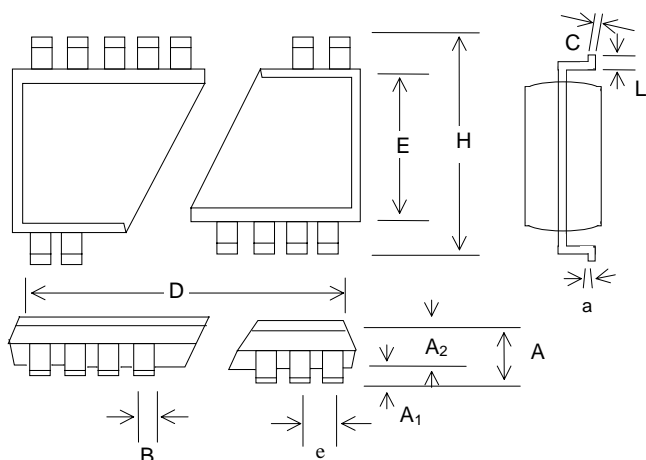


### 28 Pin SSOP Outline Dimensions

| SYMBOL | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.068 | 0.073 | 0.078 | 1.73 | 1.86 | 1.99 |
| $A_1$ | 0.002 | 0.005 | 0.008 | 0.05 | 0.13 | 0.21 |
| A2 | 0.066 | 0.068 | 0.070 | 1.68 | 1.73 | 1.78 |
| B | 0.010 | 0.012 | 0.015 | 0.25 | 0.30 | 0.38 |
| C | 0.005 | 0.006 | 0.009 | 0.13 | 0.15 | 0.22 |
| D | 0.397 | 0.402 | 0.407 | 10.07 | 10.20 | 10.33 |
| E | 0.205 | 0.209 | 0.212 | 5.20 | 5.30 | 5.38 |
| e | 0.0256 BSC | | | 0.65 BSC | | |
| H | 0.301` | 0.307 | 0.311 | 7.65 | 7.80 | 7.90 |
| a | 0° | 4° | 8° | 0° | 4° | 8° |
| L | 0.022 | 0.030 | 0.037 | 0.55 | 0.75 | 0.95 |

## Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| SG500CYB | 28 PIN SSOP | Commercial, 0ºC to +70ºC |

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
SG500CYB
Date Code, Lot #

SG500CYB

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

Device Number

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**Document Title:** SG500 Low Jitter Spectrum Clock Generator for Power PC Designs
**Document Number:** 38-07015

| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
|------|---------|------------|-----------------|-----------------------|
| ** | 106943 | 06/29/01 | IKA | Convert from IMI to Cypress |

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