PRELIMNARY

CYW3335

Dual Serial Input PLL with 2.5-GHz Prescalers

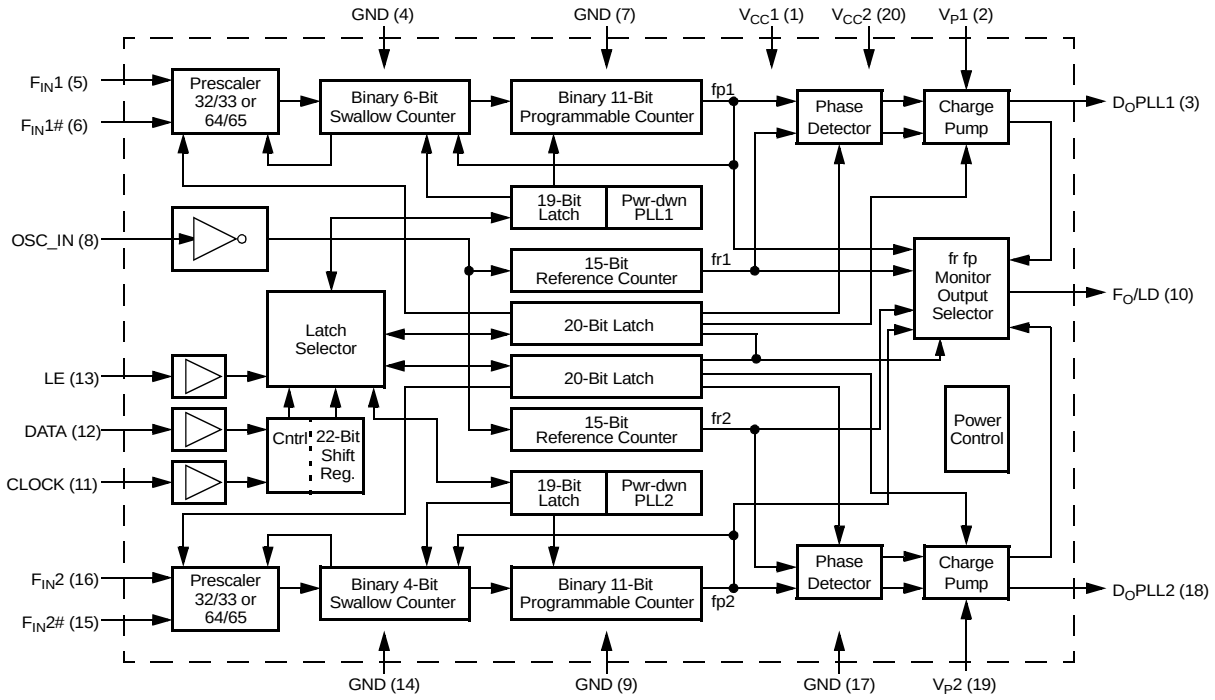
Features

- **Operating voltage 2.7V to 5.5V**
- **PLL1 and PLL2 operating frequency:**
  - **2.5 GHz with prescaler ratios of 32/33 or 64/65**
- **Lock detect feature**
- **Power-down mode I_{CC} < 1 µA typical at 3.0V**
- **Available in a 20-pin TSSOP (Thin Shrink Small Outline Package)**
- **Available in a 24-pin CSP (Chip Scale Package)**
- **Available in a 20-pin MLF (Mirco Lead Frame Package)**

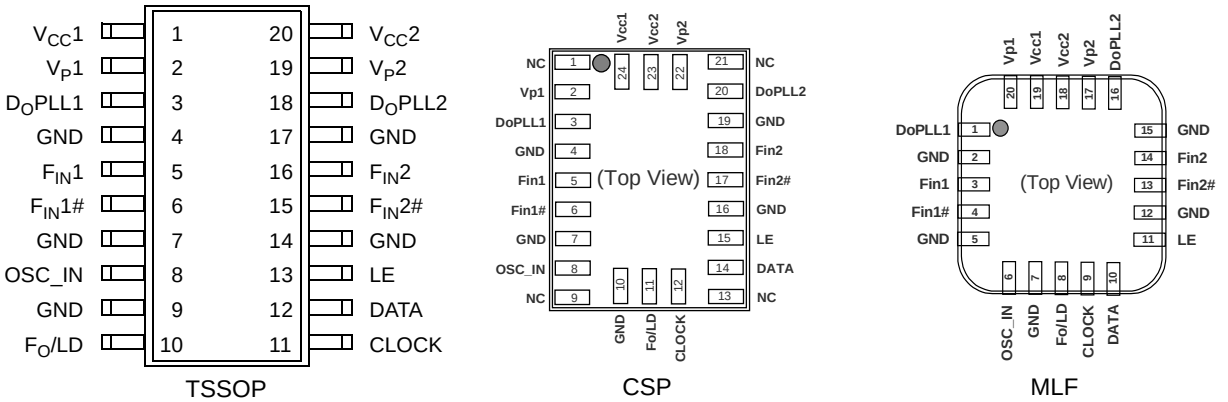
Applications

The Cypress CYW3335 is a dual serial input PLL frequency synthesizer designed to combine the Transmit and Receive RF frequency sections of wireless communications systems. Two 2.5-GHz prescalers, each with pulse swallow capability are included. The device operates from 2.7V and dissipates only 35 mW.

CYW3335 Dual Hi-Lo PLL Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No. (TSSOP)	Pin No. (CSP)	Pin No. (MLF)	Pin Type	Pin Description
$V_{CC}1$	1	24	19	P	***Power Supply Connection for PLL1 and PLL2:*** When power is removed from both the $V_{CC}1$ and $V_{CC}2$ pins, all latched data is lost.
V_P1	2	2	20	P	***PLL1 Charge Pump Rail Voltage:*** This voltage accommodates VCO circuits with tuning voltages higher than the V_{CC} of PLL1.
D_OPLL1	3	3	1	O	***PLL1 Charge Pump Output:*** The phase detector gain is $I_P/2\pi$. Sense polarity can be reversed by setting the FC bit in software (via the Shift Register).
$F_{IN}1$	5	5	3	I	***Input to PLL1 Prescaler:*** Maximum frequency 2.5 GHz.
$F_{IN}1$#	6	6	4	I	***Complementary Input to PLL1 Prescaler:*** A bypass capacitor should be placed as close as possible to this pin and must be connected directly to the ground plane.
OSC_IN	8	8	6	I	***Oscillator Input:*** This input has a $V_{CC}/2$ threshold and CMOS logic level sensitivity.
F_O/LD	10	11	8	O	***Lock Detect Pin of PLL1 Section:*** This output is HIGH when the loop is locked. It is multiplexed to the output of the programmable counters or reference dividers in the test program mode. (Refer to *Table 3* for configuration.)
CLOCK	11	12	9	I	***Data Clock Input:*** One bit of data is loaded into the Shift Register on the rising edge of this signal.
DATA	12	14	10	I	***Serial Data Input***
LE	13	15	11	I	***Load Enable:*** On the rising edge of this signal, the data stored in the Shift Register is latched into the reference counter and configuration controls, PLL1 or PLL2 depending on the state of the control bits.
$F_{IN}2$#	15	17	13	I	***Complementary Input to PLL2 Prescaler:*** A bypass capacitor should be placed as close as possible to this pin and must be connected directly to the ground plane.
$F_{IN}2$	16	18	14	I	***Input to PLL2 Prescaler:*** Maximum frequency 2.5 GHz.
D_OPLL2	18	20	16	O	***PLL2 Charge Pump Output:*** The phase detector gain is $I_P/2\pi$. Sense polarity can be reversed by setting the FC bit in software (via the Shift Register).
V_P2	19	22	17	P	***PLL2 Charge Pump Rail Voltage:*** This voltage accommodates VCO circuits with tuning voltages higher than the V_{CC} of PLL2.
$V_{CC}2$	20	23	18	P	***Power Supply Connections for PLL1 and PLL2:*** When power is removed from both the $V_{CC}1$ and $V_{CC}2$ pins, all latched data is lost.
GND	4, 7, 9, 14, 17	4, 7, 10, 16, 19	2, 5, 7, 12, 15	G	***Analog and Digital Ground Connections:*** This pin must be grounded.
N/C	N/A	1, 9, 13, 21	N/A	N/C	***No Connect.***

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{CC} or V_P	Power Supply Voltage	–0.5 to +6.5	V
V_{OUT}	Output Voltage	–0.5 to V_{CC}+0.5	V
I_{OUT}	Output Current	±15	mA
T_L	Lead Temperature	+260	°C
T_{STG}	Storage Temperature	–55 to +150	°C

Handling Precautions

Devices should be transported and stored in antistatic containers.

These devices are static sensitive. Ensure that equipment and personnel contacting the devices are properly grounded.

Cover workbenches with grounded conductive mats.

Always turn off power before adding or removing devices from system.

Protect leads with a conductive sheet when handling or transporting PC boards with devices.

If devices are removed from the moisture protective bags for more than 36 hours, they should be baked at 85°C in a moisture free environment for 24 hours prior to assembly in less than 24 hours.

Recommended Operating Conditions

Parameter	Description	Test Condition	Rating	Unit
V_{CC1}, V_{CC2}	Power Supply Voltage		2.7 to 5.5	V
V_P	Charge Pump Voltage		V_{CC} to +5.5	V
T_A	Operating Temperature	Ambient air at 0 CFM flow	–40 to +85	°C

Electrical Characteristics: V_{CC} = V_P = 2.7V to 5.5V, T_A = –40°C to +85°C, Unless otherwise specified

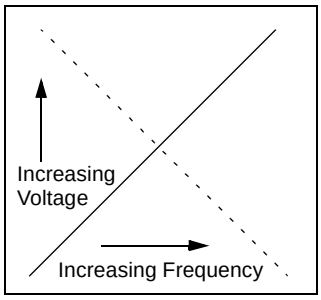
Parameter	Description	Test Condition	Pin	Min.	Typ.	Max.	Unit
I_{CC}	Power Supply Current PLL1 + PLL2	$V_{CC}1 = V_{CC}2 = 3.0V$	$V_{CC}1$, $V_{CC}2$		13.5		mA
I_{PD}	Power-down Current	Power-down, V_{CC} = 3.0V	$V_{CC}1$, $V_{CC}2$		1	25	µA
$F_{IN}1$	Operating Frequency	PLL1	$F_{IN}1$	100		2500	MHz
$F_{IN}2$		PLL2	$F_{IN}2$	100		2500	MHz
F_{OSC}	Oscillator Input Frequency		OSC_IN	5		45	MHz
Fϕ	Phase Detector Frequency					10	MHz
$PF_{IN}1$	Input Sensitivity	V_{CC} = 2.7V	$F_{IN}1$	–15		4	dBm
		V_{CC} = 5.5V		–10		4	dBm
$PF_{IN}2$		V_{CC} = 2.7V to 5.5V	$F_{IN}2$	–10		4	dBm
V_{OSC}	Oscillator Input Sensitivity	V_{CC} = 3.0V	OSC_IN	0.5			V_{P-P}
I_{IH}, I_{IL}	High/Low Level Input Current			-100		100	µA
V_{IH}	High Level Input Voltage	V_{CC} = 3.0V	DATA, CLOCK, LE	V_{CC} * 0.8			V
V_{IL}	Low Level Input Voltage					V_{CC} * 0.2	V
I_{IH}	High Level Input Current			–10	0.5	10	µA
I_{IL}	Low Level Input Current			–10	0.5	10	µA
V_{OH}	High level Output Voltage	V_{CC} = 3.0V, I_{OH} = –1 mA	F_O/LD	V_{CC} * 0.8			V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0V, I_{OL} = 1 mA				V_{CC} * 0.2	V
$ID_{OH(SO)}$	ID_O High, Source Current	$V_{CC} = V_P$ = 3.0V, $D_O = V_P/2$	D_OPLL1 D_OPLL2		–3.8		mA
$ID_{OL(SO)}$	ID_O Low, Source Current				–1		mA
$ID_{OH(SI)}$	ID_O High, Sink Current				3.8		mA
$ID_{OL(SI)}$	ID_O Low, Sink Current				1		mA
ΔID_O	ID_O Charge Pump Sink and Source Mismatch	$V_{CC} = V_P$ = 3.0V, $[IID_{O(SI)}I - IID_{O(SO)}I]/[1/2*\{IID_{O(SI)}]I+IID_{O(SO)}I\}]*100\%$			3	15	%
ID_O vs T	Charge Pump Current Variation vs Temperature	–40°C<T<85°C $V_{DO} = V_P/2$[1]			5		%
I_{OFF}	High-Impedance Leakage Current	$V_{CC} = V_P$ = 3.0V, Loop locked, between reference spikes			±2.5		nA

Note:

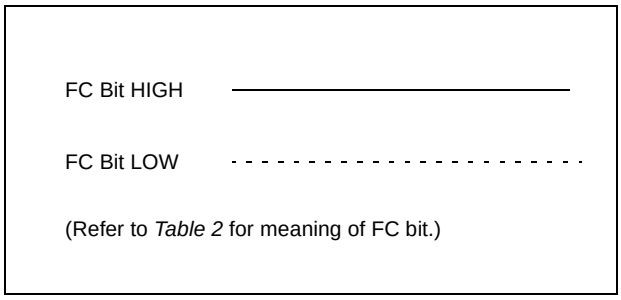
1. ID_Ovs T; Charge pump current variation vs. temperature. $[IID_{O(SI)@T}I - IID_{O(SI)@25°C}I]/IID_{O(SI)@25°C}I * 100\%$ and $[IID_{O(SO)@T}I - IID_{O(SO)@25°C}I]/IID_{O(SO)@25°C}I *100\%$.

Timing Waveforms

Key:

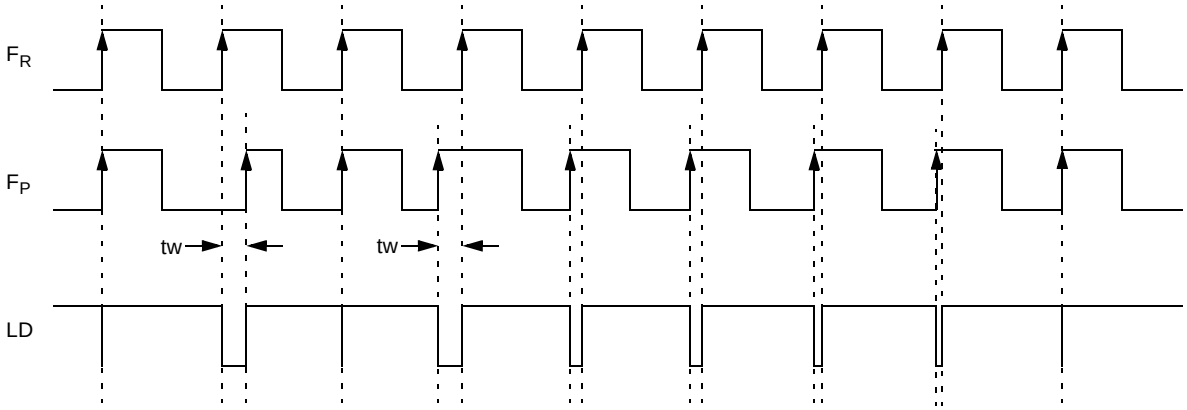


VCO Characteristics

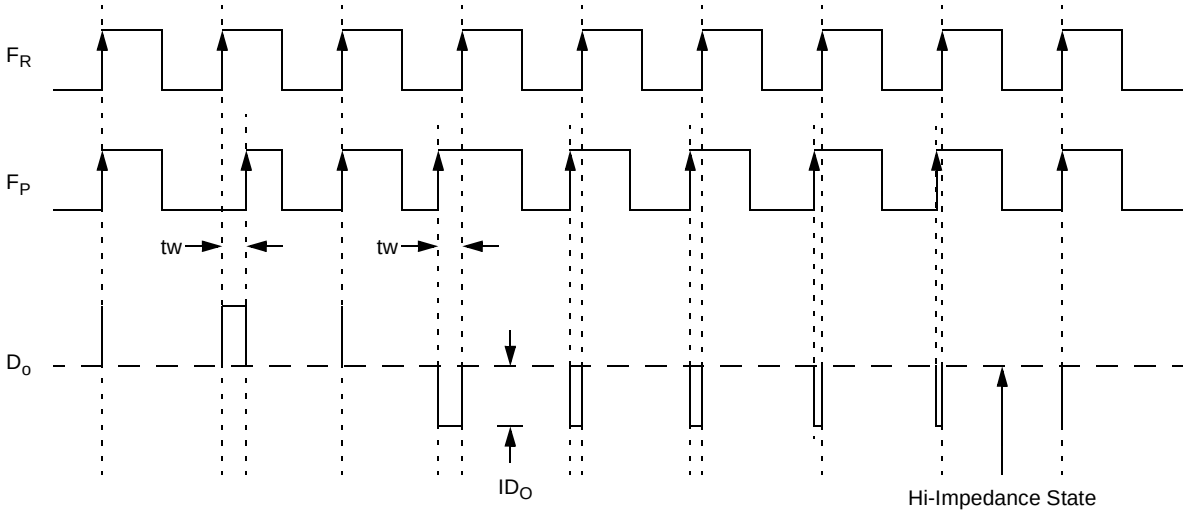


Phase Comparator Sense

Phase Detector Output Waveform

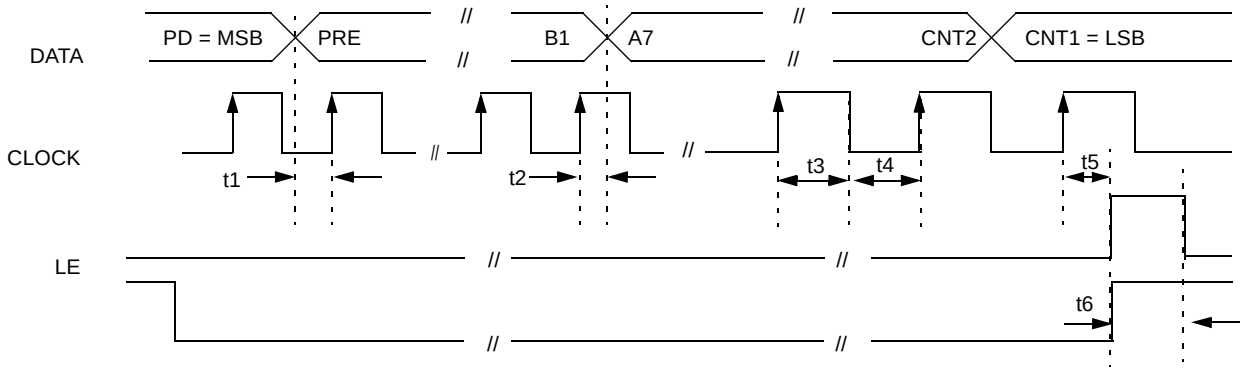


D_O Charge Pump Output Current Waveform



Timing Waveforms (continued)

Serial Data Input Timing Waveform[2, 3, 4, 5]



Serial Data Input

Data is input serially using the DATA, CLOCK, and LE pins. Two control bits direct data as described in *Table 1*.

Table 1. Control Configuration

CNT1	CNT2	Function
0	0	***Program Reference 2***: R = 3 to 32767, set PLL2 (low frequency) phase detector polarity, set current in PLL2, set PLL2 to Hi-Impedance state, set monitor selector to PLL2.
0	1	***Program Reference 1:*** R = 3 to 32767, set PLL1 (high frequency) phase detector polarity, set current in PLL1, set PLL1 to Hi-Impedance state, set monitor selector to PLL1
1	0	***Program Counter for PLL2:*** A = 0 to 63 B = 3 to 2047, set PLL2 prescaler ratio, set PLL2 to power-down.
1	1	***Program Counter for PLL1:*** A = 0 to 63, B = 3 to 2047, set PLL1 prescaler ratio, set PLL1 to power-down.

Notes:
2. t1–t6 = t > 50 ns.
3. CLOCK may remain HIGH after latching in data.
4. DATA is shifted in with the MSB first.
5. For DATA definitions, refer to *Table 2*.

Table 2. Shift Register Configuration[6]

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Reference Counter and Configuration Bits																					
CNT1	CNT2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	FC	IDO	TS	LD	FO
Programmable Counter bits																					
CNT1	CNT2	A1	A2	A3	A4	A5	A6	A7	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	PRE	PD

Bit(s) Name	Function
CNT1, CNT2	***Control Bits:*** Directs programming data to PLL1 (high frequency) or PLL2 (low frequency).
R1–R15	***Reference Counter Setting Bits:*** 15 bits, R = 3 to 32767.[7]
FC	***Phase Sense of the Phase Detector:*** Set to match the VCO polarity, H = + (Positive VCO transfer function).
IDO	***Charge Pump Setting Bit:*** ID_O HIGH = 3.8 mA, ID_O LOW = 1 mA at V_P = 3V.
TS	***Hi-Impedance State Bit:*** Makes D_O Hi-Impedance for PLL1 and PLL2 when HIGH.
LD	***Lock Detect:*** Directs the lock detect signal source pin 10. Pin 10 is HIGH with narrow low excursions when locked. When not locked, this pin is LOW.
FO	***Frequency Out:*** This bit can be set to read out reference or programmable divider at the LD pin for test purposes.
PRE	***Prescaler Divide Bit:*** For PLL1: LOW = 32/33 and HIGH = 64/65. For PLL2: LOW = 32/33 and HIGH = 64/65.
PD	***Power-down:*** LOW = power-up and HIGH = power-down. F_{IN} is at a high-impedance state, respective B counter is disabled, forces D_O outputs to Hi-Impedance and phase comparators are disabled. The reference counter is disabled and the OSC input is high-impedance after both PLLs are powered down. Data can be input and latched in the power-down state.
A1–A6	***Swallow Counter Divide Ratio:*** A = 0 to 63 for PLL1 and PLL2.
B1–B11	***Programmable Counter Divide Ratio:*** B = 3 to 2047.[7]

Table 3. F_O/LD Pin Truth Table

FO (Bit 22)		LD (Bit 21)		F_O/LD Pin Output State
PLL1	PLL2	PLL1	PLL2	
0	0	0	0	Disable
0	0	0	1	PLL2 Lock Detect
0	0	1	0	PLL1 Lock Detect
0	0	1	1	PLL1/PLL2 Lock Detect
0	1	X	0	PLL2 Reference Divider Output
1	0	X	0	PLL1 Reference Divider Output
0	1	X	1	PLL2 Programmable Divider Output
1	0	X	1	PLL1 Programmable Divider Output
1	1	0	1	PLL2 Counter Reset
1	1	1	0	PLL1 Counter Reset
1	1	1	1	PLL1/PLL2 Counter Reset

Notes:
6. The MSB is loaded in first.
7. Low count ratios may violate frequency limits of the phase detector.

Table 4. 6-Bit Swallow Counter (A) Truth Table[8]

Divide Ratio A	A7	A6	A5	A4	A3	A2	A1
PLL1							
0	X	0	0	0	0	0	0
1	X	0	0	0	0	0	1
:::	:::	:::	:::	:::	:::	:::	:::
62	X	1	1	1	1	1	0
63	X	1	1	1	1	1	1
PLL2							
0	X	0	0	0	0	0	0
1	X	0	0	0	0	0	1
:::	:::	:::	:::	:::	:::	:::	:::
62	X	1	1	1	1	1	0
63	X	1	1	1	1	1	1

Table 5. 11-Bit Programmable Counter (B) Truth Table[9]

Divide Ratio B	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::
2046	1	1	1	1	1	1	1	1	1	1	0
2047	1	1	1	1	1	1	1	1	1	1	1

Table 6. 15-Bit Programmable Reference Counter (for PLL1 and PLL2) Truth Table[9]

Divide Ratio R	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::
32766	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Ordering Information[10]

Ordering Code	Package Name	Package Type	Tape and Reel Option
CYW3335	ZI BCI LFI	20-pin Thin Shrink Small Outline Package (0.173” wide) 24-pin Chip Scale Package (3.5 mm X 4.5 mm) 20-pin Micro Lead Frame (4 mm x 4 mm)	TR

Notes:

8. B is greater than or equal to A.
9. Divide ratio less than 3 is prohibited. The divide ratio can be calculated using the following equation:
   fvco = {(P * B) + A} * fosc / R where (A ≤ B)

   fvco: Output frequency of the external VCO.

   fosc: The crystal reference oscillator frequency.

   A: Preset divide ratio of the 6-bit swallow counter (0 to 63).

   B: Preset ratio of the 11-bit programmable counter (3 to 2047).

   P: Preset divide ratio of the dual modulus prescaler.

   R: Preset ratio of the 15-bit programmable reference counter (3 to 32767).
   The divide ratio N = (P * B) + A.
10. Operating temperature range: –40°C to +85°C.

Typical Performance Characteristics

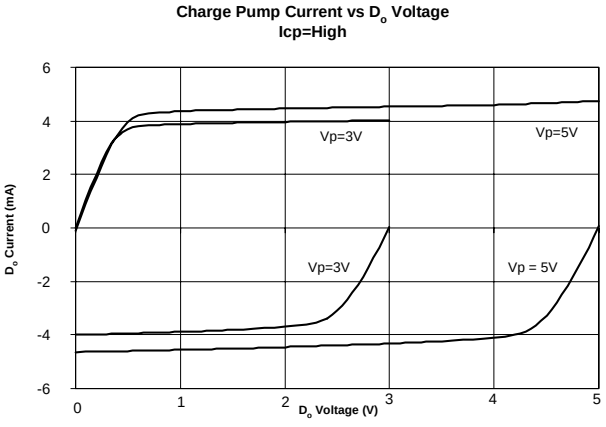


Figure 1.
D_o Output Current High Mode

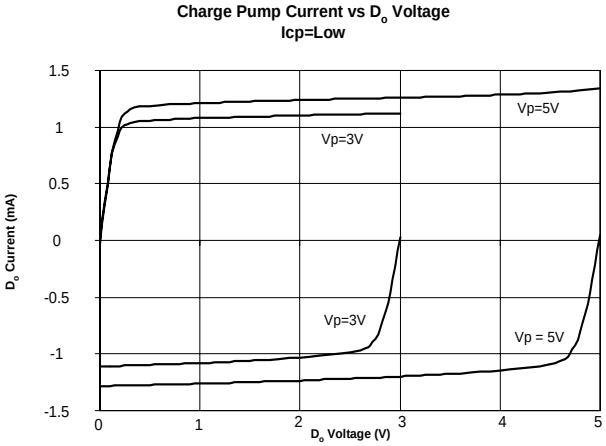


Figure 3.
D_o Output Current Low Mode

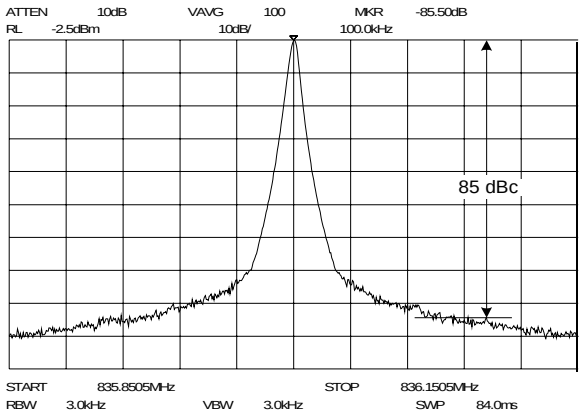
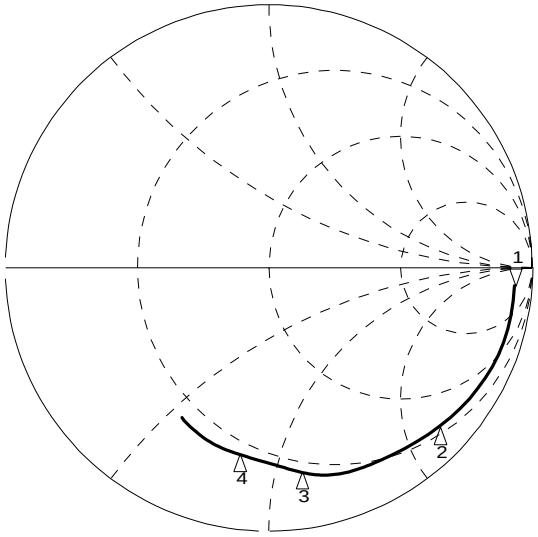


Figure 3. PLL Reference Spurs
PLL Reference Spurious Level is –85.5 dBc

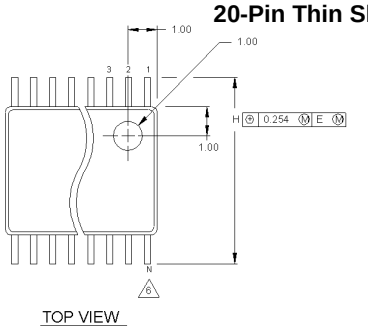


Marker Reference Number	Real	Imaginary	Input Frequency
Marker 1	623	-823	100 MHz
Marker 2	21	-120	1 GHz
Marker 3	14	-55	1.8 GHz
Marker 4	13	-39	2.2 GHz

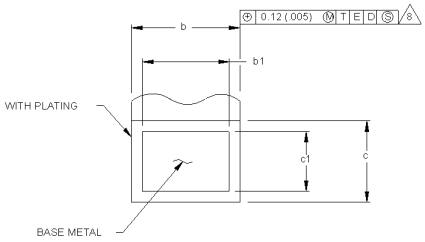
Figure 4.
Input Impedance $F_{IN}1$, $F_{IN}2$
VCC = 2.7 to 5.5V, F_{IN} = 75 MHz to 2.6 GHz

Package Diagram

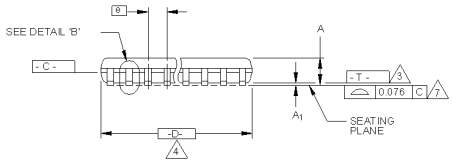
20-Pin Thin Shrink Small Outline Package (TSSOP, 0.173" wide)



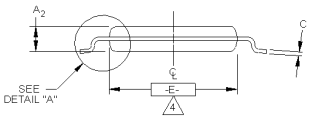
TOP VIEW



DETAIL "C"
SCALE: 120/1
(SEE NOTE 9)

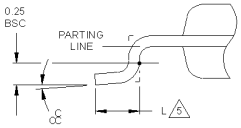


SIDE VIEW

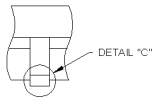


END VIEW

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (.0110±.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm. SEE DETAILS 'B' AND 'C'.
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.



DETAIL 'A'
(SCALE: 30/1)



DETAIL "B"
(SCALE: 30/1)
DAMBAR PROTRUSION

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4 D VARIATIONS			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A			1.10		AA	2.90	3.00	3.10	8
A_1	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A_2	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	-	0.30	8	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	-	0.20		AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
θC	0°	4°	8°						

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4 D VARIATIONS			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A			.0433		AA	.114	.118	.122	8
A_1	.002	.004	.006		AB	.193	.197	.201	14
A_2	.0335	.0354	.0374		AC	.193	.197	.201	16
b	.0075	-	.0118	8	AD	.252	.256	.260	20
b1	.0075	.0087	.0098		AE	.303	.307	.311	24
c	.0035	-	.0079		AF	.378	.382	.386	28
c1	.0035	.0050	.0053						
D	SEE VARIATIONS			4					
E	.169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	.020	.024	.028	5					
N	SEE VARIATIONS			6					
θC	0°	4°	8°						

VARIATION AF IS DESIGNED BUT NOT TOOLED

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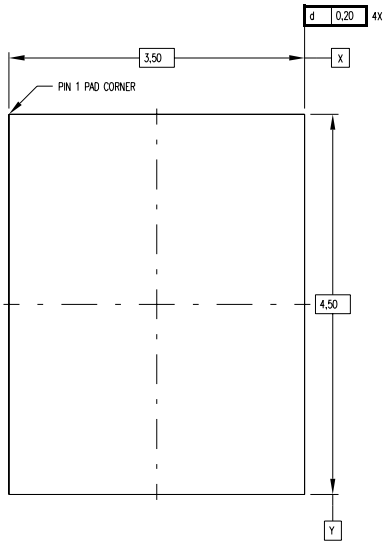
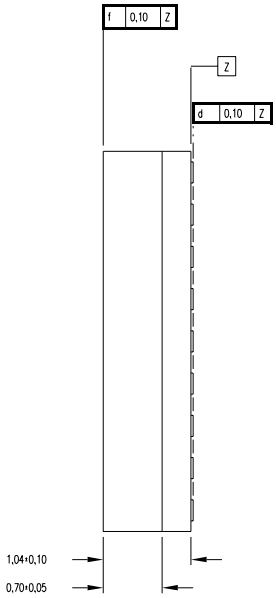
Package Diagram

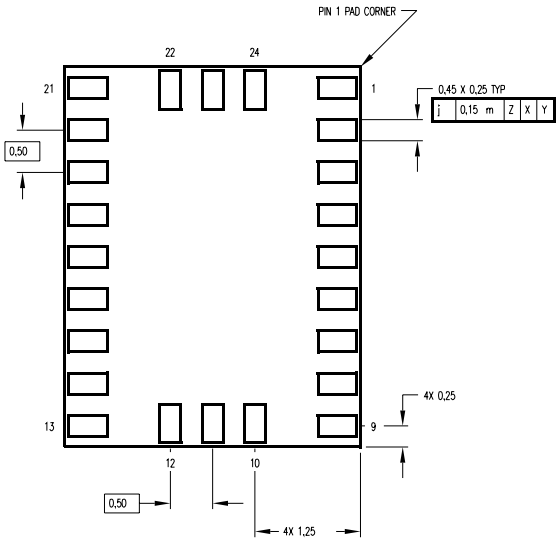
24-Pin Chip Scale Package (CSP 3.5 mm X 4.5 mm)



TOP VIEW



SIDE VIEW

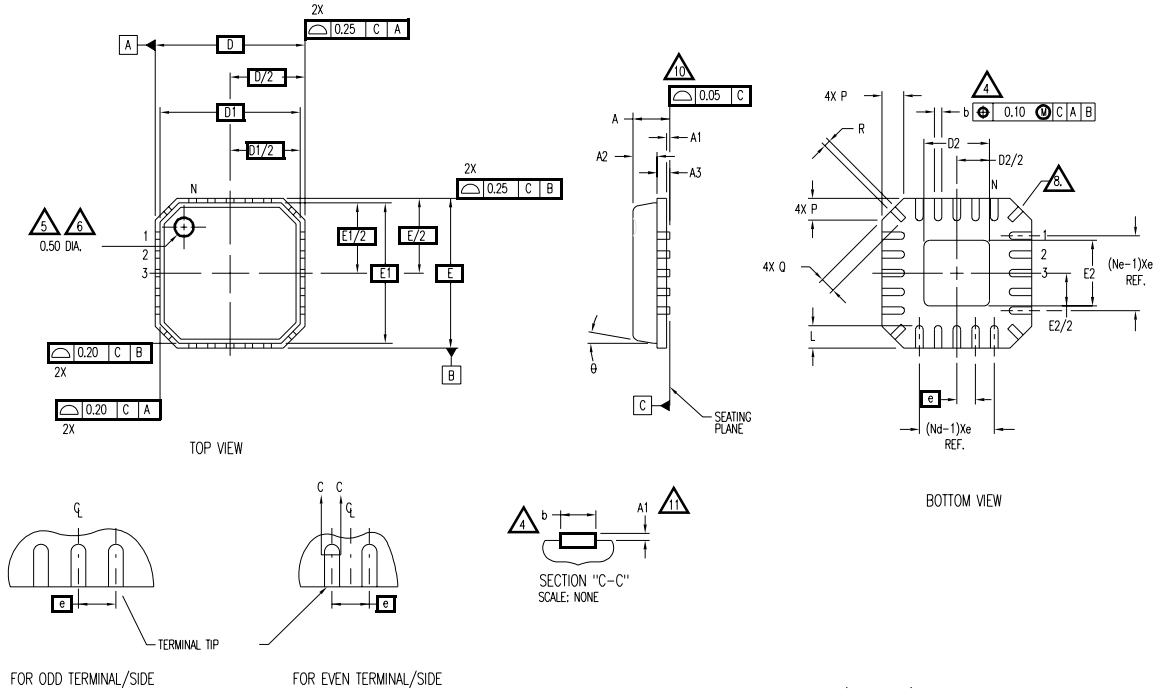


BOTTOM VIEW

ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994, UNLESS OTHERWISE SPECIFIED

Package Diagram

20-Pin Micro Lead Frame Package (MLF 4 mm X 4 mm)



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	
e		0.50 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.50	0.60	0.75	
b	0.18	0.23	0.30	4
Q	0.30	0.40	0.65	
D2	1.55	1.70	1.85	
E2	1.55	1.70	1.85	

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110502	01/07/02	SZV	Change from Spec number: 38-00964 to 38-07237