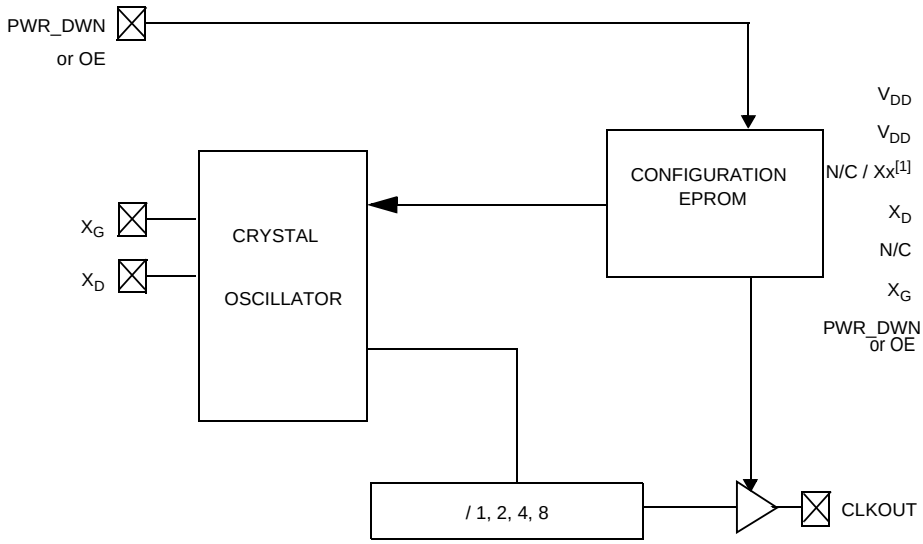
CY5039

High-accuracy EPROM-programmable Capacitor Tuning Array Die for Crystal Oscillators

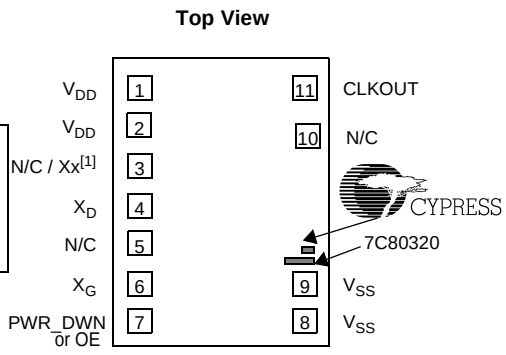
Features	Benefits
• **EPROM-programmable capacitor tuning array with shadow register**	Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
• **Twice-programmable die**	EPROM redundancy allows two programming opportunities to correct errors, and control excess inventory
• **Simple four-pin programming interface**	Enables programming of output frequency after packaging
• **On-chip oscillator runs from 10 – 30 MHz crystal**	Lowers cost of oscillator as PPM manufacturing error can be tweaked in package
• **EPROM-selectable TTL or CMOS duty cycle levels**	Duty cycle centered at 1.4V or $V_{DD}/2$ Provides flexibility to service most TTL or CMOS applications
• **Four selectable post-divide options, using reference oscillator output**	Provides flexibility in output configurations and testing
• **Programmable PWR_DWN or OE pin**	Enables low-power operation or output enable function
• **Programmable asynchronous or synchronous OE and PWR_DWN modes**	Provides flexibility for system applications, through selectable instantaneous or synchronous change in outputs
• **3.3V or 5V operation**	Lowers inventory cost as same die services both applications
• **Small die**	Enables encapsulation in small-size, surface-mount packages
• **Controlled rise and fall times and output slew rate**	Lower EMI than oscillators

Logic Block Diagram



Die Configuration

Top View



Note:

1. For customers not bonding X_D or X_G pad to external pins, an alternative bonding option would be shorting the Xx pad to the X_D pad.

Functional Description

The CY5039 is a high-accuracy IC designed for the crystal oscillator market. The die attaches directly to a low-cost 10–30 MHz crystal and can be packaged into four-pin through-hole or surface mount packages. The oscillator devices can be stocked as blank parts and PPM error programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

The CY5039 contains an on-chip oscillator and a unique oscillator tuning circuit for fine-tuning of the output frequency. The crystal C_{load} can be selectively adjusted by programming a set of seven EPROM bits. This feature can be used to compensate for crystal variations or to obtain a more accurate frequency.

The CY5039 uses EPROM programming with a simple two-wire, four-pin interface that includes V_{SS} and V_{DD}. The entire configuration can be reprogrammed one time allowing programmed inventory to be altered or reused.

The CY5039 also contains flexible power management control. The part includes both PWR_DWN and OE features with integrated pull-up resistors. The PWR_DWN and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal. When PWR_DWN or OE modes are enabled, CLKOUT is pulled low by a weak pull down. The weak pull-down is easily overdriven by another active CLKOUT for applications that require multiple CLKOUTs on a single signal path.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY5039 to have low jitter and accurate outputs making it suitable for most PC, networking and consumer applications.

EPROM Configuration Block

The following table summarizes the features that are configurable by EPROM. Please refer to the *7C80320 Programming Specification*, which can be obtained from your local Cypress representative, for further information.

EPROM Adjustable Features
Output divider selection
Oscillator Tuning (load capacitance values)
Duty cycle levels (TTL or CMOS)
Power management mode (OE or PWR_DWN)
Power management timing (synchronous or asynchronous)

Power Management Features

The CY5039 contains EPROM-programmable PWR_DWN and OE functions. If power-down is selected, all active circuitry on the chip is shut down when the control pin goes LOW. The oscillator must re-start when the part leaves Powerdown Mode. If Output Enable mode is selected, the output is three-stated and weakly pulled LOW when the Control pin goes LOW. In this mode the oscillator circuit continues to operate, allowing a rapid return to normal operation when the Control input is deasserted.

In addition, the PWR_DWN and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the power-down or output three-state occurs immediately (allowing for logic delays) regardless of position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before power-down or output enable is initiated, thus preventing output glitches.

Crystal Oscillator Tuning Circuit

The CY5039 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of eleven load capacitors on both sides of the oscillator drive inverter. The capacitor load values are EPROM-programmable and can be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.27 pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in the table on page 3. Please refer to the *7C80320 Programming Specification* for further details.

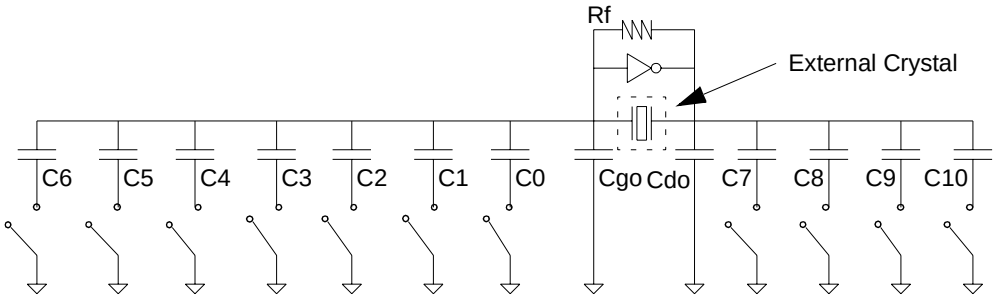
Die Pad Summary

Name	Die Pad	Description
V_{DD}	1,2	Voltage supply.
V_{SS}	8,9	Ground.
X_D	4	Crystal connection
X_x	3	No connect. (For customers not bonding X_D or X_G pad to external pins, an alternative bonding option would be shorting this pad to XD pad.)
X_G	6	Crystal connection
PWR_DWN/OE	7	EPROM programmable power down or output enable pad. Weak pull up.
CLKOUT	11	Clock output. Weak pull down.
N/C	5,10	No connect. (Do not bond to these pads.)

Device Functionality: Output Frequencies

Parameter	Description	Condition	Min.	Max.	Unit
Fo	Output frequency	V_{DD} = 4.5 – 5.5V	1.25	30	MHz
		V_{DD} = 2.7 – 3.6V	1.25	30	MHz

Crystal Oscillator Tuning Circuit



C = LOAD CAPACITOR

Parameter	Description	Min.	Typ.	Max.	Unit
R_f	Feedback resistor, V_{DD} = 4.5 – 5.5V Feedback resistor, V_{DD} = 2.7 – 3.6V	0.5 1.0	2 4	3.5 9.0	MΩ MΩ
	Capacitors have ±10% tolerance				
C_g	Gate capacitor		13		pF
C_d	Drain capacitor		9		pF
C_0	Series cap		0.27		pF
C_1	Series cap		0.52		pF
C_2	Series cap		1.00		pF
C_3	Series cap		0.7		pF
C_4	Series cap		1.4		pF
C_5	Series cap		2.6		pF
C_6	Series cap		5.0		pF
C_7	Series cap		0.45		pF
C_8	Series cap		0.85		pF
C_9	Series cap		1.7		pF
C_{10}	Series cap		3.3		pF

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5 to + 7.0V

Input and Output Voltage .....–0.5V to V_{DD} + 0.5V

Input Current ..... –1 mA to 1 mA

Storage Temperature (Non-Condensing) ... –55°C to +150°C

Junction Temperature ..... –40°C to +100°C

Static Discharge Voltage .....> = 2000V (per MIL-STD-883, Method 3015)

Output Current with absolute max output voltage ..... –10 mA to 10 mA

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage (3.3V) Supply Voltage (5.0V)	2.7 4.5	3.6 5.5	V V
T_{AJ} [2]	Operating Temperature, junction	–10	+100	°C
C_{TTL}	Max. Capacitive Load on outputs for TTL levels		25	pF
C_{CMOS}	Max. Capacitive Load on outputs for CMOS levels		25	pF
X_{REF}	Reference Frequency, input crystal	10	30	MHz

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level Input Voltage	V_{DD} = 4.5 – 5.5V V_{DD} = 2.7 – 3.6V			0.8 0.2V_{DD}	V V
V_{IH}	High-level Input Voltage	V_{DD} = 4.5 – 5.5V V_{DD} = 2.7 – 3.6V	2.0 0.7V_{DD}			V V
V_{OL}	Low-level Output Voltage	V_{DD} = 4.5 – 5.5V, I_{OL}= 16 mA V_{DD} = 2.7 – 3.6V, I_{OL}= 8 mA			0.4 0.4	V V
V_{OHCMOS}	High-level Output Voltage, CMOS levels	V_{DD} = 4.5 – 5.5V, I_{OH}= –16 mA V_{DD} = 2.7 – 3.6V, I_{OH}= –8 mA	V_{DD} – 0.4 V_{DD} – 0.4			V V
V_{OHTTL}	High-level Output Voltage, TTL levels	V_{DD} = 4.5 – 5.5V, I_{OH}= –8 mA	2.4			V
I_{IL}	Input LOW Current	V_{IN} = 0V	–10			µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			5	µA
I_{DD}	Power Supply Current, Unloaded	V_{DD} = 4.5 – 5.5V V_{DD} = 2.7 – 3.6V			45 25	mA mA
I_{DDS}[4]	Stand-by current	V_{DD} = 2.7 – 3.6V		10	50	µA
R_{UP}	Input Pull-up Resistor	V_{DD} = 4.5 – 5.5V, V_{IN} = 0V V_{DD} = 4.5 – 5.5V, V_{IN} = 0.7 V_{DD}	1.1 50	3.0 100	8.0 200	MΩ kΩ
I_{OE_CLKOUT}	CLKOUT Pull-down current	V_{DD} = 5.0		20		µA

Notes:

2. This product is sold in die form so operating conditions are specified for the die, or for junction temperature.
3. This part was characterized in a 20-pin SOIC package with external crystal; electrical characteristics may change with other package types.
4. If external reference is used, it is required to stop the reference (set reference to LOW) during power-down.

Output Clock Switching Characteristics Over the Operating Range

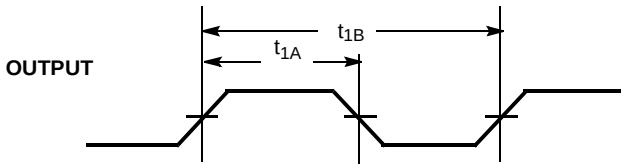
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{1w}	Output Duty Cycle at 1.4V, V_{DD} = 4.5–5.5V $t_{1w} = t_{1A} \div t_{1B}$	1 – 30 MHz, C_L <= 25 pF (TTL output)	45		55	%
t_{1x}	Output Duty Cycle at $V_{DD}/2$, V_{DD} = 4.5–5.5V $t_{1x} = t_{1A} \div t_{1B}$	1 – 30 MHz, C_L <= 25 pF (CMOS output)	45		55	%
t_{1y}	Output Duty Cycle at $V_{DD}/2$, V_{DD} = 2.7–3.6V $t_{1y} = t_{1A} \div t_{1B}$	1 – 30 MHz, C_L <= 25 pF (CMOS output)	45		55	%
t_{2t}	Output Clock Rise time	Between 0.8 – 2.0V, V_{DD} = 4.5V – 5.5V			2.0	ns
t_{2c}	Output Clock Rise time	Between $0.2V_{DD}$ – $0.8V_{DD}$, V_{DD} = 4.5V – 5.5V Between $0.2V_{DD}$ – $0.8V_{DD}$, V_{DD} = 2.7V – 3.6V			4.0 4.0	ns ns
t_{3t}	Output Clock Fall time	Between 2.0 – 0.8V, V_{DD} = 4.5V – 5.5V			2.0	ns
t_{3c}	Output Clock Fall time	Between $0.8V_{DD}$ – $0.2V_{DD}$, V_{DD} = 4.5V – 5.5V Between $0.8V_{DD}$ – $0.2V_{DD}$, V_{DD} = 2.7V – 3.6V			4.0 4.0	ns ns
t_4	Start-up Time Out of Power-down	PWR_DWN pin transition LOW to HIGH until output stable		5	10	ms
t_{5a}	Power-down Delay Time (synchronous setting)	From PWR_DWN pin at or below V_{IL} to output LOW (T = period of output CLK)		T/2	T +10	ns
t_{5b}	Power-down Delay Time (asynchronous setting)	From PWR_DWN pin at or below V_{IL} to output LOW		10	15	ns
t_6	Power-up Time	From power on at or above V_{DD} – 10% to within frequency specification[5]		5	10	ms
t_{7a}	Output Disable Time (synchronous setting)	From OE pin at or below V_{IL} to output Hi-Z (T = period of output CLK)		T/2	T + 10	ns
t_{7b}	Output Disable Time (asynchronous setting)	From OE pin at or below V_{IL} to output Hi-Z		10	15	ns
t_8	Output Enable Time	OE pin LOW to HIGH (T = period of output CLK)			1.5T + 25	ns
t_9	RMS Period Jitter	Over 6000 cycles			25	ps
t_{10}	Cycle to Cycle Jitter	Over 6000 cycles			100	ps

Note:

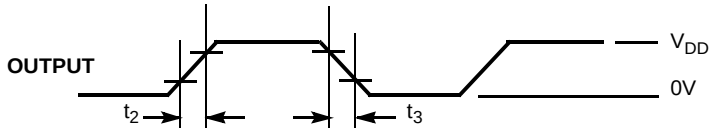
5. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70Ω.

Switching Waveforms

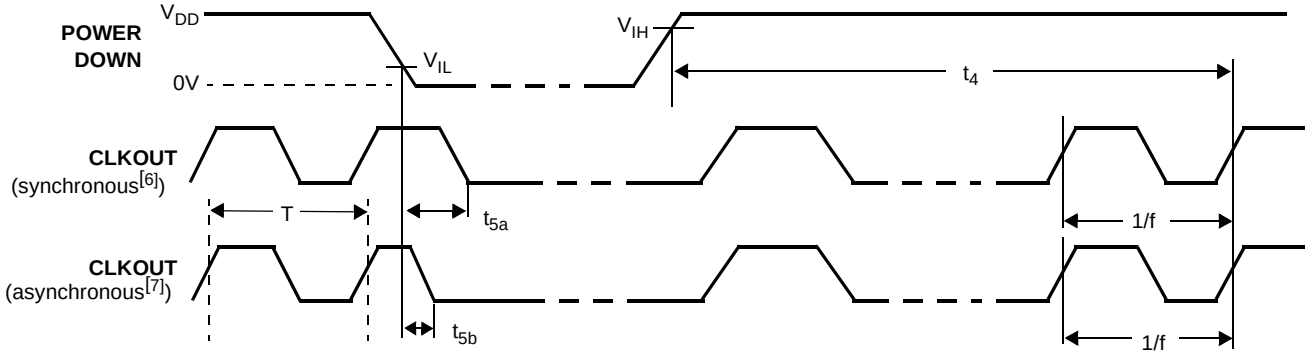
Duty Cycle Timing (t_{1w}, t_{1x}, t_{1y}, t_{1z})



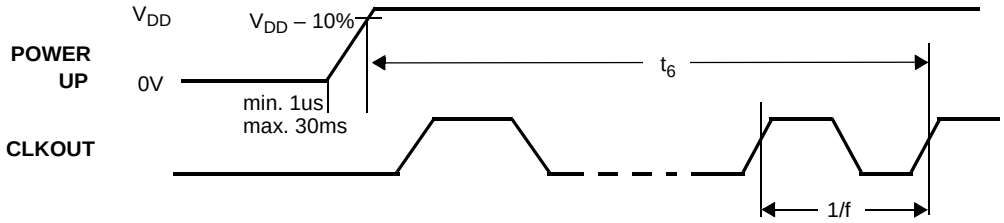
Output Rise/Fall Time



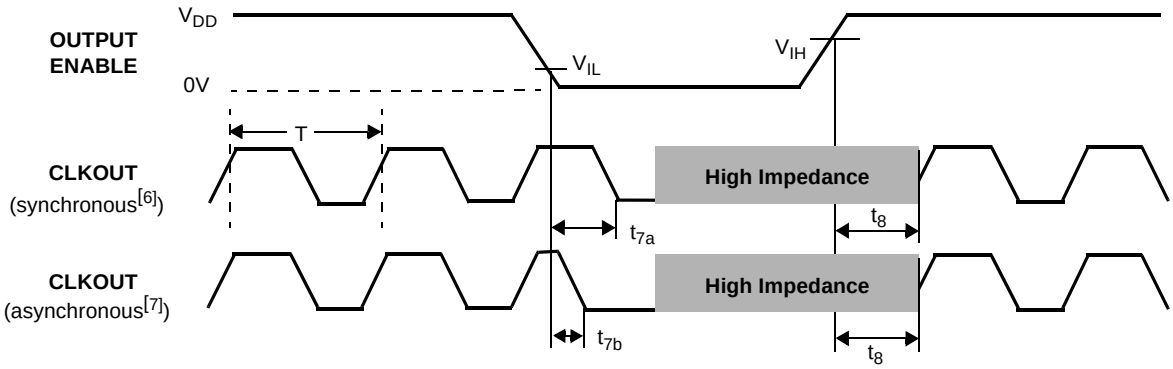
Power Down Timing (synchronous and asynchronous modes)



Power Up Timing



Output Enable Timing (synchronous and asynchronous modes)



Notes:

6. In synchronous mode the power-down or output three-state is not initiated until the next falling edge of the output clock.
7. In asynchronous mode the power-down or output three-state occurs within 25 ns, regardless of position in the ouput clock cycle.

Ordering Information

Ordering Code	Type	Operating Range
CY5039WAF	Wafer	–10°C – 40°C

Die Size Dimensions

x by y	1497 × 1105 microns
Wafer Thickness	14 ± 0.5 mils

Document Title: CY5039 High-accuracy EPROM Programmable Capacitor Tuning Array Die for Crystal Oscillators Document Number: 38-07358				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112253	12/09/02	DSG	Change from Spec number: 38-01097 to 38-07358
*A	113701	05/06/02	CKN	Added “and Output” to Absolute Max. Ratings on p. 5 Added I_{OH} and I_{OL} rows to Electrical Characteristics table on p. 5 Removed 10 in the Max. column of the I_{IL} row and added –10 in the Min. column