CY29962

## 2.5V/3.3V, 150-MHz Multi-Output Zero Delay Buffer

Features

- 2.5V or 3.3V operation
- Output frequency up to 150 MHz
- Supports PowerPC® and Pentium® processors
- 21 clock outputs: drive up to 42 clock lines
- LVPECL or LVCMOS/LVTTL clock Input
- Output-to-Output Skew < 150 ps
- Split 2.5V/3.3V outputs
- Spread-Spectrum-compatible
- Glitch-free output clocks transitioning
- Output disable control
- Pin-compatible with MPC9600
- Industrial temperature range: –40°C to +85°C
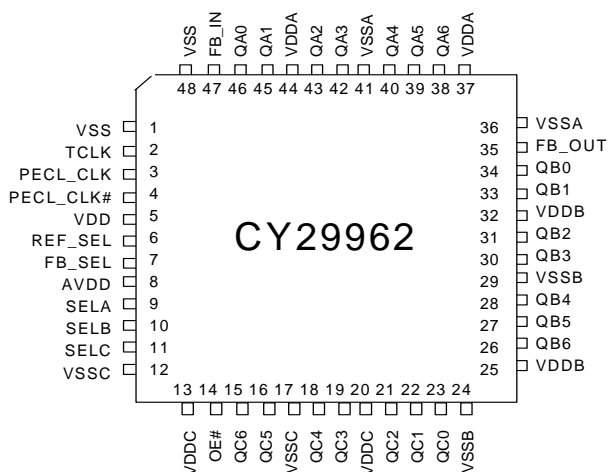- 48-pin TQFP package

Table 1. Frequency Table[1]

SELA	QA	SELB	QB	SELC	QC	FB_SEL	FB_OUT
0	VCO/2	0	VCO/2	0	VCO/2	0	VCO/8
1	VCO/4	1	VCO/4	1	VCO/4	1	VCO/12

Block Diagram
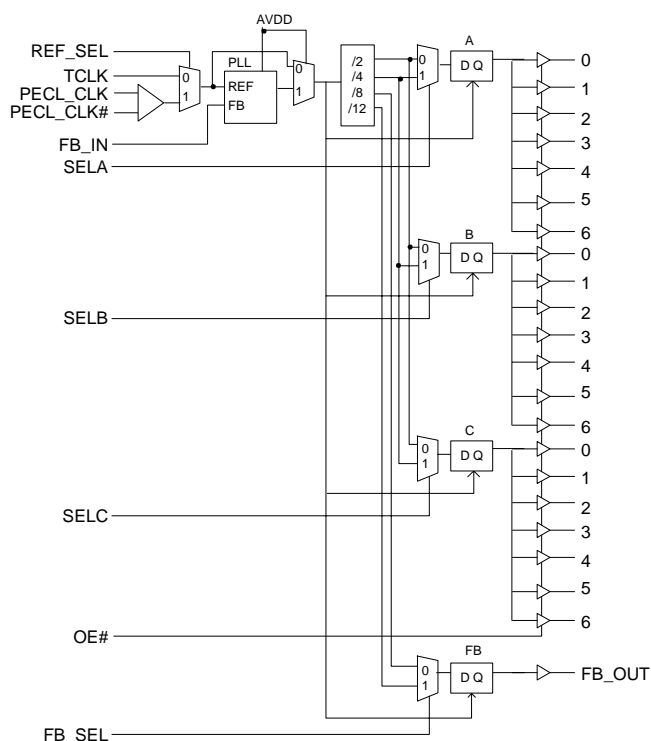
Pin Configuration

Note:
1. Input frequency range: 16 MHz to 33 MHz (FB_SEL = 1) or 25 MHz to 50 MHz (FB_SEL = 0).

Pin Description[2]

Pin	Name	PWR	I/O	Description
3	PECL_CLK		I, PD	PECL clock input
4	PECL_CLK#		I, PU	PECL clock input
2	TCLK		I, PD	External reference/test clock input
38, 39, 40, 42, 43, 45, 46	QA(6:0)	VDDA	O	**Clock Outputs**. See *Table 1* for frequency selections.
26, 27, 28, 30, 31, 33, 34	QB(6:0)	VDDB	O	**Clock Outputs**. See *Table 1* for frequency selections.
15, 16, 18, 19, 21, 22, 23	QC(6:0)	VDDC	O	**Clock Outputs**. See *Table 1* for frequency selections.
35	FB_OUT	VDD	O	**Feedback Clock Output**. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL; see *Table 1*. A bypass delay capacitor at this output will control Input Reference/ Output Banks phase relationships.
9	SELA		I, PU	**Frequency Select Inputs**. These inputs select the divider ratio at QA(0:6) outputs. See *Table 1*.
10	SELB		I, PU	**Frequency Select Inputs**. These inputs select the divider ratio at QB(0:6) outputs. See *Table 1*.
11	SELC		I, PU	**Frequency Select Inputs**. These inputs select the divider ratio at QC(0:6) outputs. See *Table 1*.
7	FB_SEL		I, PU	**Feedback Select Inputs**. These inputs select the divide ratio at FB_OUT output. See *Table 1*.
47	FB_IN		I, PD	**Feedback Clock Input**. Connect to FB_OUT for accessing the PLL.
6	REF_SEL		I, PU	**Reference Select Input**. When HIGH, the PECL clock is selected. When LOW, TCLK is the reference clock.
14	OE#		I, PD	**Output Enable Input**. When asserted LOW, enables all of the outputs. When pulled HIGH, disables to high impedance all of the outputs except FB_OUT.
37, 44	VDDA			Power supply for Bank A clock buffers
25, 32	VDDB			Power supply for Bank B clock buffers
13, 20	VDDC			Power supply for Bank C clock buffers
5	VDD			Power supply for core
8	AVDD			**Power Supply for PLL**. When AVDD is set LOW, PLL is bypassed.
36, 41	VSSA			Common ground for Bank A
24, 29	VSSB			Common ground for Bank B
12, 17	VSSC			Common ground for Bank C
1, 48	VSS			Common ground

Table 2. Function Table

Control Pin	0	1
REF_SEL	TCLK	PECL_CLK
AVDD	PLL Bypass, outputs controlled by OE#	PLL power
OE#	Outputs Enabled	Outputs Disabled (except FB_OUT)
SELA	Output Bank A at VCO/2	Output Bank A at VCO/4
SELB	Output Bank B at VCO/2	Output Bank B at VCO/4
SELC	Output Bank C at VCO/2	Output Bank C at VCO/4
FB_SEL	Feedback Output at VCO/8	Feedback Output at VCO/12

Note:
2. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Description

The CY29962 has an integrated PLL that provides low skew and low jitter clock outputs for high-performance microprocessors. Three independent banks of seven outputs as well as an independent PLL feedback output, FB_OUT, provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 400 MHz. This allows a wide range of output frequencies up to 150 MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by FB_SEL select inputs (see *Table 1*). The VCO frequency is then divided down to provide the required output frequencies.

Zero Delay Buffer

When used as a zero delay buffer, the CY29962 will likely be in a nested clock tree application. For these applications the CY29962 offers a low-voltage PECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The CY29962 can then lock onto the LVPECL reference and translate with near zero delay to low-skew outputs.

By using one of the outputs as a feedback to the PLL, the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge, thus producing a near-zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock, the Tpd of the CY29962 is a function of the configuration used.

Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: .... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: .... V_{DD} + 0.3V

Storage Temperature: .... –65°C to + 150°C

Operating Temperature: .... –40°C to +85°C

Maximum ESD protection .... 2 kV

Maximum Power Supply: 5.5V

Maximum Input Current: .... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

V_{SS} < (V_{IN} or V_{OUT}) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

Table 3. DC Parameters V_{DD} = 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}[3]	Input LOW Voltage		V_{SS}		0.7	V
V_{IH}[3]	Input HIGH Voltage		1.7		V_{DD}	V
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		500		1000	mV
V_{CMR}[4]	Common Mode Range PECL_CLK		V_{DD} – 1.4		V_{DD} – 0.6	V
I_{IL}[5]	Input LOW Current (@ V_{IL} = V_{SS})				–120	µA
I_{IH}[5]	Input HIGH Current (@ V_{IH} = V_{DD})				120	µA
V_{OL}[6]	Output LOW Voltage	I_{OL} = 15 mA			0.6	V
V_{OH}[6]	Output HIGH Voltage	I_{OH} = –15 mA	1.8			V
I_{DD}	Quiescent Supply Current	V_{DD} and AV_{DD}		10	13	mA
C_{IN}	Input Pin Capacitance			4		pF

Table 4. DC Parameters V_{DD} = 3.3V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}[3]	Input LOW Voltage		V_{SS}		0.8	V
V^{IH}[3]	Input HIGH Voltage		2.0		V_{DD}	V
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		500		1000	mV
V_{CMR}[4]	Common Mode Range PECL_CLK		V_{DD} – 1.4		V_{DD} – 0.6	V
I_{IL}[5]	Input LOW Current (@ V_{IL} = V_{SS})				–120	µA
I_{IH}[5]	Input HIGH Current (@ V_{IH} = V_{DD})				120	µA
V_{OL}[6]	Output LOW Voltage	I_{OL} = 24mA			0.55	V
V_{OH}[6]	Output HIGH Voltage	I_{OH} = –24mA	2.4			V
I_{DD}	Quiescent Supply Current	V_{DD} and AV_{DD}		15	20	mA
C_{IN}	Input Pin Capacitance			4		pF

Notes:
3. The LVCMOS inputs threshold is at 30% of V_{DD}.
4. The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the HIGH input is within the VCMR range and the input lies within the V_{PP} specification.
5. Inputs have pull-up/pull-down resistors that affect input current.
6. Driving series or parallel terminated 50Ω (or 50Ω to V_{DD}/2) transmission lines.

Table 5. AC Parameters V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C[7]

| Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fref	Reference Input Frequency	FB_SEL = 1	16		33	MHz
		FB_SEL = 0	25		50	
FrefDC	Reference Input Duty Cycle		25		75	%
Fvco	PLL VCO Lock Range		200		400	MHz
Tlock	Maximum PLL lock Time				10	ms
Tr / Tf	Output Clocks Rise/Fall Time[8,9]	0.55V to 2.0V, V_{DD} = 3.3V	0.1		1.0	ns
		0.5V to 1.8V, V_{DD}=2.5V				
Fout	Maximum Output Frequency	Q (÷2)	100		150	MHz
		Q (÷4)	50		100	
FoutDC	Output Duty Cycle[8,9]		45	50	55	%
tpZL, tpZH	Output Enable Time[8] (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time[8] (all outputs)		2		8	ns
TCCJ	Cycle-to-Cycle Jitter[8,9]			±100		ps
Tskew	Any Output to Any Output Skew[8,9]	Same Frequency			150	ps
		Different Frequency			300	
Tskew	Bank to Bank Skew	Banks at different voltages			400	ps
Tskew(pp)	Part to Part Skew[10]				450	ps
Tpd	Phase Error[8,9]	TCLK or PECL_CLK to FB_IN	VDD = 3.3V	0	100	200	ps
		VDD = 2.5V	25	125	225	

Notes:
7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. Outputs loaded with 30 pF each.
9. 50Ω transmission line terminated into $V_{DD}/2$
10. Part-to-part skew at a given temperature and voltage.
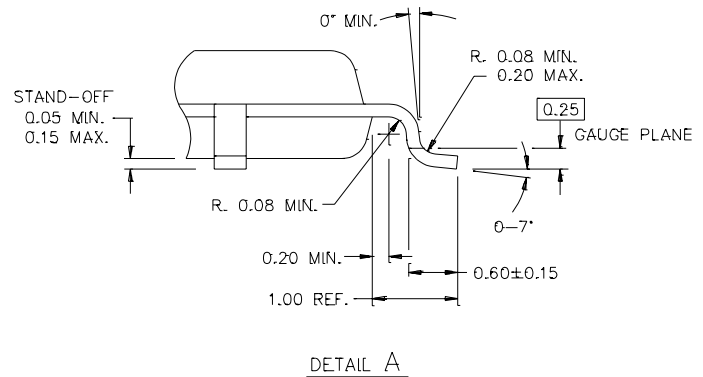
Ordering Information

Part Number	Package Type	Production Flow
CY29962AI	48-pin TQFP	Industrial, –40°C to +85°C

Package Drawing and Dimensions

48-lead Thin Plastic Quad Flat Pack (7 × 7 × 1.4 mm) A48
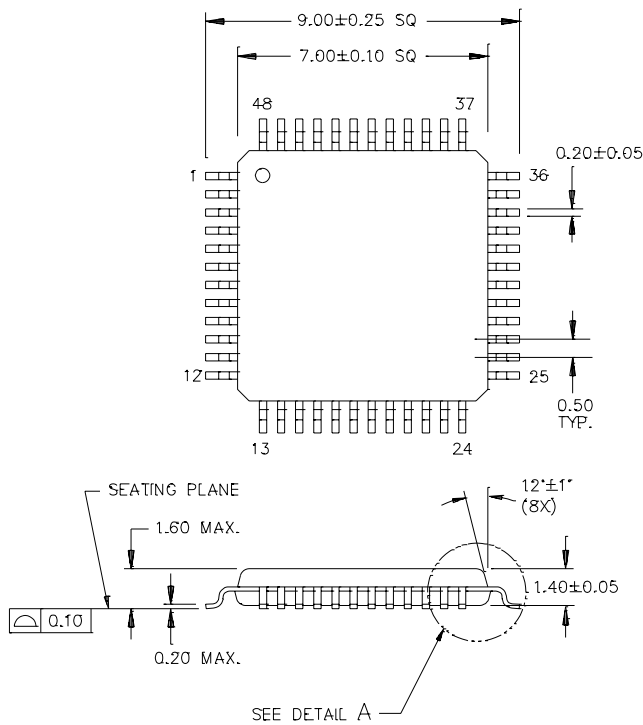
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