CY29949

2.5V or 3.3V, 200-MHz, 1:15 Clock Distribution Buffer

Features

- **2.5V or 3.3V Operation**
- **200-MHz Clock Support**
- **LVPECL or LVCMOS/LVTTL Clock Input**
- **LVCMOS/LVTTL Compatible Inputs**
- **15 Clock Outputs: Drive up to 30 Clock Lines**
- **1X and 1/2X Configurable Outputs**
- **Output Three-state Control**
- **350 ps max. Output-to-Output Skew**
- **Pin Compatible with MPC949**
- **Industrial Temp. Range: –40°C to +85°C**
- **52-Pin TQFP Package**

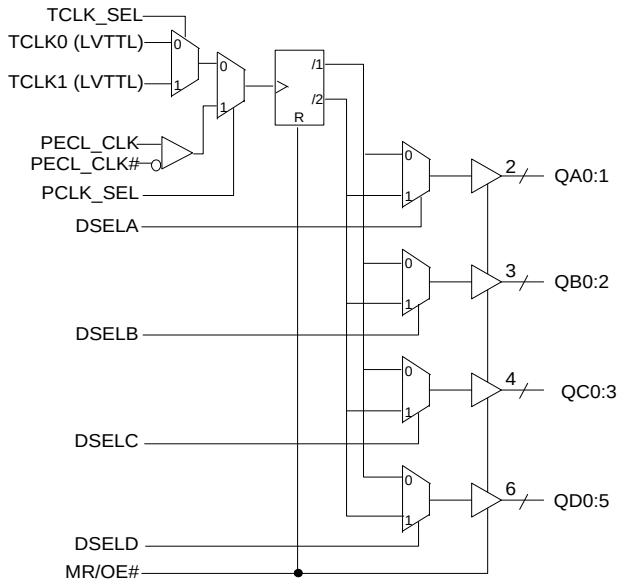
Description

The CY29949 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 15 outputs are LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the CY29949 has an effective fan-out of 1:30.

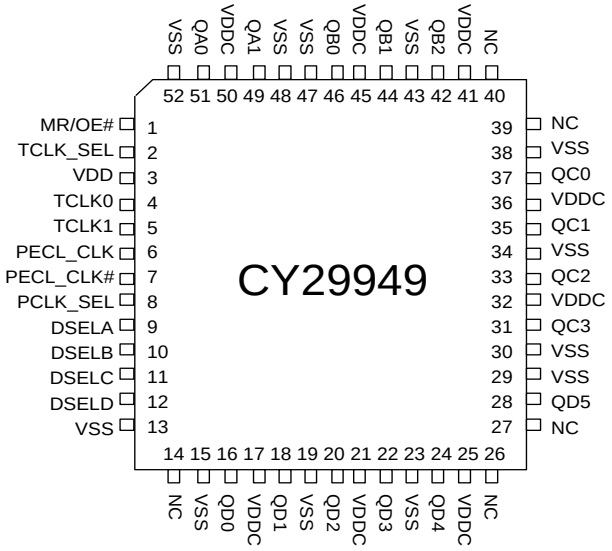
The CY29949 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:D) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The CY29949 outputs can also be three-stated via the MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
6	PECL_CLK		I, PD	PECL Input Clock
7	PECL_CLK#		I, PU	PECL Input Clock
4, 5	TCLK(0,1)		I, PU	External Reference/Test Clock Input
49, 51	QA(1,0)	VDDC	O	Clock Outputs
42, 44, 46	QB(2:0)	VDDC	O	Clock Outputs
31, 33, 35, 37	QC(3:0)	VDDC	O	Clock Outputs
16, 18, 20, 22, 24, 28	QD(5:0)	VDDC	O	Clock Outputs
9, 10, 11, 12	DSEL(A:D)		I, PD	Divider Select Inputs. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
2	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
8	PCLK_SEL		I, PD	PECL Select Input. When HIGH, PECL clock is selected and when LOW TCLK(0,1) is selected
1	MR_OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated.
17, 21, 25, 32, 36, 41, 45, 50	VDDC			2.5V or 3.3V Power Supply for Output Clock Buffers
3	VDD			2.5V or 3.3V Power Supply
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	VSS			Common Ground
14, 26, 27, 39, 40,	NC			Not Connected

Note:
1. PD = Internal Pull-Down, PU = Internal Pull- UP

Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: ..... –65°C to + 150°C
Operating Temperature: ..... –40°C to +85°C
Maximum ESD protection 2kV
Maximum Power Supply: 5.5V
Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	V_{DD} = 3.3V, PECL_CLK single ended	1.49		1.825	V
		V_{DD} = 2.5V, PECL_CLK single ended	1.10		1.45	
		All other inputs	V_{SS}		0.8	
V_{IH}	Input High Voltage	V_{DD} = 3.3V, PECL_CLK single ended	2.135		2.42	V
		V_{DD} = 2.5V, PECL_CLK single ended	1.75		2.0	
		All other inputs	2.0		V_{DD}	
I_{IL}	Input Low Current[2]				–100	µA
I_{IH}	Input High Current[2]				100	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		300		1000	mV
V_{CMR}	Common Mode Range[3] PECL_CLK	V_{DD} = 3.3V	V_{DD} – 2.0		V_{DD} – 0.6	V
		V_{DD} = 2.5V	V_{DD} – 1.2		V_{DD} – 0.6	
V_{OL}	Output Low Voltage[4]	I_{OL} = 20 mA			0.4	V
V_{OH}	Output High Voltage[4]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5			V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF		200		mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF		330		
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF		140		
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF		235		
C_{in}	Input Capacitance			4		pF

Notes:
2. Inputs have pull-up/pull-down resistors that effect input current.
3. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
4. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters[5]: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[6]	V_{DD} = 3.3V			200	MHz
		V_{DD} = 2.5V			170	
Tpd	PECL_CLK to Q Delay[6]	V_{DD} = 3.3V	4.0		8.6	ns
	TCLK to Q Delay[6]		4.2		10.5	
	PECL_CLK to Q Delay[6]	V_{DD} = 2.5V	6.0		10.6	
	TCLK to Q Delay[6]		6.2		10.5	
FoutDC	Output Duty Cycle[6,7]	Measured at VDD/2	TCYCLE/2 – 1		TCYCLE/2 + 1	ns
tpZL, tpZH	Output Enable Time (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[6,8]			250	350	ps
Tskew(pp)	Part-to-Part Skew[9]	PECL_CLK to Q		1.5	2.75	ns
		TCLK to Q		2.0	4.0	
Tr/Tf	Output Clocks Rise/Fall Time[8]	0.8V to 2.0V, V_{DD} = 3.3V	0.10		1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.10		1.3	

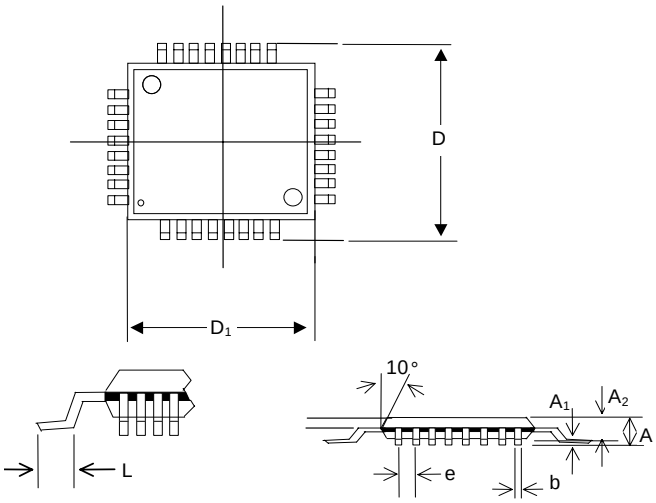
Notes:

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. 50% input duty cycle.
8. Outputs loaded with 30 pF each.
9. Part-to-Part skew at a given temperature and voltage.

Ordering Information

Part Number	Package Type	Production Flow
CY29949AI	52 Pin TQFP	Industrial, -40°C to +85°C

Package Drawing and Dimensions



52 Pin TQFP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.0472	-	-	12.00	-
D1		0.394	-	-	10.00	-
b	0.009	-	0.015	0.22	-	0.38
e	0.026 BSC			0.65 BSC		
L	0.018	-	0.030	0.45	-	0.75

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111100	02/01/02	BRK	New data sheet