CY29947

2.5V or 3.3V, 200-MHz, 1:9 Clock Distribution Buffer

Features

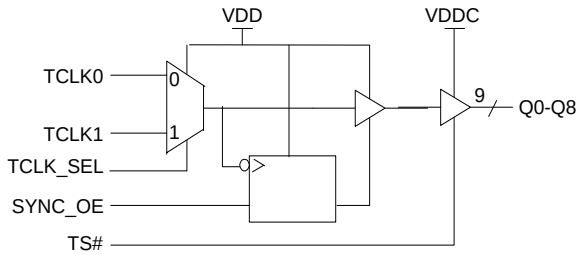
- **2.5V or 3.3V Operation**
- **200-MHz Clock Support**
- **LVCMOS/LVTTL Compatible Inputs**
- **9 Clock Outputs: Drive up to 18 Clock Lines**
- **Synchronous Output Enable**
- **Output Three-state Control**
- **250 ps max. Output to Output Skew**
- **Pin Compatible with MPC947**
- **Industrial Temp. Range: –40°C to +85°C**
- **32-pin TQFP package**

Description

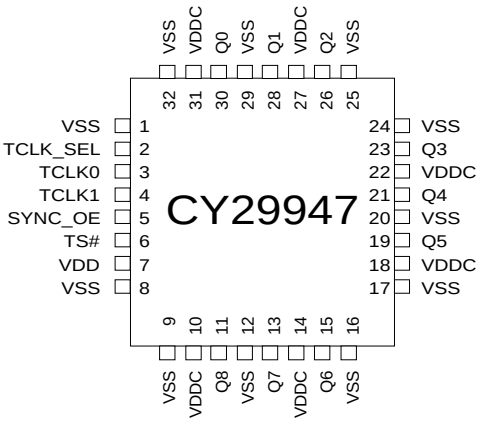
The CY29947 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible clock inputs. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The 9 outputs are LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the CY29947 has an effective fan-out of 1:18. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the CY29947 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The CY29947 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
3	TCLK0		I, PU	Test Clock Input
4	TCLK1		I, PU	Test Clock Input
2	TCLK_SEL		I, PU	Test Clock Select Input. When LOW, TCLK0 is selected. When asserted HIGH, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q(8:0)	VDDC	O	Clock Outputs
5	SYNC_OE		I, PU	Output Enable Input. When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	Three-state Control Input. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 27, 31	VDDC			3.3V or 2.5V Power Supply for Output Clock Buffers
7	VDD			3.3V or 2.5V Power Supply
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	VSS			Common Ground

Note:
1. PD = Internal Pull-Down, PU = Internal Pull- UP

Output Enable/ Disable

The CY29947 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in *Figure 1*.

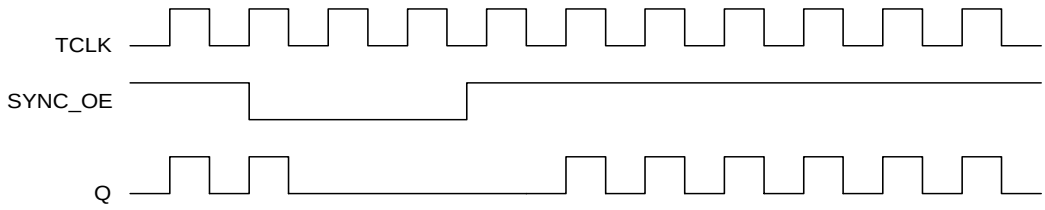


Figure 1. SYNC_OE Timing Diagram

Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... –40°C to +85°C

Maximum ESD protection 2kV

Maximum Power Supply: 5.5V

Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[2]				–100	µA
I_{IH}	Input High Current[2]				10	µA
V_{OL}	Output Low Voltage[3]	I_{OL} = 20 mA			0.4	V
V_{OH}	Output High Voltage[3]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5			V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF		120		mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF		200		
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF		85		
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF		140		
C_{in}	Input Capacitance			4		pF

Notes:

2. Inputs have pull-up/pull-down resistors that effect input current.
3. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters[4]: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[5]	V_{DD} = 3.3V			200	MHz
		V_{DD} = 2.5V			170	
Tpd	TCLK To Q Delay[5]	V_{DD} = 3.3V	4.75		9.25	ns
		V_{DD} = 2.5V	6.50		10.50	
FoutDC	Output Duty Cycle[5,6]	Measured at $V_{DD}/2$	TCYCLE/2 – 800		TCYCLE/2 + 800	ns
tpZL, tpZH	Output Enable Time (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[5,8]			150	250	ps
Tskew(pp)	Part-to-Part Skew[9]				2.0	ns
Ts	Setup Time[5,7]	SYNC_OE to TCLK	0.0			ps
Th	Hold Time[5,7]	TCLK to SYNC_OE	1.0			ps
Tr/Tf	Output Clocks Rise/Fall Time[8]	0.8V to 2.0V, V_{DD} = 3.3V	0.20		1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.20		1.3	

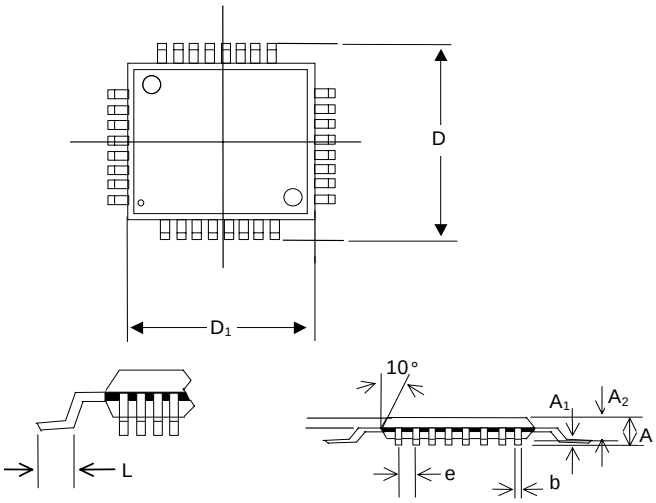
Notes:

4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
5. Outputs driving 50Ω transmission lines.
6. 50% input duty cycle.
7. Setup and hold times are relative to the falling edge of the input clock
8. Outputs loaded with 30 pF each.
9. Part-to-Part skew at a given temperature and voltage.

Ordering Information

Part Number	Package Type	Production Flow
CY29947AI	32 Pin TQFP	Industrial, –40°C to +85°C

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80BSC		
L	0.018	-	0.030	0.45	-	0.75

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111098	02/07/02	BRK	New data sheet