CY29946

2.5V or 3.3V, 200-MHz, 1:10 Clock Distribution Buffer

Features

- **2.5V or 3.3V Operation**
- **200-MHz Clock Support**
- **LVCMOS/LVTTL Compatible Inputs**
- **10 Clock Outputs: Drive up to 20 Clock Lines**
- **1X or 1/2X Configurable Outputs**
- **Output Three-state Control**
- **250 ps max. Output to Output Skew**
- **Pin Compatible with MPC946**
- **Industrial Temp. Range: –40°C to +85°C**
- **32-Pin TQFP Package**

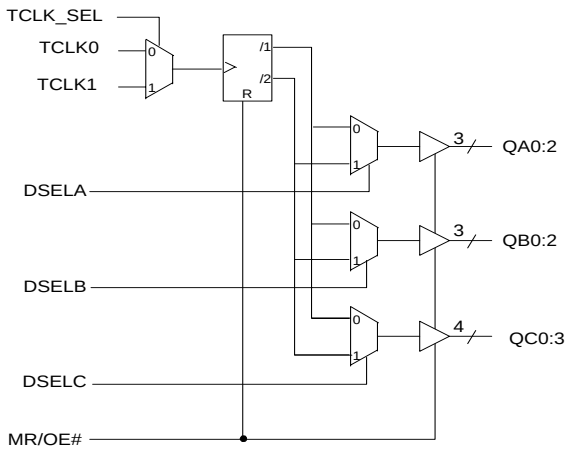
Description

The CY29946 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 10 outputs are LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the CY29946 has an effective fan-out of 1:20.

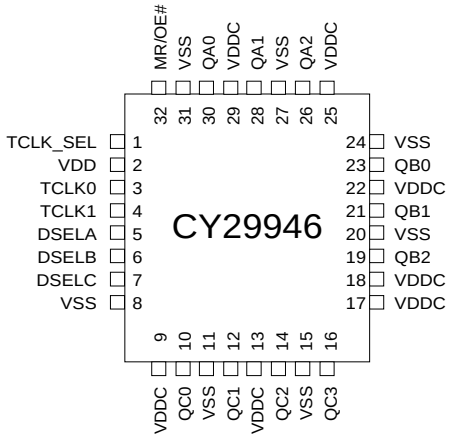
The CY29946 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The CY29946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	Divider Select Inputs. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated.
9, 13, 17, 18, 22, 25, 29	VDDC			2.5V or 3.3V Power Supply for Output Clock Buffers
2	VDD			2.5V or 3.3V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

Note:
1. PD = Internal Pull-Down, PU = Internal Pull- UP

Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... –40°C to +85°C

Maximum ESD protection 2kV

Maximum Power Supply: 5.5V

Maximum Input Current: ..... ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[2]				–100	µA
I_{IH}	Input High Current[2]				100	µA
V_{OL}	Output Low Voltage[3]	I_{OL} = 20 mA			0.4	V
V_{OH}	Output High Voltage[3]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5			V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF		130		mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF		225		
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF		95		
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF		160		
C_{in}	Input Capacitance			4		pF

Notes:

2. Inputs have pull-up/pull-down resistors that effect input current.
3. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters[4]: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[5]	V_{DD} = 3.3V			200	MHz
		V_{DD} = 2.5V			170	
Tpd	TTL_CLK To Q Delay[5]		5.0		11.5	ns
FoutDC	Output Duty Cycle[5,6]	Measured at $V_{DD}/2$	TCYCLE/2-1		TCYCLE/2+1	ns
tpZL, tpZH	Output enable time (all outputs)		2		10	ns
tpLZ, tpHZ	Output disable time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[5,7]			150	250	ps
Tskew(pp)	Part-to-Part Skew[8]			2.0	4.5	ns
Tr/Tf	Output Clocks Rise / Fall Time[7]	0.8V to 2.0V, V_{DD} = 3.3V	0.10		1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.10		1.3	

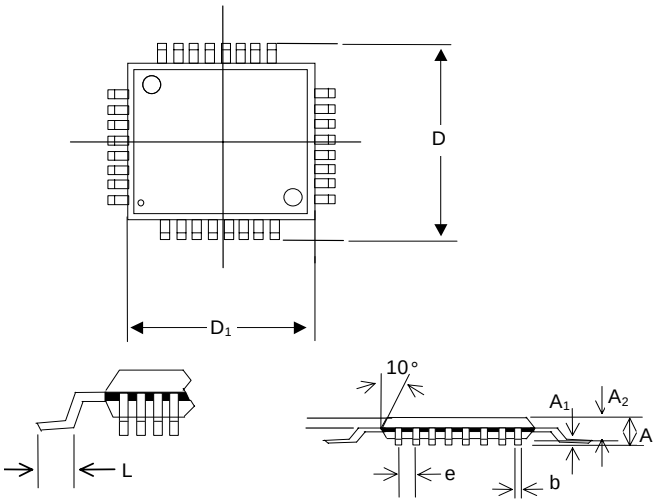
Notes:

4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
5. Outputs driving 50Ω transmission lines.
6. 50% input duty cycle.
7. Outputs loaded with 30 pF each.
8. Part-to-Part skew at a given temperature and voltage.

Ordering Information

Part Number	Package Type	Production Flow
CY29946AI	32 Pin TQFP	Industrial, -40°C to +85°C

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80BSC		
L	0.018	-	0.030	0.45	-	0.75

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111097	02/07/02	BRK	New data sheet