CY29943

2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer

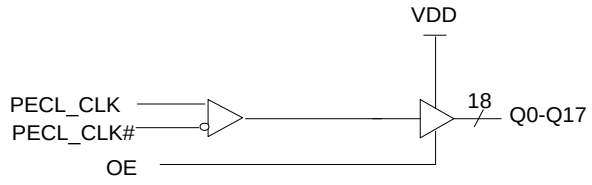
Features

- **200-MHz Clock Support**
- **2.5V or 3.3V Operation**
- **LVPECL Clock Input**
- **LVCMOS/LVTTL Compatible Inputs**
- **18 Clock Outputs: Drive up to 36 Clock Lines**
- **200 ps max. Output to Output Skew**
- **Output Enable Control**
- **Pin Compatible with MPC942P**
- **Industrial Temperature Range: –40°C to +85°C**
- **32-Pin LQFP Package**

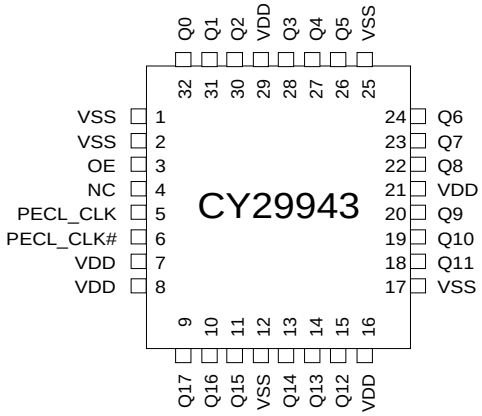
Description

The CY29943 is a low-voltage 200-MHz clock distribution buffer with an LVCMOS or LVTTL compatible input clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the CY29943 has an effective fan-out of 1:36. Low output-to-output skews make the CY29943 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
5	PECL_CLK		I, PU	PECL Input Clock
6	PECL_CLK#		I, PD	PECL Input Clock
3	OE		I, PU	Output Enable. When HIGH, all the outputs are enabled. When set LOW, the outputs are at high impedance.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDD	O	Clock Outputs
7, 8, 16, 21, 29	VDD			3.3V or 2.5V Power Supply
1, 2, 12, 17, 25	VSS			Common Ground
4	NC			No Connection

Note:
1. PD = Internal Pull-Down, PU = Internal Pull- UP

Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... –40°C to +85°C

Maximum ESD protection 2kV

Maximum Power Supply: 5.5V

Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDC} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[2]				–200	µA
I_{IH}	Input High Current[2]				200	µA
V_{PP}	Peak-to-Peak Input Voltage		500		1000	mV
VCMR	Common Mode Range[3] PECL_CLK	V_{DD} = 3.3V	V_{DD} – 1.4		V_{DD} – 0.6	V
		V_{DD} = 2.5V	V_{DD} – 1.0		V_{DD} – 0.6	
V_{OL}	Output Low Voltage[4]	I_{OL} = 20 mA			0.5	V
V_{OH}	Output High Voltage[4]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.4			V
		I_{OH} = –16 mA, V_{DD} = 2.5V	2.0			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 150 MHz, CL = 15 pF		285		mA
		V_{DD} = 3.3V, Outputs @ 200 MHz, CL = 15 pF		335		
		V_{DD} = 2.5V, Outputs @ 150 MHz, CL = 15 pF		200		
		V_{DD} = 2.5V, Outputs @ 200 MHz, CL = 15 pF		240		
Z_{out}	Output Impedance			12		W
C_{in}	Input Capacitance			4		pF

Notes:

2. Inputs have pull-up/pull-down resistors that effect input current.
3. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the VPP specification.
4. Driving series or parallel terminated 50Ω (or 50Ω to V_{DD}/2) transmission lines.

AC Parameters[5]**:** V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDC} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency				200	MHz
Tpd	PECL_CLK to Q Delay[6,8]	V_{DD} = 3.3V	2.0	3.5	4.0	ns
		V_{DD} = 2.5V	2.6	4.0	5.2	
FoutDC	Output Duty Cycle[6,7,8]	Measured at V_{DD}/2	45		55	%
Tskew	Output-to-Output Skew[6,8]				200	ps
Tskew(pp)	Part-to-Part Skew[9]	V_{DD} = 3.3V			1.7	ns
		V_{DD} = 2.5V			2.2	
Tskew(pp)	Part-to-Part Skew[10]				1.0	ns
Tr/Tf	Output Clocks Rise / Fall Time[6,8]	0.8V to 2.0V, V_{DD} = 3.3V	0.2		1.0	ns
		0.5V to 1.8V, V_{DD} = 2.5V				

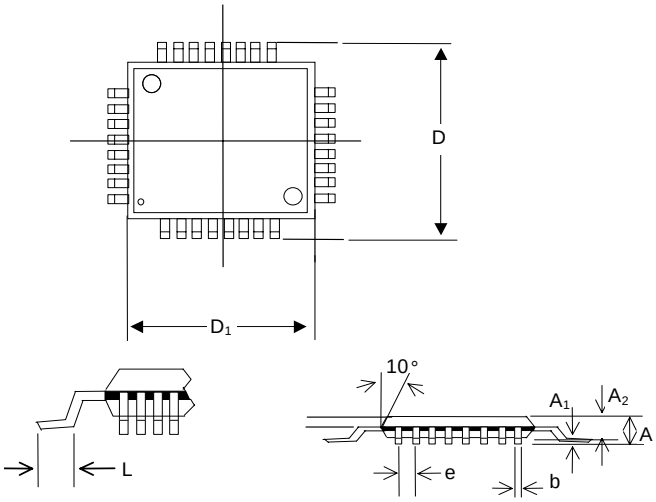
Notes:

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. 50% input duty cycle.
8. Outputs loaded with 15 pF each.
9. Across temperature and voltage ranges, includes output skew.
10. For a specific temperature and voltage, includes output skew

Ordering Information

Part Number	Package Type	Production Flow
CY29943AI	32 Pin LQFP	Industrial, -40°C to +85°C

Package Drawing and Dimensions



32 Pin LQFP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	-	0.057	1.35	-	1.45
D	-	0.354	-	-	9.00	-
D1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

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Revision History

Document Title: CY29943 2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer Document Number: 38-07285				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111096	02/07/02	BRK	New data sheet