



CYPRESS

2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer

CY29942

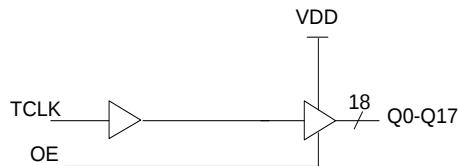
Features

- 200-MHz Clock Support
- 2.5V or 3.3V Operation
- LVC MOS/LVTTL Clock Input
- LVC MOS/LVTTL Compatible Inputs
- 18 Clock Outputs: Drive up to 36 Clock Lines
- 200 ps max. Output to Output Skew
- Output Enable Control
- Pin Compatible with MPC942C
- Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$
- 32-Pin LQFP Package

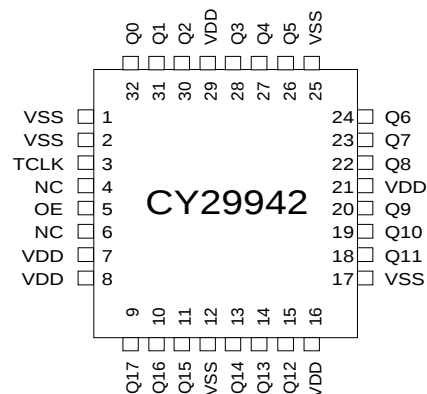
Description

The CY29942 is a low-voltage 200-MHz clock distribution buffer with an LVC MOS or LVTTL compatible input clock. All other control inputs are LVC MOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V LVC MOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the CY29942 has an effective fan-out of 1:36. Low output-to-output skews make the CY29942 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram



Pin Configuration



Pin Description^[1]

Pin	Name	PWR	I/O	Description
3	TCLK		I, PD	External Reference/Test Clock Input
5	OE		I, PU	Output Enable. When high, all the outputs are enabled. When set low, the outputs are at high impedance.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDD	O	Clock Outputs
7, 8, 16, 21, 29	VDD			3.3V or 2.5V Power Supply
1, 2, 12, 17, 25	VSS			Common Ground
4, 6	NC			No Connection

Note:

1. PD = Internal Pull-Down, PU = Internal Pull- UP

Maximum Ratings

Maximum Input Voltage Relative to V_{SS} : $V_{SS} - 0.3V$
 Maximum Input Voltage Relative to V_{DD} : $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum ESD protection 2kV
 Maximum Power Supply: 5.5V
 Maximum Input Current: ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{DDC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current ^[2]				-200	μA
I_{IH}	Input High Current ^[2]				200	μA
V_{OL}	Output Low Voltage ^[3]	$I_{OL} = 20$ mA			0.5	V
V_{OH}	Output High Voltage ^[3]	$I_{OH} = -20$ mA, $V_{DDC} = 3.3V$	2.4			V
		$I_{OH} = -16$ mA, $V_{DDC} = 2.5V$	2.0			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	$V_{DD} = 3.3V$, Outputs @ 150 MHz, $CL = 15$ pF		285		mA
		$V_{DD} = 3.3V$, Outputs @ 200 MHz, $CL = 15$ pF		335		
		$V_{DD} = 2.5V$, Outputs @ 150 MHz, $CL = 15$ pF		200		
		$V_{DD} = 2.5V$, Outputs @ 200 MHz, $CL = 15$ pF		240		
Z_{out}	Output Impedance			12		W
C_{in}	Input Capacitance			4		pF

Notes:

- Inputs have pull-up/pull-down resistors that effect input current.
- Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.

AC Parameters^[4]: $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{DDC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency				200	MHz
Tpd	TTL_CLK to Q Delay ^[5,7]	$V_{DD} = 3.3V$	1.8	3.3	3.8	ns
		$V_{DD} = 2.5V$	2.3	3.8	4.4	
FoutDC	Output Duty Cycle ^[5,6,7]	Measured at $V_{DD}/2$	45		55	%
Tskew	Output-to-Output Skew ^[5,7]				200	ps
Tskew(pp)	Part-to-Part Skew ^[8]	$V_{DD} = 3.3V$			1.0	ns
		$V_{DD} = 2.5V$			1.3	
Tskew(pp)	Part to Part Skew ^[9]				600	ps
Tr/Tf	Output Clocks Rise / Fall Time ^[5,7]	0.8V to 2.0V, $V_{DD} = 3.3V$	0.2		1.0	ns
		0.5V to 1.8V, $V_{DD} = 2.5V$				

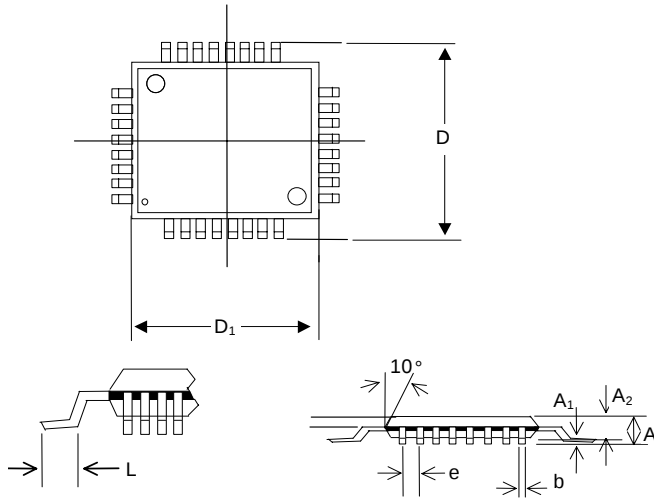
Notes:

4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
5. Outputs driving 50Ω transmission lines.
6. 50% input duty cycle.
7. Outputs loaded with 15 pF each.
8. Across temperature and voltage ranges, includes output skew.
9. For a specific temperature and voltage, includes output skew

Ordering Information

Part Number	Package Type	Production Flow
CY29942AI	32 Pin LQFP	Industrial, -40°C to +85°C

Package Drawing and Dimensions



32 Pin LQFP Outline Dimensions

Symbol	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	-	0.057	1.35	-	1.45
D	-	0.354	-	-	9.00	-
D1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

Revision History

Document Title: CY29942 2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer Document Number: 38-07284				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111095	02/07/02	BRK	New data sheet