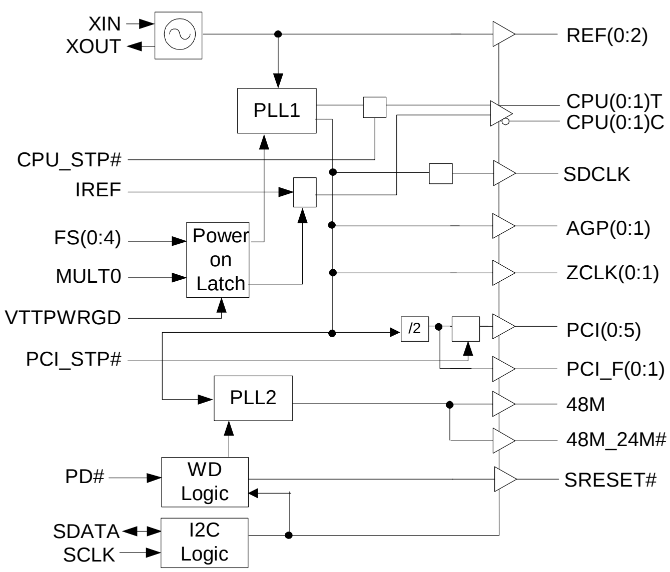
High-performance SiS645/650 Pentium® Four-clock Synthesizer

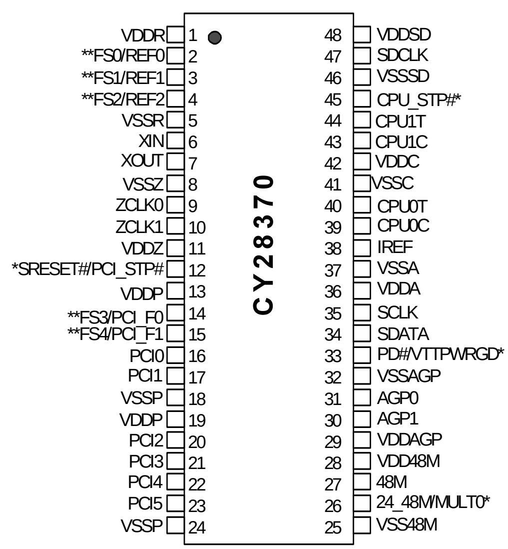
Features

- Supports Pentium® 4-type CPUs
- 3.3V power supply
- Eight copies of PCI clocks
- One 48-MHz USB clock
- Two copies of ZCLK clocks
- One 48-MHz/24-MHz programmable SIO clock
- Two differential CPU clock pairs
- SMBus Support with readback capabilities
- Spread Spectrum EMI reduction
- Dial-a-Frequency™ features
- Dial-a-Ratio™ features
- Dial-a-DB™ features
- 48-pin SSOP package
- Watchdog function

Block Diagram



Pin Configuration[1]



48 pin SSOP

Note:

1. Pins marked with [*] have internal pull-up resistors. Pins marked with [**] have internal pull-down resistors.

Table 1. Frequency Table

FS(4:0)	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGP (MHz	PCI (MHz)	VCO (MHz)
00000	66.67	66.67	66.67	66.67	33.33	400.00
00001	100.00	133.33	66.67	66.67	33.33	400.00
00010	111.11	166.67	66.67	66.67	33.33	666.66
00011	100.00	200.00	66.67	66.67	33.33	400.00
00100	100.00	100.00	133.33	66.67	33.33	400.00
00101	133.90	133.90	133.90	66.95	33.48	669.50
00110	133.33	166.67	133.33	66.67	33.33	666.66
00111	133.33	200.00	133.33	66.67	33.33	400.00
01000	100.00	166.67	125.00	62.50	31.25	500.00
01001	100.00	133.33	133.33	66.67	33.33	400.00
01010	111.11	166.67	133.33	66.67	33.33	666.66
01011	100.00	200.00	133.33	66.67	33.33	400.00
01100	100.60	134.13	100.60	67.07	33.53	402.40
01101	133.33	133.33	100.00	66.67	33.33	400.00
01110	100.00	166.67	100.00	71.43	35.71	500.00
01111	133.33	166.67	111.11	66.67	33.33	666.66
10000	125.00	125.00	100.00	71.43	35.71	500.00
10001	150.00	150.00	120.00	66.67	33.33	600.00
10010	140.00	140.00	140.00	70.00	35.00	560.00
10011	166.67	166.67	133.33	66.67	33.33	666.66
10100	100.00	100.00	66.67	66.67	33.33	400.00
10101	133.33	133.33	95.24	66.67	33.33	666.66
10110	133.33	166.67	95.24	66.67	33.33	666.66
10111	133.33	200.00	100.00	66.67	33.33	400.00
11000	111.11	133.33	133.33	66.67	33.33	666.66
11001	125.00	166.67	166.67	62.50	31.25	500.00
11010	105.00	140.00	140.00	60.00	30.00	420.00
11011	120.00	150.00	150.00	66.67	33.33	600.00
11100	133.33	133.33	133.33	57.14	28.57	400.00
11101	100.00	133.33	133.33	50.00	25.00	400.00
11110	180.00	135.00	135.00	60.00	30.00	540.00
11111	160.00	213.33	128.00	64.00	32.00	640.00

Pin Description [2]

Pin	Name	PWR	I/O	Description
6	XIN		I	**Oscillator Buffer Input**. Connect to a crystal or to an external clock.
7	XOUT	VDDR	O	**Oscillator Buffer Output**. Connect to a crystal. Do not connect when an external clock is applied at XIN.
40,44	CPU(0:1)T	VDDC	O	“**True” host output clocks**. See *Table 1* on page 2 for frequencies and functionality.
39,43	CPU(0:1)C	VDDC	O	“**Complementary” host output clocks**. See *Table 1* on page 2 for frequencies and functionality.
16,17,20,23	PCI (0:5)	VDDP	O	**PCI Clock Outputs**. See *Table 1* on page 2.
14	FS3/PCI_F0	VDDP	I/O PD	**Power-on bidirectional input/output**. At power-up, FS3 is the input. When VTTPWRGD transitions to a logic HIGH, FS3 state is latched and this pin becomes PCI_F0 Clock Output. See *Table 1* on page 2.
15	FS4/PCI_F1	VDDP	I/O PD	**Power-on bidirectional input/output**. At power-up, FS4 is the input. When VTTPWRGD transitions to a logic HIGH, FS4 state is latched and this pin becomes PCI_F1 Clock Output. See *Table 1* on page 2.
2	FS0/REF0	VDDR	I/O PD	**Power-on bidirectional input/output**. At power-up, FS0 is the input. When VTTPWRGD transitions to a logic HIGH, FS0 state is latched and this pin becomes REF0, buffered Output copy of the device’s XIN clock.
3	FS1/REF1	VDDR	I/O PD	**Power-on bidirectional input/output**. At power-up, FS1 is the input. When VTTPWRGD is transited to logic LOW, FS1 state is latched and this pin becomes REF1, buffered Output copy of the device’s XIN clock.
4	FS2/REF2	VDDR	I/O PD	**Power-on bidirectional input/output**. At power-up, FS2 is the input. When VTTPWRGD is transited to logic LOW, FS2 state is latched and this pin becomes REF2, buffered Output copy of the device’s XIN clock.
38	IREF		I	**Current reference programming input for CPU buffers**. A resistor is connected between this pin and VSS. See *Figure 1*.
33	PD#/VTTPRGD		I PU	**Power-down Input/VTT Power Good Input**. At power-up, VTTPWRGD is the input. When this input is transitions initially from LOW to HIGH, the FS (0:4) and MULT0 are latched. After the first LOW-to-HIGH transition, this pin become a PD# input with an internal pull-up. When PD# is asserted LOW, the device enters power-down mode. See power management function.
27	48M	VDD48M	O	Fixed 48-MHz USB Clock Output
26	24_48M/MULT0	VDD48M	I/O PU	**Power-on bidirectional input/output**. At power-up, MULT0 is the input. When VTTPWRGD is transited to logic LOW, MULT0 state is latched and this pin becomes 24_48M, SIO programmable clock output.
9,10	ZCLK (0:1)	VDDZ	O	**HyperZip Clock Outputs**. See *Table 1* on page 2.
34	SDATA		I/O	**Serial Data Input**. Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
35	SCLK		I	**Serial Clock Input**. Conforms to the SMBus specification.
12	SRESET#		O	**PCI Clock Disable Input**. If Byte12 Bit7 = 0, this pin becomes an SRESET# open drain output, and the internal pulled up is not active. See system reset description.
	PCI_STP#		I PU	**System Reset Control Output**. If Byte12 Bit7 = 1 (Default), this pin becomes PCI Clock Disable Input. When PCI_STP# is asserted low, PCI (0:5) clocks are synchronously disabled in a low state. This pin does not affect PCI_F (0:1) if they are programmed to be Free-running clocks via the device’s SMBus interface.
45	CPU_STP#		I PU	**CPU Clock Disable Input**. When asserted low, CPU (0:1)T clocks are synchronously disabled in a high state and CPU (0:1)C clocks are synchronously disabled in a low state.
47	SDCLK	VDDSD	O	**SDRAM Clock Output**.

Pin Description (continued)[2]

Pin	Name	PWR	I/O	Description

Note:

2. PU = internal pull-up. PD = internal pull-down. T = tri-level logic input with valid logic voltages of LOW = < 0.8V, T = 1.0–1.8V and HIGH => 2.0V.

Pin Description (continued)[2]

Pin	Name	PWR	I/O	Description
30,31	AGP (0:1)	VDDAGP	O	**AGP clock outputs**. See *Table 1* on page 2 for frequencies and functionality.
48	VDDSD		PWR	**3.3V power supply for SDRAM clock outputs**
29	VDDAGP		PWR	**3.3V power supply for AGP clock outputs**
11	VDDZ		PWR	**3.3V power supply for HyperZip clock outputs**
1	VDDR		PWR	**3.3V power supply for REF clock outputs**
13,19	VDDP		PWR	**3.3V power supply for PCI clock outputs**
42	VDDC		PWR	**3.3V power supply for CPU clock outputs**
28	VDD48M		PWR	**3.3V power supply for 48-MHz/24-MHz clock outputs**
36	VDDA		PWR	**3.3V Analog power supply**
18,24	VSSP		PWR	**GND for PCI clock outputs**
41	VSSC		PWR	**GND for CPU clock outputs**
8	VSSZ		PWR	**GND for HyperZip clock outputs**
25	VSS48M		PWR	**GND for 48-MHz/24-MHz clock outputs**
5	VSSR		PWR	**GND for REF clock outputs**
46	VSSSD		PWR	**GND for SDRAM clock outputs**
32	VSSAGP		PWR	**GND for AGP clock outputs**
37	VSSA		PWR	**GND for Analog**

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled.

The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operations from the controller. For Block Write/Read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The Block Write and Block Read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding Byte Write and Byte Read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte read or Byte Write operation
(6:0)	Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be “0000000”

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8-bit “00000000” stands for block operation	11:18	Command Code – 8-bit “00000000” stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave

Table 3. Block Read and Block Write Protocol (continued)

20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Not acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits "1xxxxxxx" stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits "1xxxxxxx" stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not acknowledge
		39	Stop

Since SDR and DDR Zero Delay Buffers will share this same address this device starts from Byte 4.

Byte 4: CPU Clock Register

Bit	@Pup	Pin#	Name	Description
7	H/W Setting	14	FS3	For selecting frequencies in *Table 1*
6	H/W Setting	4	FS2	For selecting frequencies in *Table 1*
5	H/W Setting	3	FS1	For selecting frequencies in *Table 1*
4	H/W Setting	2	FS0	For selecting frequencies in*Table 1*
3	0			If this bit is programmed to a "1," it enables Writes to bits (7:4, 2) for selecting the frequency via software (SMBus). If this bit is programmed to a "0," it enables only Reads of bits (7:4, 2) that reflect the hardware setting of FS(0:4).
2	H/W Setting	15	FS4	For selecting frequencies in *Table 1*

Byte 4: CPU Clock Register (continued)

1	1		SSCG	Spread Spectrum Enable. 0 = Spread Off, 1 = Spread On. This is a Read and Write control bit.
0	0			Master Output Control. 0 = running, 1 = three-state all outputs

Byte 5: CPU Clock Register (All bits are Read-only)

Bit	@Pup	Pin#	Name	Description
7	0			Reserved
6	0			Reserved
5	X	26	MULT0	MULT0 (pin 26) Value. This bit is Read-only
4	X	15	FS4	FS4 read back. This bit is Read-only.
3	X	14	FS3	FS3 read back. This bit is Read-only.
2	X	4	FS2	FS2 read back. This bit is Read-only.
1	X	3	FS1	FS1 read back. This bit is Read-only.
0	X	2	FS0	FS0 read back. This bit is Read-only.

Byte 6: CPU Clock Register

Bit	@Pup	Pin#	Name	Description
7	0			Function Test Bit, always program to 0.
6	0			Reserved
5	0	14	PCI_F0	PCI_STP# control of PCI_F0. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
4	0	15	PCI_F1	PCI_STP# control of PCI_F1. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
3	1	40,39	CPU0T/C	Controls CPU0T and CPU0C functionality when CPU_STP# is asserted LOW 0 = Free Running, 1 + Stopped with CPU_STP# asserted LOW This is a Read and Write Control bit.
2	0	44,43	CPU1T/C	Controls CPU1T and CPU1C functionality when CPU_STP# is asserted LOW 0= Free Running, 1 Stopped with CPU_STP# asserted to LOW This and Read and Write Control bit.
1	1	40,39	CPU0T/C	CPU0T, CPU0C Output Control, 1= enabled, 0 = disabled. This is a Read and Write Control bit.
0	1	44,43	CPU1T/C	CPU1T, CPU1C Output Control, 1= enabled, 0 = disabled. This is a Read and Write Control bit.

Byte 7: PCI Clock Register

Bit	@Pup	Pin#	Name	Description
7	1	14	PCI_F0	PCI_F0 Output Control 1 = enabled, 0 = forced LOW
6	1	15	PCI_F1	PCI_F1 Output Control 1 = enabled, 0 = forced LOW
5	1	23	PCI5	PCI5 Output Control 1 = enabled, 0 = forced LOW
4	1	22	PCI4	PCI4 Output Control 1 = enabled, 0 = forced LOW
3	1	21	PCI3	PCI3 Output Control 1 = enabled, 0 = forced LOW
2	1	20	PCI2	PCI2 Output Control 1 = enabled, 0 = forced LOW
1	1	17	PCI1	PCI1 Output Control 1 = enabled, 0 = forced LOW
0	1	16	PCI0	PCI0 Output Control 1 = enabled, 0 = forced LOW

Byte 8: Silicon Signature Register

Bit	@Pup	Description
7	1	Vendor ID 1000 = Cypress
6	0	
5	0	
4	0	
3	0	Revision ID
2	0	
1	0	
0	0	

Byte 9: Peripheral Control Register

Bit	@Pup	Pin#	Name	Description
7	1	33	PD#	PD# Enable. 0 = enable, 1 = disable
6	0	39,40,43, 44	PD# output control	0 = when PD# is asserted LOW, CPU(0:1)T stop in a HIGH state, CPU(0:1)C stop in a LOW state. 1 = when PD# is asserted LOW, CPU(0:1)T and CPU(0:1)C stop in H-Z.
5	1	27	48M	48M Output Control 1 = enabled, 0 = forced LOW
4	1	26	48M_24M	48M_24M Output Control 1 = enabled, 0 = forced LOW
3	0	26	48M_24M	48M_24M, 0 = pin28 output is 24 MHz, 1 = pin28 output is 48 MHz.
2	0		SS2	SS2 Spread Spectrum control bit (0 = down spread, 1 = center spread)
1	0		SS1	SS1 Spread Spectrum control bit. See *Table 9*.
0	0		SS0	SS0 Spread Spectrum control bit. See *Table 9*.

Byte 10: Peripheral Control Register

Bit	@Pup	Pin#	Name	Description
7	1	47	SDCLK	SDCLK Output Enable 1 = enabled, 0 = disabled
6	1	4	REF2	REF2 Output Control 1 = enabled, 0 = forced LOW
5	1	3	REF1	REF1 Output Control 1 = enabled, 0 = forced LOW
4	1	2	REF0	REF0 Output Control 1 = enabled, 0 = forced LOW
3	1	10	ZCLK1	ZCLK1 Output Enable 1 = enabled, 0 = disabled
2	1	9	ZCLK0	ZCLK0 Output Enabled 1 = enabled, 0 = disabled
1	1	30	AGP1	AGP1 Output Enabled 1 = enabled, 0 = disabled
0	1	31	AGP0	AGP0 Output Enabled 1 = enabled, 0 = disabled

Byte 11: Dial-a-Skew™ and Dial-a-Ratio™ Control Register

Bit	@Pup	Name	Description
7	0	DARSD2	Programming these bits allows modifying the frequency ratio of the SDCLK clock relative to the VCO. See *Table 5*.
6	0	DARSD1	
5	0	DARSD0	
4	0	DARAG2	Programming these bits allows modifying the frequency ratio of the AGP(1:0), PCI(5:0) and PCIF(0:1) clocks relative to the VCO. See *Table 6*.
3	0	DARAG1	
2	0	DARAG0	
1	0	DASSD1	Programming these bits allows shifting skew between CPU and SDCLK signals. See *Table 7*.
0	0	DASSD0	

Table 5. Dial-a-Ratio SDCLK

DARSD(2:0)	VC0/SDCLK ratio
000	Frequency Selection Default
001	2

Table 5. Dial-a-Ratio SDCLK (continued)

010	3
011	4
100	5
101	6
110	8
111	9

Table 6. Dial-a-Ratio AGP(0:1)[3]

DARAG(2:0)	VC0/AGP ratio
000	Frequency Selection Default
001	6
010	7
011	8
100	9
101	10
110	10
111	10

Table 7. Dial-a-Skew SDCLK CPU

DASSD(1:0)	SDCLK-CPU Skew
00	0ps (Default)[4]
01	+150ps (CPU lag)*
10	+300ps (CPU lag)*
11	+450ps (CPU lag)*

Byte 12: Watchdog Time Stamp Register

Bit	@Pup	Name	Description
7	1		SRESET#/PCI_STP#. 1 = Pin 12 is the input pin as PCI_STP# signal. 0 = Pin 12 is the output pin as SRESET# signal.
6	0		Frequency Revert. This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only.0 = selects frequency of existing H/W setting1 = selects frequency of the second to last S/W setting. (the software setting prior to the one that caused a system reboot).
5	0		WDTEST. For WD-Test, ALWAYS program to ’0’
4	0		WD Alarm. This bit is set to “1” when the Watchdog times out. It is reset to “0” when the system clears the WD time stamps (WD3:0).
3	0	WD3	This bits selects the Watchdog Time Stamp Value. See *Table 8*.
2	0	WD2	
1	0	WD1	
0	0	WD0	

Notes:
3. The ratio of AGP to PCI is retained at 2:1.
4. See *Figure 1* for CPU measurement point. See *Figure 2* for SDCLK measurement point.

Table 8. Watchdog Time Stamp Table

WD(3:0)	Function
0000	Off
0001	1 second
0010	2 seconds
0011	3 seconds
0100	4 seconds
0101	5 seconds
0110	6 seconds
0111	7 seconds
1000	8 seconds
1001	9 seconds
1010	10 seconds
1011	11 seconds
1100	12 seconds
1101	13 seconds
1110	14 seconds
1111	15 seconds

Byte 13: Dial-a-Frequency™ Control Register N (All bits are read and write functional)[5]

Bit	@Pup	Description
7	0	Reserved
6	0	N6, MSB
5	0	N5
4	0	N4
3	0	N3
2	0	N2
1	0	N3
0	0	N0, LSB

Byte 14: Dial-a-Frequency Control Register R (All bits are read and write functional)[5]

Bit	@Pup	Description
7	0	Reserved
6	0	R5 MSB
5	0	R4
4	0	R3
3	0	R2
2	0	R1
1	0	R0, LSB
0	0	R and N register mux selection. 0 = R and N values come from the ROM. 1 = data is loaded from the DAF registers into R and N.

Note:

5. Byte 13 and Byte 14 should be written together in every case.

Dial-a-Frequency Feature

SMBus Dial-a-Frequency feature is available in this device via Byte13 and Byte14. P is a large value PLL constant that depends on the frequency selection achieved through the hardware selectors (FS4, FS0). P value may be determined from the following table.

FS(4:0)	P
00111, 01101, 10111, 11100, 11110	127995867
00001, 00011, 00100, 01001, 01011, 01100, 10000, 10001, 10010, 10011, 10100, 11001, 11010, 11101, 11111	95996900
00101, 00110, 01000, 00111, 01110, 01111, 10101, 10110, 10010, 11011	76797520
0000, 00010, 01010, 11000	63997933

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing electromagnetic interference (EMI) radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control bytes. See the SMBus register section of this data sheet for the exact bit and byte functionally. The following table is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

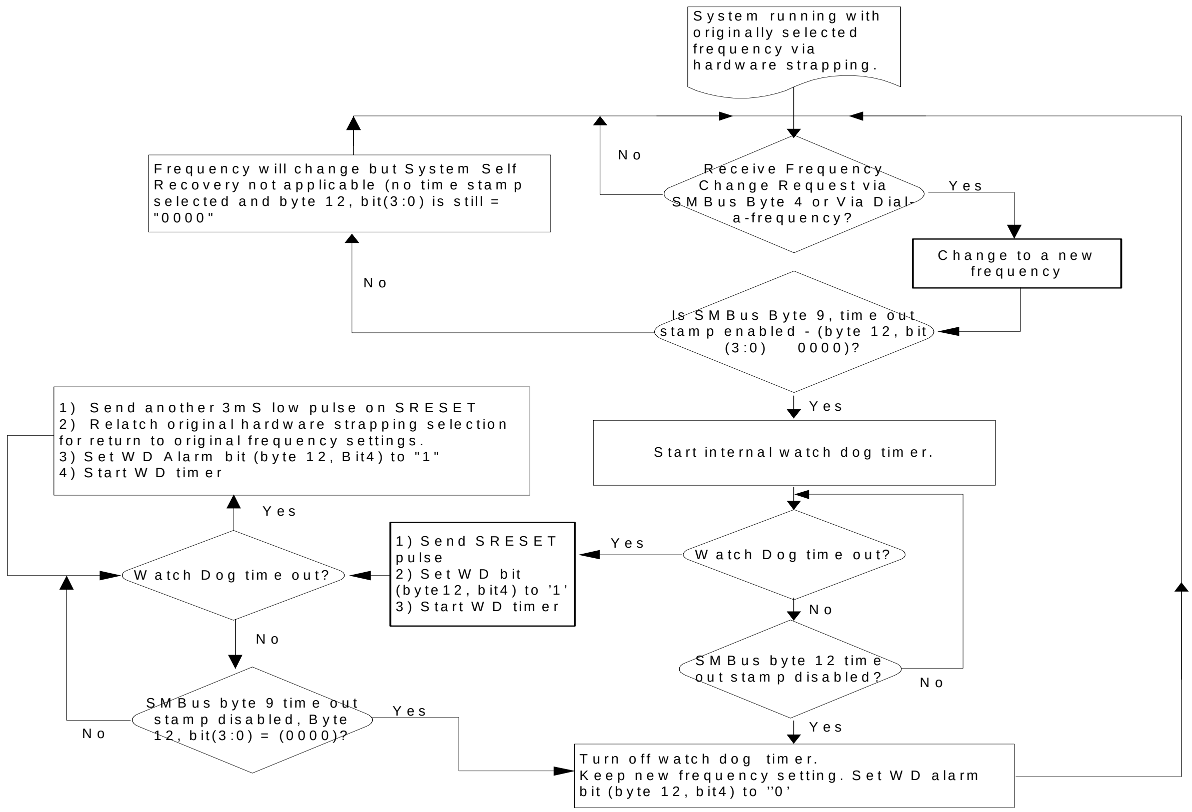
Table 9. Spread Spectrum

SS2	SS1	SS0	Spread Mode	Spread%
0	0	0	Down	–0.50
0	0	1	Down	–0.75
0	1	0	Down	–1.00
0	1	1	Down	–1.50
1	0	0	Center	+0.25, –0.25
1	0	1	Center	+0.37, –0.37
1	1	0	Center	+0.50, –0.50
1	1	1	Center	+0.75, –0.75

System Self-recovery Clock Management

This feature is designed to allow the system designer to change frequency while the system is running and reboot the operation of the system in case of a hang up due to the frequency change.

When the system sends an SMBus command requesting a frequency change through byte 4 or through bytes 13 and 14, it must have previously sent a command to byte 12, for selecting which time out stamp the Watchdog must perform, otherwise the System Self-recovery feature will not be applicable. Consequently, this device will change frequency and then the Watchdog timer starts timing. Meanwhile, the system BIOS is running its operation with the new frequency. If this device receives a new SMBus command to clear the bits originally programmed in byte 12, bits (3:0) (reprogram to 0000), before the Watchdog times out, then this device will keep operating in its normal condition with the new selected frequency. If the Watchdog times out the first time before the new SMBus reprograms Byte 12, bits (3:0) to (0000), then this device will send a low system reset pulse, on SRESET# (see byte12, bit7), and changes WD alarm (Byte12, Bit4) status to "1" then restarts the Watchdog timer again. If the Watchdog times out a second time, then this device will send another low pulse on SRESET#, will relatch original hardware strapping frequency (or second to last software selected frequency, see byte12, bit6) selection, set WD alarm bit (Byte12, bit4) to "1," then start WD timer again. The above described sequence will keep repeating until the BIOS clears the SMBus byte 12 bits (3:0). Once the BIOS sets byte 12 bits (3:0) = 0000, the Watchdog timer is turned off and the WD alarm bit (Byte 12, bit4) is reset to "0."


System running with originally selected frequency via hardware strapping.
Receive Frequency Change Request via SMBus Byte 4 or Via Dial-a-frequency?
No
Yes
Frequency will change but System Self Recovery not applicable (no time stamp selected and byte 12, bit(3:0) is still = "0000"
Change to a new frequency
No
Is SMBus Byte 9, time out stamp enabled - (byte 12, bit (3:0) 0000)?
Yes
Start internal watch dog timer.
1) Send another 3mS low pulse on SRESET
2) Relatch original hardware strapping selection for return to original frequency settings.
3) Set WD Alarm bit (byte 12, Bit4) to "1"
4) Start WD timer
Yes
1) Send SRESET pulse
2) Set WD bit (byte12, bit4) to '1'
3) Start WD timer
Yes
Watch Dog time out?
Watch Dog time out?
No
No
SMBus byte 12 time out stamp disabled?
No
SMBus byte 9 time out stamp disabled, Byte 12, bit(3:0) = (0000)?
Yes
No
Yes
Turn off watch dog timer.
Keep new frequency setting. Set WD alarm bit (byte 12, bit4) to "0'

Maximum Ratings

Input Voltage Relative to V_{SS}: .... V_{SS} – 0.3V
Input Voltage Relative to V_{DDQ} or AV_{DD}: .... V_{DD} + 0.3V
Storage Temperature: ....–65°C to + 150°C

Operating Temperature:.................................... 0°C to +70°C
Maximum Power Supply:... 3.5V

AC Parameters

Parameter	Description	100 MHz		133 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
Crystal							
TDC	Xin Duty Cycle	47.5	52.5	47.5	52.5	%	6,15
TPeriod	Xin Period	69.841	71.0	69.841	71.0	ns	6,7,9,15
VHIGH	Xin High Voltage	0.7Vdd	Vdd	0.7Vdd	Vdd	Volts	
VLOW	Xin Low Voltage	0	0.3Vdd	0	0.3Vdd	Volts	
Tr / Tf	Xin Rise and Fall Times		10.0		10.0	ns	
TCCJ	Xin Cycle to Cycle Jitter		500		500	ps	7,10,15
CPU at 0.7V Timing							
TSKEW	Any CPU to CPU Clock Skew		150		150	ps	10, 18, 22
TCCJ	CPU Cycle to Cycle Jitter		150		150	ps	10, 18, 22
TDC	CPU and CPUC Duty Cycle	45	55	45	55	%	10, 18, 22
TPeriod	CPU and CPUC Period	9.8	10.2	7.35	7.65	ns	10, 18, 22
Tr / Tf	CPU and CPUC Rise and Fall Times	175	700	175	700	ps	10, 11
	Rise/Fall Matching		20%		20%		11, 21, 22
DeltaTr	Rise Time Variation		125		125	ps	11, 22
DeltaTf	Fall Time Variation		125		125	ps	11, 22
Vcross	Crossing Point Voltage at 0.7V Swing	280	430	280	430	mV	11,18, 22
AGP							
TDC	AGP Duty Cycle	45	55	45	55	%	7, 9
TPeriod	AGP Period	15.0	15.3	15.0	15.3	ns	7, 9
THIGH	AGP High Time	5.25	–	5.25		ns	19
TLOW	AGP Low Time	5.05	–	5.05		ns	20
Tr / Tf	AGP Rise and Fall Times	0.5	1.6	0.5	1.6	ns	7, 8
Tskew Unbuffered	Any AGP to Any AGP Clock Skew		175		175	ps	7, 9
TCCJ	AGP Cycle to Cycle Jitter		250		250	ps	7, 9
ZCLK							
TDC	ZCLK(0:1) Duty Cycle	45	55	45	55	%	7, 9
Tr / Tf	ZCLK(0:1) Rise and Fall Times	0.5	1.6	0.5	1.6	ns	7, 8
TSKEW	Any ZCLK(0:1) to Any ZCLK(0:1) Skew		175		175	ps	7, 9

Notes:

6. This parameter is measured as an average over 1us duration with a crystal center frequency of 14.318MHz
7. All outputs loaded as per table 1 below.
8. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals (see test and measurement setup section of this data sheet).
9. Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals (see test and measurement setup section of this data sheet).
10. This measurement is applicable with Spread On or Spread OFF.
11. Measured from V_{OL} = 0.175 to V_{OH} = 0.525V.
12. The time specified is measured from when all VDD's reach their supply rail (3.3V) till the frequency output is stable and operating within the specifications.
13. Measured from when both SEL1 and SEL0 are low
14. CPU_STP# and PCI_STP# setup time with respect to any PCI_F clock to guarantee that the effected clock will stop or start at the next PCI_F clock's rising edge.
15. When Xin is driven from an external clock source.
16. When Crystal meets minimum 40 ohm device series resistance specification.
17. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
18. Measured at crossing point (Vx) or where subtraction of CLK-CLK# crosses 0V.
19. THIGH is measured at 2.4V for all non host outputs.
20. TLOW is measured at 0.4V for all non host outputs.
21. Determined as a fraction of 2*(Trise-Tfall)/ (Trise+Tfall).
22. For CPU load. See *Figure 1*.

AC Parameters (continued)

Parameter	Description	100 MHz		133 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
TCCJ	ZCLK(0:1) Cycle to Cycle Jitter		250		250	ps	7,9
PCI							
TDC	PCI_F(0:1) PCI (0:5) Duty Cycle	45	55	45	55	%	7, 9
TPeriod	PCI_F(0:1) PCI (0:5) Period	30.0		30.0		nS	6,7,9
THIGH	PCI_F(0:1) PCI (0:5) High Time	12.0		12.0		nS	19
TLOW	PCI_F(0:1) PCI (0:5) Low Time	12.0		12.0		nS	20
Tr / Tf	PCI_F(0:1) PCI (0:5) Rise and Fall Times	0.5	2.0	0.5	2.0	nS	7, 8
TSKEW	Any PCI Clock to Any PCI Clock Skew		500		500	pS	7, 9
TCCJ	PCI_F(0:1) PCI (0:5) Cycle to Cycle Jitter		250		250	ps	7, 9
SDCLK							
TDC	SDCLK Duty Cycle	45	55	45	55	%	7, 9
TPeriod	SDCLK Period	7.4	15	7.4	15	ns	7, 9
THIGH	SDCLK High Time	3.0		1.87		ns	19
TLOW	SDCLK Low Time	2.8		1.67		ns	20
Tr / Tf	SDCLK Rise and Fall Times	0.4	1.6	0.4	1.6	ns	7, 8
TCCJ	SDCLK Cycle to Cycle Jitter	–	250	–	250	ps	7, 8
48M							
TDC	48M Duty Cycle	45	55	45	55	%	7, 9
TPeriod	48M Period	20.829	20.834	20.829	20.834	ns	7, 9
Tr / Tf	48M Rise and Fall Times	1.0	2.0	1.0	2.0	ns	7, 8
TCCJ	48M Cycle to Cycle Jitter		350		350	ps	7, 9
24M							
TDC	24 MHz Duty Cycle	45	55	45	55	%	7, 9
TPeriod	24 MHz Period	41.66	41.67	41.66	41.67	ns	7, 9
Tr / Tf	24 MHz Rise and Fall Times	1.0	4.0	1.0	4.0	ns	7, 8
TCCJ	24 MHz Cycle to Cycle Jitter		500		500	ps	7, 9
REF							
TDC	REF Duty Cycle	45	55	45	55	%	7, 9
TPeriod	REF Period	69.8413	71.0	69.8413	71.0	ns	7, 9
Tr / Tf	REF Rise and Fall Times	1.0	4.0	1.0	4.0	ns	7, 8
TCCJ	REF Cycle to Cycle Jitter		1000		1000	ps	7, 9
ENABLE/DISABLE and SET-UP							
tpZL, tpZH	Output Enable Delay (all outputs)	1.0	10.0	1.0	10.0	ns	
tpLZ, tpZH	Output Disable Delay (all outputs)	1.0	10.0	1.0	10.0	ns	
tstable	All Clock Stabilization from power-up		1.5		1.5	ms	
tss	Stopclock Set-up Time	10.0		10.0		ns	
tsh	Stopclock Hold Time	0		0		ns	14

Table 10. Maximum Lumped Capacitive Output Loads

Clock	Max. Load	Units
PCI(0:5), PCI_F(0:1)	30	pF
AGP(0:1), SDCLK	30	pF
ZCLK	10	pF
48M_24, 48M Clock	20	pF
REF(0:2)	30	pF
CPU(0:1)T, CPU(0:1)C	2	pF

DC Characteristics

Current Accuracy

	Conditions	Configuration	Load	Min.	Max.
Iout	V_{DD} = nominal (3.30V)	M0 = 0 or 1 and Rr shown in table	Nominal test load for given configuration	–7% Inom[23]	+7% Inom
Iout	V_{DD} = 3.30 ±5%	All combinations of M0 or 1 and Rr shown in table	Nominal test load for given configuration	–12% Inom	+12% Inom

DC Component Parameters (V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
Idd3.3V	Dynamic Supply Current	All frequencies at maximum values[24]			300	mA
Ipd3.3V	Power-down Supply Current	PD# Asserted			*Note 25*	mA
Cin	Input Pin Capacitance				5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Cxtal	Crystal Pin Capacitance	Measured from the Xin or Xout pin to Ground	30	36	42	pF

Notes:

23. Inom refers to the expected current based on the configuration of the device
24. All outputs loaded as per maximum capacitive load table.
25. Absolute value = (Programmed CPU Iref) +10mA

Test and Measurement Set-up

For Differential CPU Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

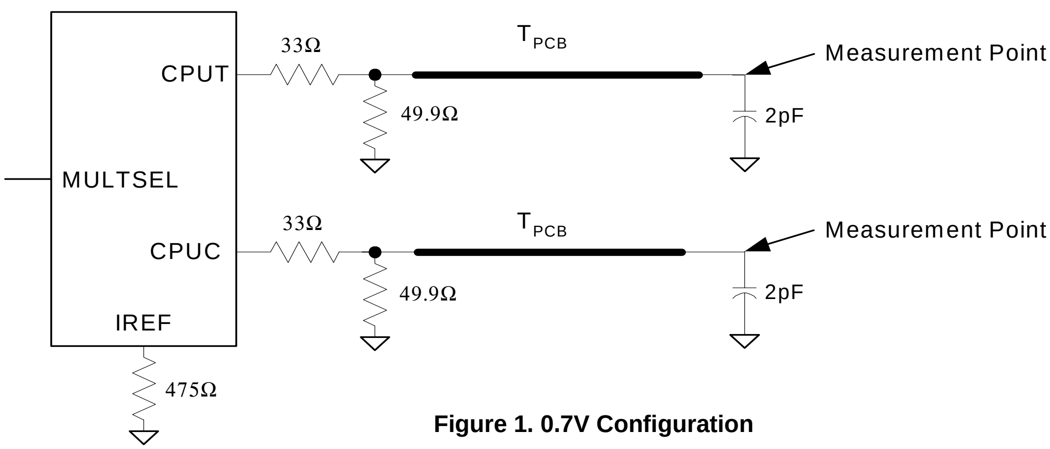


Figure 1. 0.7V Configuration

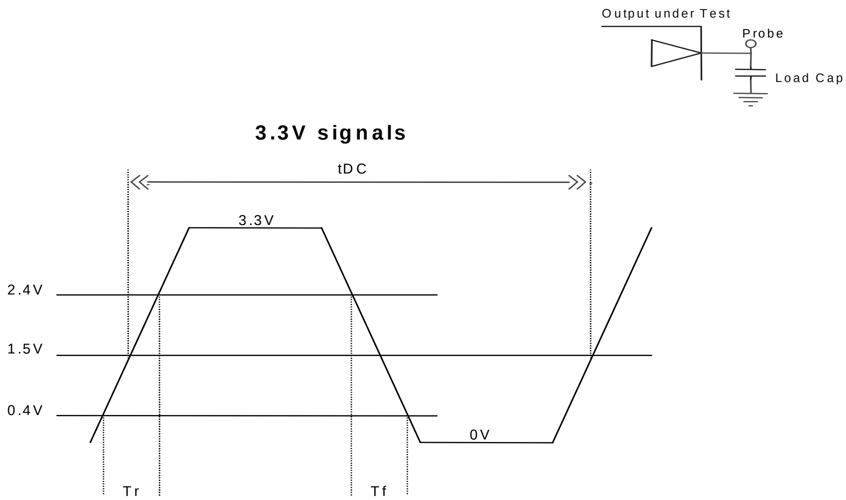


Figure 2. Lumped Load For Single-Ended Output Signals (for AC Parameters Measurement)

Table 11. CPU Clock Current Select Function

Mult0	Board Target Trace/Term Z	Reference R, Iref – V_{DD} (3*Rr)	Output Current	V_{OH} @ Z
0	50 Ohms (not used)	Rr = 221 1%, Iref = 5.00 mA	I_{OH} = 4*Iref	1.0V @ 50
1	50 Ohms	Rr = 475 1%, Iref = 2.32 mA	I_{OH} = 6*Iref	0.7V @ 50

Table 12. Group Timing Relationship and Tolerances

	Offset	Tolerance (or Range)	Conditions	Notes
CPU to SDCLK	TypicaL 0 ns	± 2 ns	CPU leads	26
CPU to AGP	TypicaL 2 ns	1–4 ns	CPU leads	26
CPU to ZCLK	TypicaL 2 ns	1–4 ns	CPU leads	26
CPU to PCI	Typical 2 ns	1–4 ns	CPU leads	26

CPU_STP# Clarification

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function.

CPU_STP# Assertion

When CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped after being sampled by two falling CPU clock edges. The final state of the stopped CPU signals is CPU = HIGH and CPU0# = LOW. There is no change to the output drive current values during the stopped state. The CPU is driven HIGH with a current value equal to (Mult 0 “select”) × (Iref), and the CPU# signal will not be driven. Due to external pull-down circuitry CPU# will be LOW during this stopped state.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{setup}) (see *Figure 5*). The PCI_F (0:2) clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free-running.

Note:

26. See *Figure 1* for CPU clock measurement point. See*Figure 2* for SDCLK, AGP, ZCLK, and PCI Outputs measurement point.

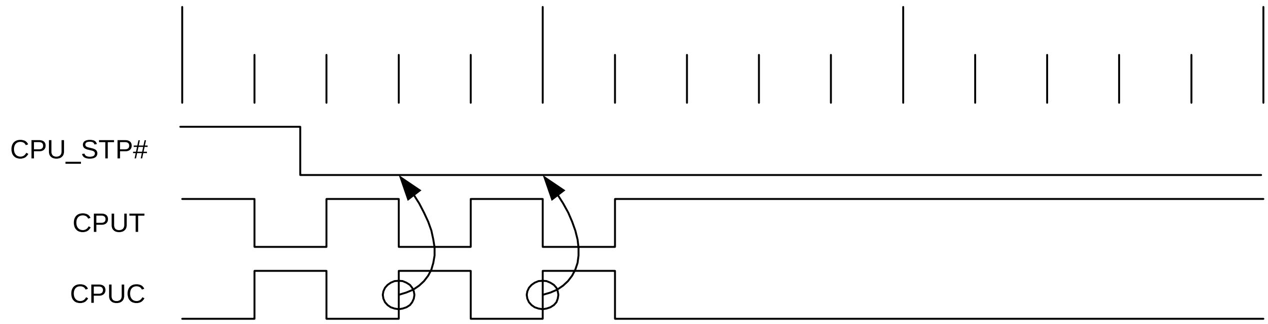


Figure 3. Assertion CPU_STP# Waveform

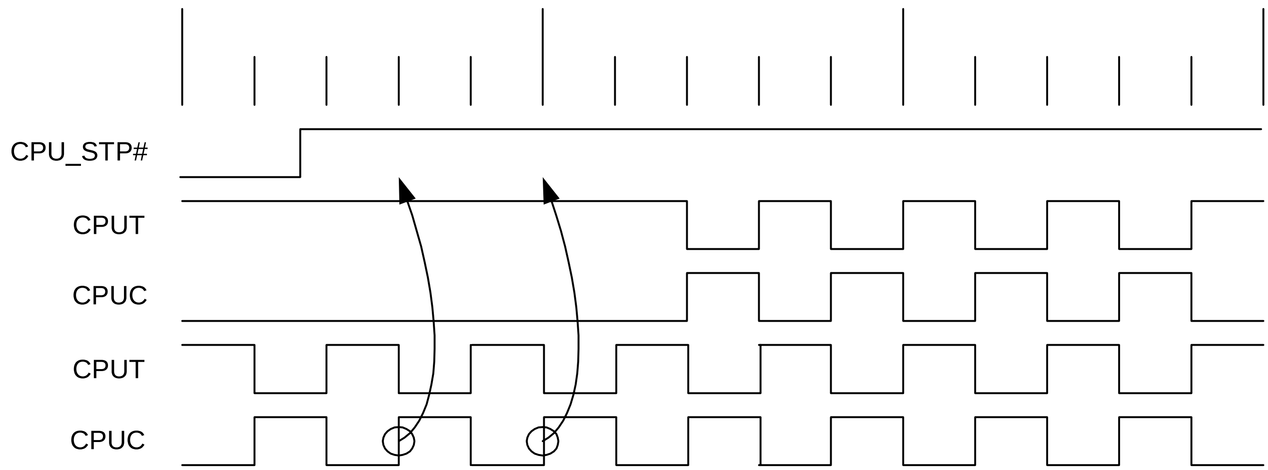


Figure 4. Deassertion CPU_STP# Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI(0:6) and stoppable PCI_F(0:2) clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a HIGH level.

PD# (Power-down) Clarification

The PD# (power-down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is low, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low “stopped” state.

PD#–Assertion (transition from logic “l” to logic “0”)

When PD# is sampled LOW by two consecutive rising edges of CPUC clock, all clock outputs (except CPUT) clocks must be held LOW on their next HIGH to LOW transition. CPUT clocks must be hold with CPUT clock pin driven HIGH with a value of 2x Iref and CPUC undriven.

Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

PD# Deassertion (transition from logic “0” to logic “l”)

The power-up latency between PD# rising to a valid logic “1” level and the starting of all clocks is less than 3.0 ms.

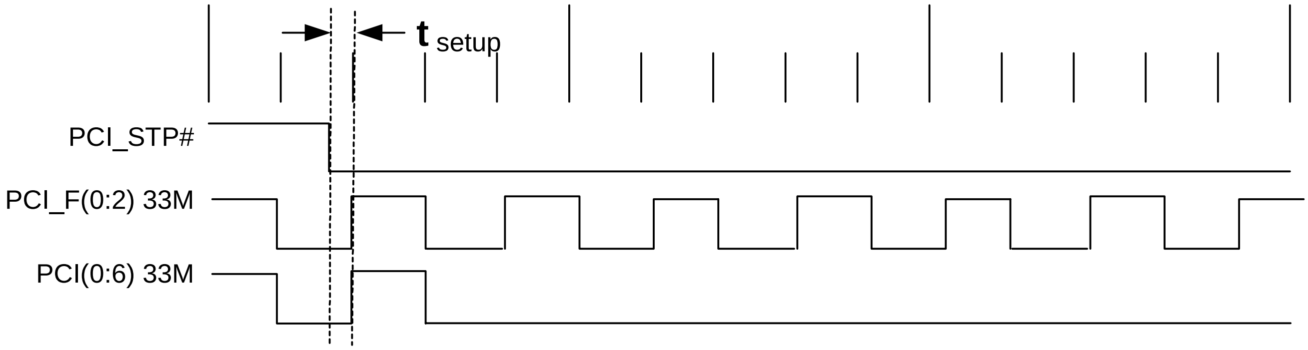


Figure 5. Assertion PCI_STP# Waveform

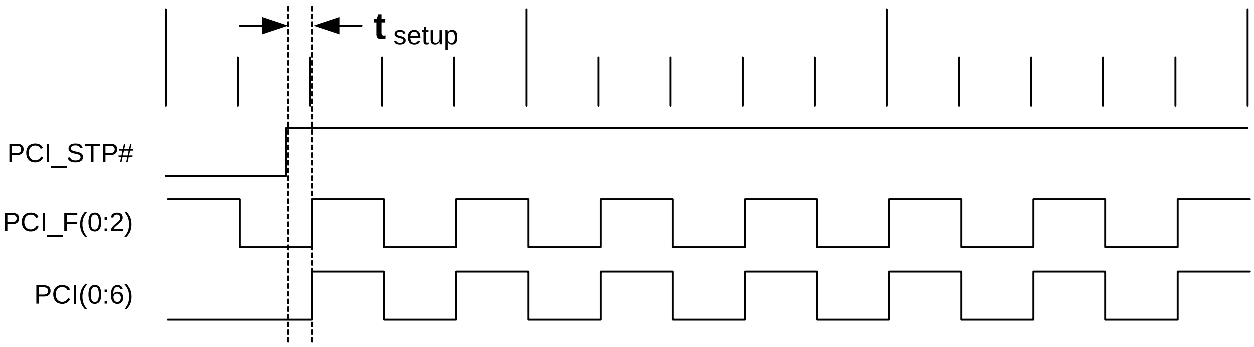


Figure 6. Deassertion PCI_STP# Waveform[27]

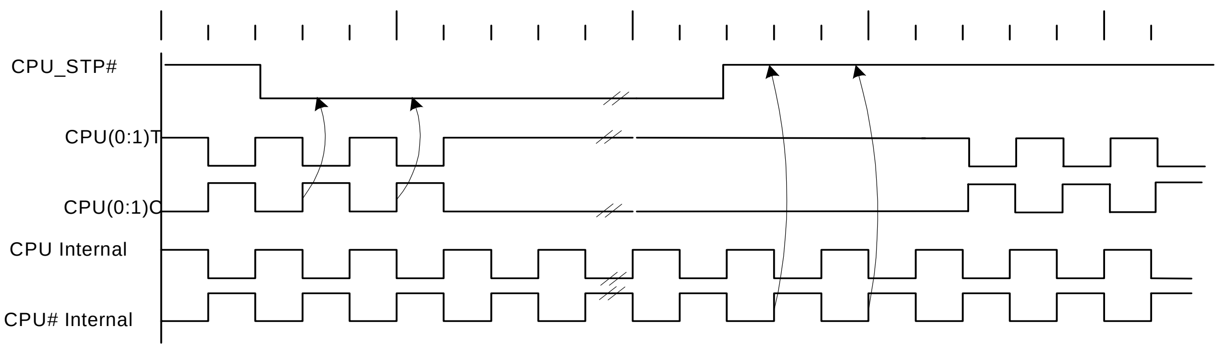


Figure 7. Power-down Assertion/Deassertion Timing Waveforms–Nonbuffered Mode

Note:

27. The PCI STOP function is controlled by two inputs. One is the device PCI_STP# pin 34 and the other is SMBus Byte 0 Bit 3. These two inputs are logically ANDed. If either the external pin or the internal SMBus register bit is set low, the stoppable PCI clocks will be stopped in a logic LOW state. Reading SMBus Byte 0 Bit 3 will return a 0 value if either of these control bits are set LOW, thereby indicating that the device's stoppable PCI clocks are not running.

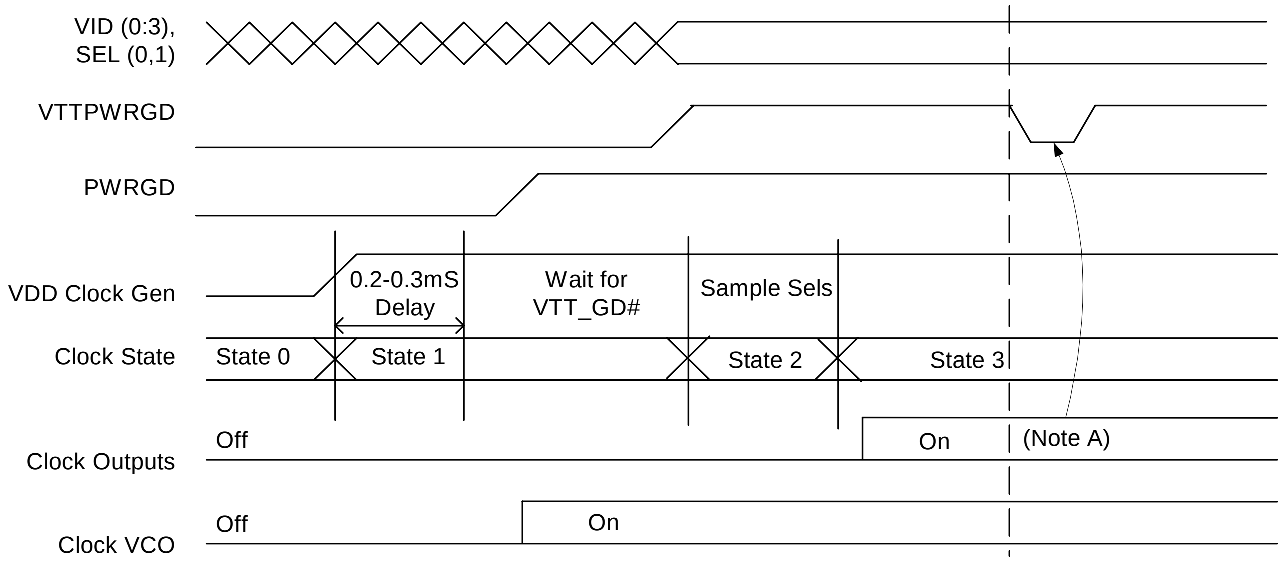


Figure 8. VTTPWRGD Timing Diagram[28]

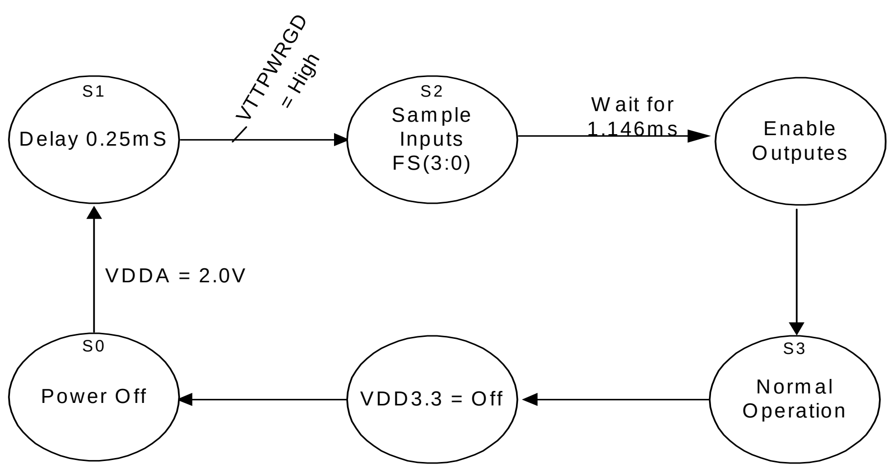


Figure 9. Clock Generator Power-up/Run State Diagram

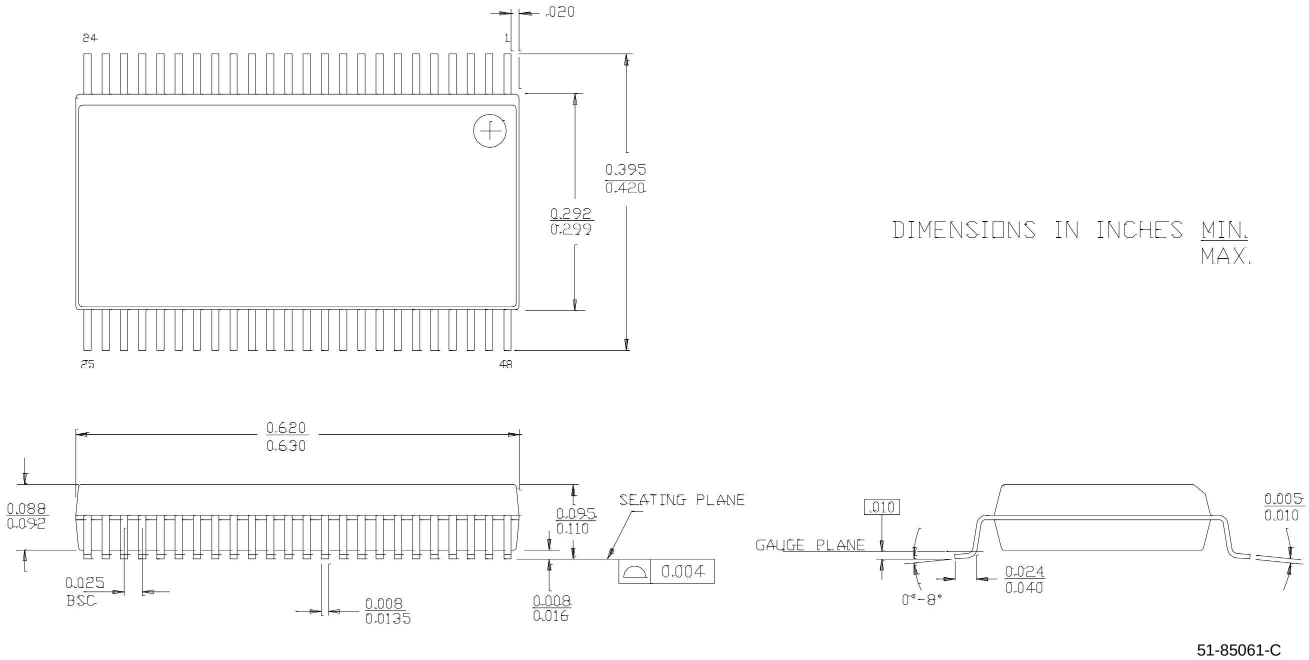
28. Device is not affected, VTTPWRGD is ignored.

Ordering Information

Part Number	Package Type	Product Flow
CY28370OC	48-pin Shrunk Small Outline Package (SSOP)	Commercial, 0° to 70°C
CY28370OCT	48-pin Shrunk Small Outline Package (SSOP)–Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-lead Shrunk Small Outline Package O48



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**	112789	05/07/02	DMG	New Data Sheet