Universal Single-Chip Clock Solution for VIA P4M266/KM266 DDR Systems

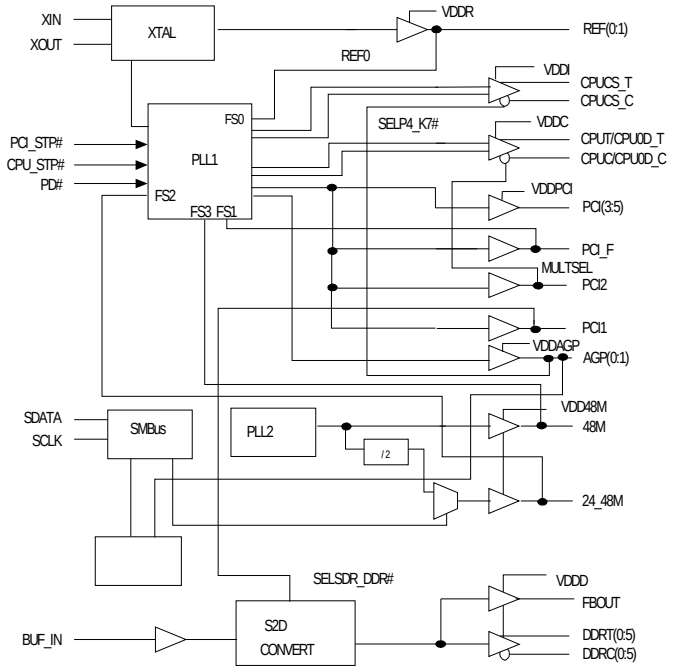
Features

- **Supports VIA P4M266/KM266 chipsets**
- **Supports Pentium® 4, Athlon™ processors**
- **Supports two DDR DIMMS**
- **Provides**
  - **— Two different programmable CPU clock pairs**
  - **— Six differential DDR SDRAM pairs**
  - **— Two low-skew/low-jitter AGP clocks**
  - **— Six low-skew/low-jitter PCI clocks**
  - **— One 48M output for USB**
  - **— One programmable 24M or 48M for SIO**
- **Dial-a-Frequency™ and Dial-a-dB™ features**
- **Spread Spectrum for best electromagnetic interference (EMI) reduction**
- **SMBus-compatible for programmability**
- **56-pin SSOP and TSSOP packages**

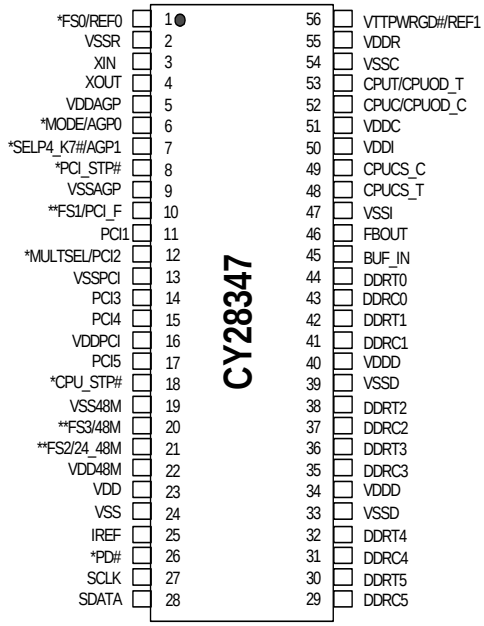
Table 1. Frequency Selection Table

FS(3:0)	CPU	AGP	PCI
0000	66.80	66.80	33.40
0001	100.20	66.80	33.40
0010	120.00	60.00	30.00
0011	133.33	66.67	33.33
0100	72.00	72.00	36.00
0101	105.00	70.00	35.00
0110	160.00	64.00	32.00
0111	140.00	70.00	35.00
1000	77.00	77.00	38.50
1001	110.00	73.33	36.67
1010	180.00	60.00	30.00
1011	150.00	60.00	30.00
1100	90.00	60.00	30.00
1101	100.00	66.67	33.33
1110	200.00	66.67	33.33
1111	133.33	66.67	33.33

Block Diagram



Pin Configuration[1]



Note:

1. Pins marked with [*] have internal pull-up resistors. Pins marked with [**] have internal pull-down resistors.

Pin Description [2]

Pin	Name	PWR	I/O	Description
3	XIN		I	**Oscillator Buffer Input**. Connect to a crystal or to an external clock.
4	XOUT	VDD	O	**Oscillator Buffer Output**. Connect to a crystal. Do not connect when an external clock is applied at XIN.
1	FS0/REF0	VDD	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, FS0 is the input. When the power supply voltage crosses the input threshold voltage, FS0 state is latched and this pin becomes REF0, buffered copy of signal applied at XIN. (1–2 x strength, selectable by SMBus. Default value is 1 x strength.)
56	VTTPWRGD#	VDDR	I	If SELP4_K7# = 1, with a P4 processor setup as CPU(T:C). At power-up, VTT_PWRGD# is an input. When this input is sampled LOW, the FS (3:0) and MULTSEL are latched and all output clocks are enabled. After the first transition to a LOW on VTT_PWRGD#, this pin is ignored and will not effect the behavior of the device thereafter. When the VTT_PWRGD# feature is not used, please connect this signal to ground through a 10KΩ resistor.
	REF1	VDDR	O	If SELP4_K7# = 0, with an Athlon (K7) processor as CPUOD_(T:C). VTT_PWRGD# function is disabled, and the feature is ignored. This pin becomes REF1 and is a buffered copy of the signal applied at XIN.
44,42,38, 36,32,30	DDRT(0:5)	VDDD	O	These pins are configured for DDR clock outputs. They are "True" copies of signal applied at Pin45, BUF_IN.
43,41,37 35,31,29	DDRC(0:5)	VDDD	O	These pins are configured for DDR clock outputs. They are "Complementary" copies of signal applied at Pin45, BUF_IN.
7	SELP4_K7#/AGP1	VDDAGP	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, SELP4_K7# is the input. When the power supply voltage crosses the input threshold voltage, SELP4_K7# state is latched and this pin becomes AGP1 clock output. SELP4_K7# = 1 selects P4 mode. SELP4_K7# = 0 selects K7 mode.
12	MULTSEL/PCI2	VDDPCI	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, MULTSEL is the input. When the power supply voltage crosses the input threshold voltage, MULTSEL state is latched and this pin becomes PCI2 clock output. MULTSEL = 0, Ioh is 4 x IREFMULTSEL = 1, Ioh is 6 x IREF
53	CPUT/CPUOD_T	VDDC	O	**3.3V True CPU Clock Outputs**. This pin is programmable through strapping pin7, SELP4_K7#. If SELP4_K7# = 1, this pin is configured as the CPUT Clock Output. If SELP4_K7# = 0, this pin is configured as the CPUOD_T Open Drain Clock Output. See *Table 1.*
52	CPUC/CPUOD_C	VDDC	O	**3.3V Complementary CPU Clock Outputs**. This pin is programmable through strapping pin7, SELP4_K7#. If SELP4_K7# = 1, this pin is configured as the CPUC Clock Output. If SELP4_K7# = 0, this pin is configured as the CPUOD_C Open Drain Clock Output. See *Table 1.*
14,15,17	PCI (3:5)	VDDPCI	O	**PCI Clock Outputs**. Are synchronous to CPU clocks. See *Table 1.*
48,49	CPUCS_T/C	VDDI	O	**2.5V CPU Clock Outputs for Chipset**. See *Table 1*.
18	CPU_STP#	VDDPCI	I PU	If pin 6 is pulled down at power on reset, then this pin becomes CPU_STP#. When CPU_STP# is asserted LOW, then both of the CPU signals stop at the next HIGH to LOW transition or stays LOW if it already is LOW. This does not stop the CPUCS signals.
10	FS1/PCI_F	VDDPCI	I/O PD	**Power-on Bidirectional Input/Output**. At power-up, FS1 is the input. When the power supply voltage crosses the input threshold voltage, FS1 state is latched and this pin becomes PCI_F clock output.
20	FS3/48M	VDD48M	I/O PD	**Power-on Bidirectional Input/Output**. At power-up, FS3 is the input. When the power supply voltage crosses the input threshold voltage, FS3 state is latched and this pin becomes 48M, a USB clock output.
11	PCI1	VDDPCI	O	**PCI Clock Output**

Note:
2. PU = internal pull-up. PD = internal pull-down. Typically = 250 kW (range 200 kW to 500 kW).

Pin Description (continued)[2]

Pin	Name	PWR	I/O	Description
21	FS2/24_48M	VDD48M	I/O PD	**Power-on Bidirectional Input/Output.** At power-up, FS2 is the input. When the power supply voltage crosses the input threshold voltage, FS2 state is latched and this pin becomes 24_48M, a SIO programmable clock output.
6	MODE/AGP0	VDDAGP	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, MODE is an input and becomes AGP0 output after the power supply voltage crosses the input threshold voltage. Must have 10KΩ resistor to V_{SS}. See *Table 2*.
8	PCI_STP#	VDDAGP	I PU	If pin 6 is pulled down at power on reset, then this pin becomes PCI_STP#. When PCI_STP# is asserted LOW, then all of the PCI signals, except the PCI_F, stops at the next HIGH to LOW transition or stays LOW if it already is LOW.
25	IREF		I	Current reference programming input for CPU buffers. A precise resistor is attached to this pin, which is connected to the internal current reference.
28	SDATA		I/O	**Serial Data Input**. Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
27	SCLK		I	**Serial Clock Input**. Conforms to the SMBus specification.
26	PD#		I PU	When PD# is asserted LOW, the device enters power down mode. See power management function.
45	BUF_IN		I	2.5V CMOS type input to the DDR differential buffers.
46	FBOUT		O	This is the single-ended, SDRAM buffered output of the signal applied at BUF_IN. It is in phase with the DDRT(0:5) signals.
5	VDDAGP			3.3V power supply for AGP clocks
51	VDDC			3.3V power supply for CPU (T: C) clocks
16	VDDPCI			3.3V power supply for PCI clocks
55	VDDR			3.3V power supply for REF clock
50	VDDI			2.5V power supply for CPUCS_T/C clocks
22	VDD48M			3.3V power supply for 48M
23	VDD			3.3V Common power supply
34,40	VDDD			2.5V power supply for DDR clocks
9	VSSAGP			Ground for AGP clocks
13	VSSPCI			Ground for PCI clocks
54	VSSC			Ground for CPU (T:C) clocks
33,39	VSSD			Ground for DDR clocks
19	VSS48M			Ground for 48M clock
47	VSSI			Ground for CPUCS_T/C clocks
24	VSS			Common ground

Table 2. MODE Pin-Power Management Input Control

MODE, Pin 6 (Latched Input)	Pin 26	Pin 18	Pin 8
0	PD#	CPU_STP#	PCI_STP#
Invalid	Reserved	Reserved	Reserved

Table 3. Swing Select Functions Through Hardware

MULTSEL	Board Target Trace/Term Z	Reference R, IREF = VDD/(3*Rr)	Output Current	VOH@Z
0	50 Ohm	Rr = 221 1%, IREF = 5.00 mA	IOH = 4* Iref	1.0V@50
1	50 Ohm	Rr = 475 1%, IREF = 2.32 mA	IOH = 6* Iref	0.7V@50

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled.

The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operation from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 4*.

The Block Write and Block Read protocol is outlined in *Table 5* while *Table 6* outlines the corresponding Byte Write and Byte Read protocol. The slave receiver address is 11010010 (D2H).

Table 4. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation
(6:0)	Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be “0000000”

Table 5. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit “00000000” stands for block operation	11:18	Command Code - 8 Bit “00000000” stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 6. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits

Table 6. Byte Read and Byte Write Protocol (continued)

9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits “1xxxxxxx” stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits “1xxxxxxx” stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Byte 0: Frequency Select Register

Bit	@Pup	Pin#	Name	Description
7	0			Reserved.
6	H/W Setting	21	FS2	For Selecting Frequencies see *Table 1.*
5	H/W Setting	10	FS1	For Selecting Frequencies see *Table 1.*
4	H/W Setting	1	FS0	For Selecting Frequencies see *Table 1.*
3	0			If this bit is programmed to “1,” it enables WRITES to bits (6:4,1) for selecting the frequency via software (SMBus) If this bit is programmed to a “0” it enables only READS of bits (6:4,1), which reflect the hardware setting of FS(0:3).
2	H/W Setting	11	Reserved	Reserved
1	H/W Setting	20	FS3	For Selecting frequencies in *Table 1*.
0	H/W Setting	7	SELP4_K7#	Only for reading the hardware setting of the CPU interface mode, status of SELP4_K7# strapping.

Byte 1: CPU Clocks Register

Bit	@Pup	Pin#	Name	Description
7	0		SSMODE	0 = Down Spread. 1 = Center Spread. See *Table 9*.
6	1		SSCG	1 = Enable (default). 0 = Disable
5	1		SST1	Select spread bandwidth. See *Table 9*.
4	1		SST0	Select spread bandwidth. See *Table 9*.
3	1	48,49	CPUCS_T/C_ EN#	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
2	1	53,52	CPUOD_T/C_EN#	1 = output enabled (running). 0 = output disable asynchronously in a LOW state.
1	0	53,52	CPUT/C_PD_CNTRL	In K7 mode, this bit is ignored. In P4 mode, when PD# asserted LOW, 0 = drive CPUT to 2xIref and CPUC LOW and 1 = three-state CPUT and CPUC.
0	1	11	MULT0	Only For reading the hardware setting of the Pin11 MULT0 value.

Byte 2: PCI Clock Register

Bit	@Pup	Pin#	Name	Description
7	0		PCI_DRV	PCI clock output drive strength 0 = Normal, 1 = increase the drive strength 20%.
6	1	10	PCI_F	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
5	1			Reserved, set = 1.

Byte 2: PCI Clock Register (continued)

Bit	@Pup	Pin#	Name	Description
4	1	17	PCI5	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
3	1	15	PCI4	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
2	1	14	PCI3	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
1	1	12	PCI2	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
0	1	11	PCI1	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.

Byte 3: AGP/Peripheral Clocks Register

Bit	@Pup	Pin#	Name	Description
7	0	21	24_48M	"0" = pin 21 output is 24 MHz. Writing a “1” into this register asynchronously changes the frequency at pin 21 to 48 MHz.
6	1	20	48MHz	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
5	1	21	24_48M	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
4	0	6,7,8	DASAG1	Programming these bits allow shifting skew of the AGP(0:2) signals relative to their default value. See *Table 7*.
3	0	6,7,8	DASAG0	
2	1			Reserved, set = 1.
1	1	7	AGP1	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
0	1	6	AGP0	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.

Byte 4: Peripheral Clocks Register

Bit	@Pup	Pin#	Name	Description
7	1	20	48M	1 = strength x 1. 0= strength x 2 1 = strength x 1. 0= strength x 2
6	1	21	24_48M	1 = strength x 1. 0= strength x 2 1 = strength x 1. 0= strength x 2
5	0	6,7,8	DARAG1	Programming these bits allow modifying the frequency ratio of the AGP(2:0), PCI(6:1, F) clocks relative to the CPU clocks. See *Table 8*.
4	0	6,7,8	DARAG0	
3	1	1	REF0	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
2	1	56	REF1	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state. (K7 Mode only.)
1	1	1	REF0	1 = strength x 1. 0 = strength x 2
0	1	56	REF1	1 = strength x 1. 0 = strength x 2 (K7 Mode only)

Table 7. Dial-a-Skew™ AGP(0:2)

DASAG (1:0)	AGP(0:2) Skew Shift
00	Default
01	–280 ps
10	+280 ps
11	+480 ps

Table 8. Dial-A-Ratio™ AGP(0:2)

DARAG (1:0)	CU/AGP Ratio
00	Frequency Selection Default
01	2/1
10	2.5/1
11	3/1

Byte 5: DDR Clock Register

Bit	@Pup	Pin#	Name	Description
7	0	45	BUF_IN threshold voltage	DDR Mode, BUF_IN threshold setting. 0 = 1.15V, 1 = 1.05V.
6	1	46	FBOUT	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
5	1	29,30	DDRT/C5	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
4	1	31,32	DDRT/C4	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
3	1	35,36	DDRT/C3	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
2	1	37,38	DDRT/C2	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
1	1	41,42	DDRT/C1	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.
0	1	43,44	DDRT/C0	1 = output enabled (running). 0 = output disabled asynchronously in a LOW state.

Byte 6: Reserve Register

Bit	@Pup	Description
7	1	Reserved.
6	0	Reserved.
5	0	Reserved.
4	0	Reserved.
3	0	Reserved.
2	0	Reserved.
1	0	Reserved.
0	0	Reserved.

Byte 7: Dial-a-Frequency Control Register N

Bit	@Pup	Name	Description
7	0	Reserved	Reserved for device function test.
6	0	N6, MSB	These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0	N5	
4	0	N4	
3	0	N3	
2	0	N2	
1	0	N1	
0	0	N0, LSB	

Byte 8: Silicon Signature Register (all bits are Read-only)

Bit	@Pup	Name	Description
7	0	Revision_ID3	Revision ID bit [3]
6	0	Revision_ID2	Revision ID bit [2]

Byte 8: Silicon Signature Register (all bits are Read-only)

5	0	Revision_ID1	Revision ID bit [1]
4	0	Revision_ID0	Revision ID bit [0]
3	1	Vender_ID3	Cypress's Vendor ID bit [3]
2	0	Vender_ID2	Cypress's VendorID bit [2]
1	0	Vender_ID1	Cypress's Vendor ID bit [1]
0	0	Vender_ID0	Cypress's Vendor ID bit [0]

Byte9: Dial-A-Frequency Control Register R

Bit	@Pup	Name	Description
7	0		Reserved
6	0	R5, MSB	These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0	R4	
4	0	R3	
3	0	R2	
2	0	R1	
1	0	R0	
0	0	DAF_ENB	R and N register mux selection. 0=R and N values come from the ROM. 1=data is load from DAF (I2C) registers.

Dial-a-Frequency Feature

SMBus Dial-a-frequency feature is available in this device via Byte7 and Byte9.

P is a PLL constant that depends on the frequency selection prior to accessing the Dial-a-Frequency feature.

FS(4:0)	P
XXXXX	96016000

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is enabled/disabled via SMBus register Byte 1, Bit 7.

Table 9. Spread Spectrum Table

Mode	SST1	SST0	% Spread
0	0	0	–1.5%
0	0	1	–1.0%
0	1	0	–0.7%
0	1	1	–0.5%
1	0	0	±0.75%
1	0	1	±0.5%
1	1	0	±0.35%
1	1	1	±0.25%

Maximum Ratings

Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: .....–65°C to + 150°C
Operating Temperature: .....0°C to +70°C
Maximum ESD 2000V
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to HIGH static voltages or electric field. However, precautions should be take to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range.

$V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters ($V_{DD} = V_{DDPCI} = V_{DDAGP} = V_{DDR} = V_{DD48M} = V_{DDC} = 3.3V \pm 5\%$, $V_{DDI} = V_{DD} = 2.5 \pm 5\%$, $T_A = 0$ °C to +70 °C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VIL1	Input LOW Voltage	Applicable to PD#, F S(0:4)			1.0	Vdc
VIH1	Input HIGH Voltage		2.0			Vdc
VIL2	Input LOW Voltage	Applicable to SDATA and SCLK			1.0	Vdc
VIH2	Input HIGH Voltage		2.2			Vdc
Vol	Output LOW Voltage for Sreset#	IOL	0.4			V
Iol	Pull-down Current for Sreset#	VOL = 0.4V	24	35		mA
Ioz	Three-state Leakage Current				10	µA
Idd3.3V	Dynamic Supply Current	CPU frequency set at 133.3 MHz		156	180	mA
Idd2.5V	Dynamic Supply Current	CPU frequency set at 133.3 MHz		177	200	mA
Ipd	Power-down Supply current	PD# = 0		3.8	4.0	mA
Ipup	Internal Pull-up Device Current	Input @ V_{SS}			–25	µA
Ipdwn	Internal Pull-down Device Current	Input @ V_{DD}			10	µA
Cin	Input Pin Capacitance				5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	pF
Cxtal	Crystal Pin Capacitance	Measured from the X_{IN} or X_{OUT} to V_{SS}	27	36	45	pF

AC Parameters

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	M.ax	Min.	Max.		
Crystal											
TDC	Xin Duty Cycle	45	55	45	55	45	55	45	55	%	4,7,14,15
TPeriod	Xin Period	69.84	71.0	69.84	71.0	69.84	71.0	69.84	71.0	ns	4,7,14,15
VHIGH	Xin HIGH Voltage	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	V	13,14
VLOW	Xin LOW Voltage	0	$0.3V_{DD}$	0	$0.3V_{DD}$	0	$0.3V_{DD}$	0	$0.3V_{DD}$	V	
Tr / Tf	Xin Rise and Fall Times		10.0		10.0		10		10	ns	14
TCCJ	Xin Cycle to Cycle Jitter		500		500		500		500	ps	5,8,11,12
Txs	Crystal Start-up Time		30		30		30		30	ms	13
P4 Mode CPU at 0.7V											
TDC	CPUT/C Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7,18, 23
TPeriod	CPUT/C Period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	ns	4,5,7,18,23

Notes:

3. All outputs loaded as per maximum capacitative load table in P4 and DDR mode. See *Table 11*.
4. All outputs loaded as per loading specified in the loading table. See *Table 11*.
5. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals, and between 20% and 80% for differential signals.
6. Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at 1.25V for 2.5V, and 50% point for differential signals.
7. This measurement is applicable with Spread ON or spread OFF.
8. Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals.
9. Probes are placed on the pins, and measurements are acquired at 0.4V.
10. The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within specifications.
11. When Xin is driven from and external clock source (3.3V parameters apply).
12. When Crystal meets minimum 40 ohm device series resistance specification.
13. Measured between 0.2Vdd and 7Vdd.
14. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
15. The typical value of VX is expected to be 0.5*VDDD (or 0.5*VDDC for CPUCS signals) and will track the variations in the DC level of the same.
16. VD is the magnitude of the difference between the measured voltage level on a DDRT (and CPUCS_T) clock and the measured voltage level on its complementary DDRC (and CPUCS_C) one.
17. Measured at VX, or where subtraction of CLK–CLK# crosses 0 volts.
18. Measured at VX between the rising edge and the following falling edge of the signal.

AC Parameters (continued)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	M.ax	Min.	Max.		
Tr/Tf	CPUT/C Rise and Fall Times	175	700	175	700	175	700	175	700	ps	22,23
	Rise/Fall Matching		20%		20%		20%		20%		22,24
Delta Tr/Tf	Rise/Fall Time Variation		125		125		125		125	ps	5,10,22,23
TSKEW	CPUT/C to CPUCS_T/C Clock Skew		100		100		100		100	ps	5,8,11,18,23
TCCJ	CPUT/C Cycle to Cycle Jitter		150		150		150		150	ps	5,7,8,11,18, 23
Vcross	Crossing Point Voltage	280	430	280	430	280	430	280	430	mV	23.
P4 Mode CPU at 1.0V											
TDC	CPUT/C Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7,18
TPeriod	CPUT/C Period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	nS	4,5,7,18
Differential Tr/Tf	CPUT/C Rise and Fall Times	175	467	175	467	175	467	175	467	ps	5,8,27
Delta Tr/Tf	Rise/Fall Time Variation		125		125		125		125	ps	5,10
TSKEW	CPUT/C to CPUCS_T/C Clock Skew		100		100		100		100	ps	5,8,11,18
TCCJ	CPUT/C Cycle to Cycle Jitter		150		150		150		150	ps	5,8,11,18
Vcross	Crossing Point Voltage	510	760	510	760	510	760	510	760	mV	27
SE-DeltaSlew	Absolute Single-ended Rise/Fall Waveform Symmetry		325		325		325		325	ps	26
K7 Mode											
TDC	CPUOD_T/C Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	CPUOD_T/C Period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	ns	4,5,7
TLOW	CPUOD_T/C LOW Time	2.8		2.8		1.67		2.8		ns	4,5,7
Tf	CPUOD_T/C Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	0.4	1.6	ns	4,5,6
TCCJ	CPUOD_T/C Cycle to Cycle Jitter		±250		±250		±250		±250	ps	5,7
VD	Differential Voltage AC	.4	Vp+.6V	.4	Vp+.6V	.4	Vp+.6V	.4	Vp+.6V	V	17
VX	Differential Crossover Voltage	500	1100	500	1100	500	1100	500	1100	mV	16
Chipset											
TDC	CPUCS_T/C Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	CPUCS_T/C Period	15	15.5	10.0	10.5	7.35	7.65	4.85	5.1	ns	4,5,7
Tr / Tf	CPUCS_T/C Rise and Fall Times	0.4	1.6	0.4	1.6	0.4	1.6	0.4	1.6	ns	4,5,6
VD	Differential Voltage AC	0.4	Vp+.6V	0.4	Vp+.6V	0.4	Vp+.6V	0.4	Vp+.6V	V	19
VX	Differential Crossover Voltage	0.5*VD-DI-0.2	0.5*VD-DI+0.2	0.5*VD-DI-0.2	0.5*VD-DI+0.2	0.5*VD-DI-0.2	0.5*VD-DI+0.2	0.5*VD DI-0.2	0.5*VD-DI+0.2	V	18
AGP											
TDC	AGP(0:2) Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	AGP(0:2) Period	15	16	15	16	15	16	15	16	ns	4,5,7
THIGH	AGP(0:2) HIGH Time	5.25		5.25		5.25		5.25		ns	5,9

Notes:

19. Measured at VX between the falling edge and the following rising edge of the signal.
20. This parameter is intended to be 0.45*Tperiod(min) for minimum spec. and 0.55*Tperiod(min) for maximum spec.
21. Measured from Vol = 0.175V to Voh = 0.525V.
22. See figure 6 for 0.7V loading specification.
23. Determined as a fraction of 2*(Trise-Tfall)/(Trise+Tfall).
24. Measurement taken from differential waveform, from -0.35V to +0.35V.
25. Measurements taken from common mode waveforms, measure rise/fall time from 0.41V to 0.86V. Rise/fall time matching is defined a s " the instantaneous difference between maximum CLK rise (fall) and minimum CLK# fall (rise) time, or minimum clk rise (fall) and maximum clk# fall (rise) time." This parameter is designed for waveform symmetry.
26. Measured in absolute voltage, i.e., single-ended measurement.
27. Ideally the probes should be placed on the pins. If there is a transmission line between the test point and the pin for one signal of the pair (e.g., CPU), you should add the same length transmission line to the other signal of the pair (e.g., AGP).

AC Parameters (continued)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	M.ax	Min.	Max.		
TLOW	AGP(0:2) LOW Time	5.05		5.05		5.05		5.05		ns	5,10
Tr / Tf	AGP(0:2) Rise and Fall Times	0.4	1.6	0.4	1.6	0.4	1.6	0.4	1.6	ns	5,6
TSKEW	Any AGP to Any AGP Clock Skew		250		250		250		250	ps	5,8,11
TCCJ	AGP(0:2) Cycle to Cycle Jitter		500		500		500		500	ps	5,7,8,11
PCI											
TDC	PCI(_F,1:6) Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	PCI(_F,1:6) Period	30.0		30.0		30.0		30.0		ns	4,5,7
THIGH	PCI(_F,1:6) HIGH Time	12.0		12.0		12.0		12.0		ns	5,9
TLOW	PCI(_F,1:6) LOW Time	12.0		12.0		12.0		12.0		ns	5,10
Tr / Tf	PCI(_F,1:6) Rise and Fall Times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	ns	5,6
TSKEW	Any PCI to Any PCI clock Skew		500		500		500		500	ps	5,8,11
TCCJ	PCI(_F,1:6) Cycle to Cycle Jitter		500		500		500		500	ps	5,7,8,11
48 MHz											
TDC	48 MHz Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	48 MHz period	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	ns	4,5,7
Tr / Tf	48 MHz rise and fall times	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns	5,6
TCCJ	48 MHz Cycle to Cycle Jitter		500		500		500		500	ps	5,7,8,11
24 MHz											
TDC	24 MHz Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	24 MHz Period	41.660	41.667	41.660	41.667	41.660	41.667	41.660	41.667	ns	4,5,7
Tr / Tf	24 MHz Rise and Fall Times	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns	5,6
TCCJ	24 MHz Cycle to Cycle Jitter		500		500		500		500	ps	5,7,8,11
REF											
TDC	REF Duty Cycle	45	55	45	55	45	55	45	55	%	4,5,7
TPeriod	REF Period	69.8413	71.0	69.8413	71.0	69.8413	71.0	69.8413	71.0	ns	4,5,7
Tr / Tf	REF Rise and Fall Times	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns	5,6
TCCJ	REF Cycle to Cycle Jitter		1000		1000		1000		1000	ps	5,7,8,11
DDR											
VX	Crossing Point Voltage of DDRT/C	0.5*VDD-0.2	0.5*VDD+0.2	0.5*VDD-0.2	0.5*VDD+0.2	0.5*VDD-0.2	0.5*VDD+0.2	0.5*VDD-0.2	0.5*VDD+0.2	V	16
VD	Differential Voltage Swing	0.7	VDDD + 0.6	0.7	VDDD + 0.6	0.7	VDDD + 0.6	0.7	VDDD + 0.6	V	17
TDC	DDRT/C(0:5) Duty Cycle	45	55	45	55	45	55	45	55	%	18
TPeriod	DDRT/C(0:5) Period	14.85	15.3	9.85	10.2	14.85	15.3	9.85	10.2	ns	18
Tr / Tf	DDRT/C(0:5) Rise/Fall Slew Rate	1	3	1	3	1	3	1	3	V/ns	6
TSKEW	DDRT/C to Any DDRT/C Clock Skew		100		100		100		100	ps	5,8,18
TCCJ	DDRT/C(0:5) Cycle to Cycle Jitter		±75		±75		±75		±75	ps	5,8,18
THPJ	DDRT/C(0:5) Half Period Jitter		±100		±100		±100		±100	ps	5,8,18

AC Parameters (continued)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	M.ax	Min.	Max.		
TDelay	BUF_IN to Any DDRT/C Delay	1	4	1	4	1	4	1	4	ns	5,7
TSKEW	FBOUT to Any DDRT/C Skew		100		100		100		100	ps	5,7
tstable	All Clock Stabilization from Power-up		1.5		1.5		1.5		1.5	ms	11

Connection Circuit DDRT/C Signals

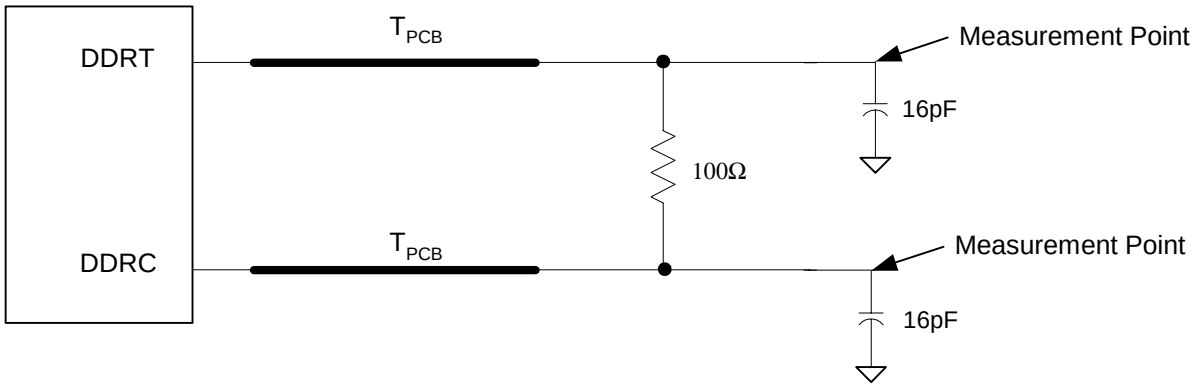


Figure 1. Differential DDR Termination

For Open Drain CPU Output Signals (with K7 Processor SELP4_K7# = 0)

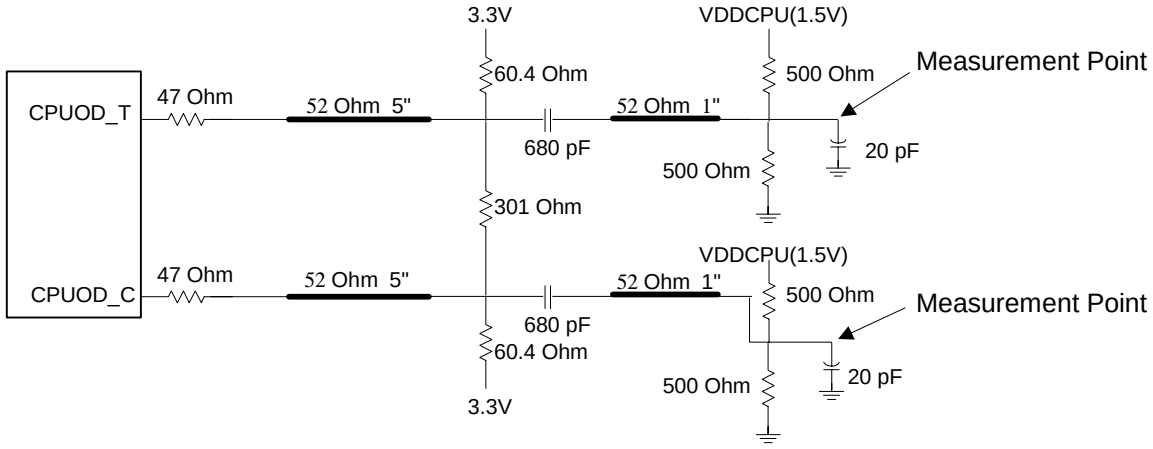


Figure 2. K7 Termination

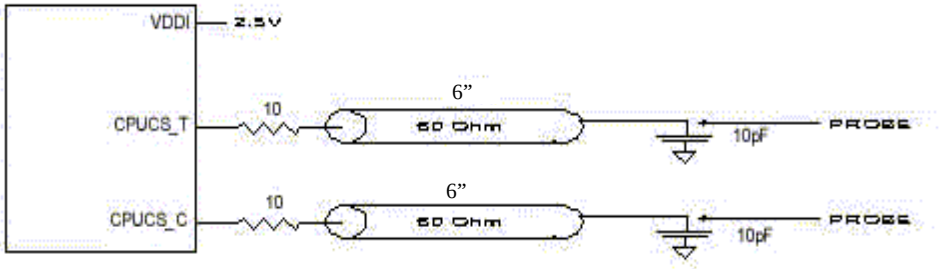


Figure 3. Chipset Termination

For Differential CPU Output Signals (with P4 Processor SELP4_K7#= 1)

The following diagram shows lumped test load configurations for the differential Host Clock Outputs. *Figure 4* is for the 1.0V amplitude signalling and *Figure 5* is for the 0.7 Volt amplitude signalling.

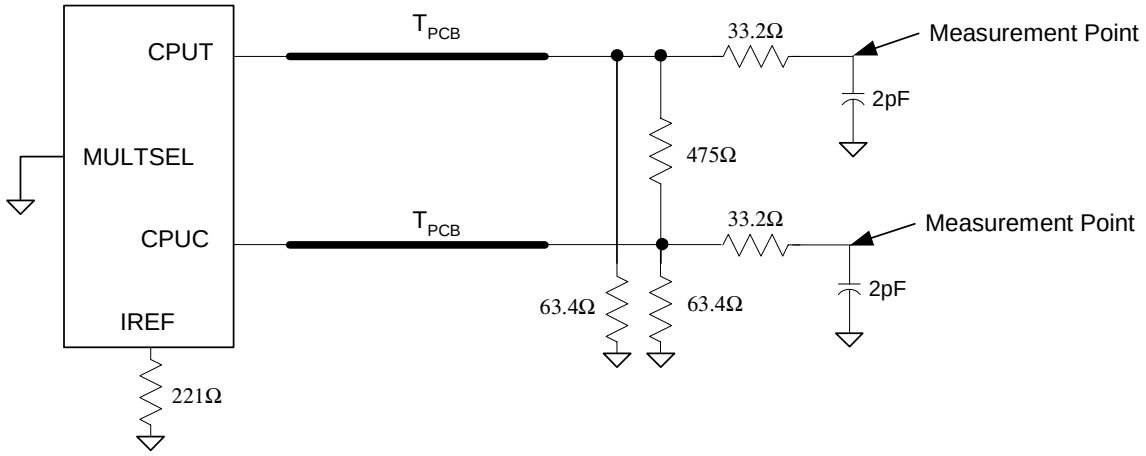


Figure 4. P4 1.0V Configuration

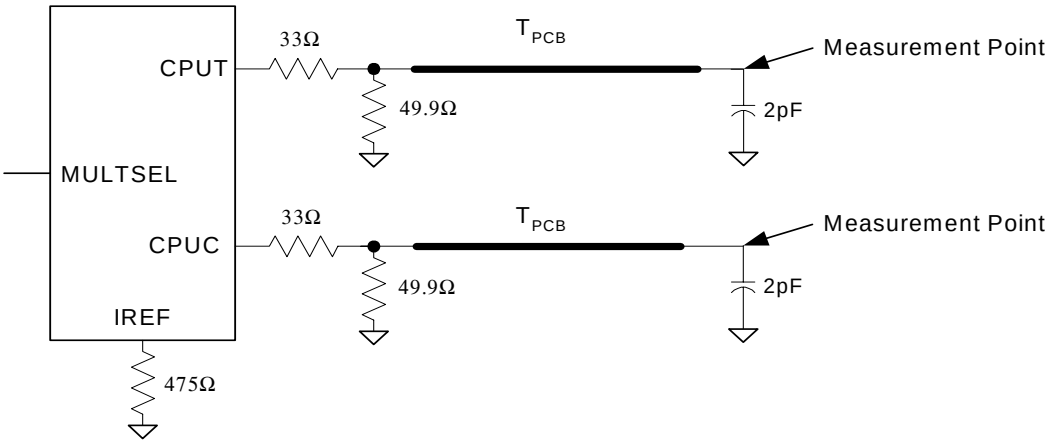


Figure 5. P4 0.7V Configuration

Table 10. Group Timing Relationships and Tolerances

		Offset (ps)	Tolerance (ps)	Conditions
t_{CSAGP}	CPUCS to AGP	750	500	CPUCS Leads
t_{AP}	AGP to PCI	500	500	AGP Leads

Table 11. Signal Loading

Clock Name	Max Load (in pF)
REF (0:1), 48MHz (USB), 24_48MHz	20
AGP(0:2), PCI_F(0:5)SDRAM (0:11)	30
FBOUT	10
DDRT/C	See *Figure 1*
CPUT/C	See *Figure 4* and *Figure 5*
CPUOD_T/C	See *Figure 2*
CPUCS_T/C	See *Figure 3*

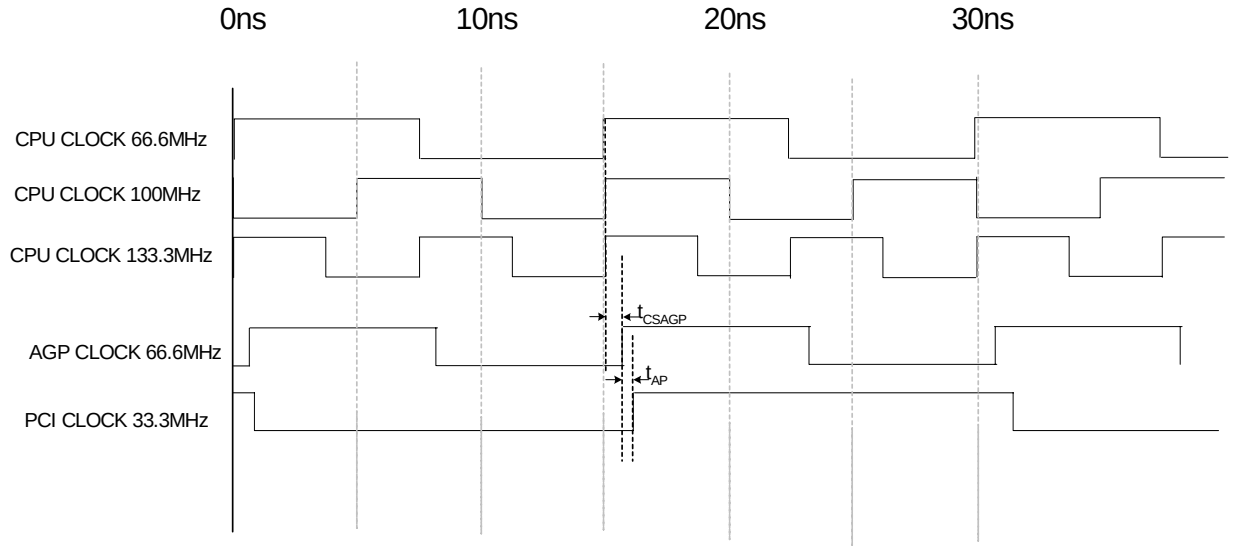


Figure 6. Clock Timing Relationships

CPU_STP# Assertion (P4 Mode)

When CPU_STP# pin is asserted, all CPU outputs will be stopped after being sampled by two rising CPUC clock edges. The final state of the stopped CPU signal is CPUT = HIGH and CPUC = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to (Mult 0 “select”) x (Iref), and the CPUC signal will not be driven. Due to external pulldown circuitry CPUC will be LOW during this stopped state.

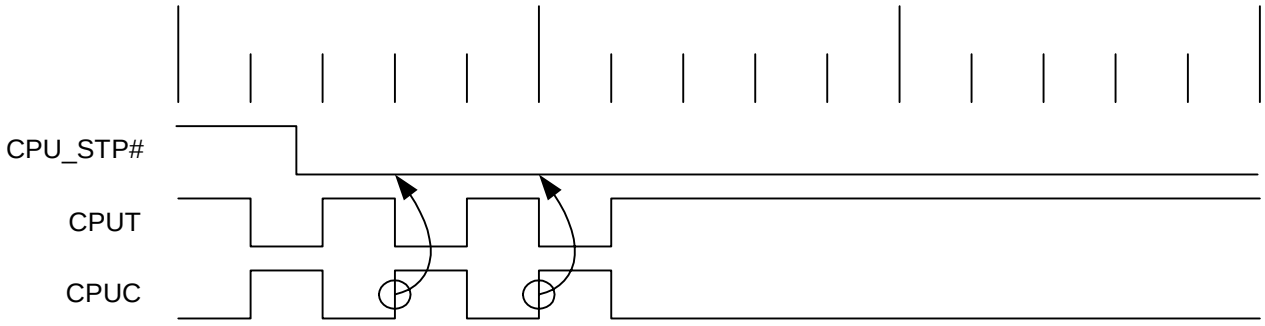


Figure 7. CPU_STP# Assertion Waveform (P4 Mode)

Table 12. CPU_STP# Functionality

CPU_STP#	CPU#4	CPU
1	Normal	Normal
0	Iref*Mult	Float

CPU_STP# Deassertion (P4 Mode)

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the de-assertion to active outputs is no more than two CPU clock cycles.

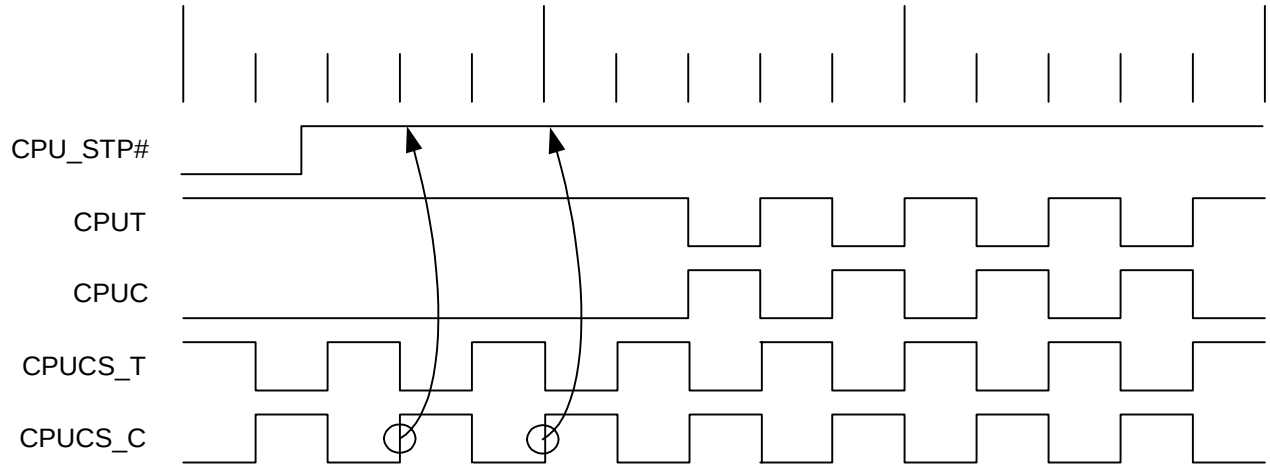


Figure 8. CPU_STP# Deassertion Waveform (P4 Mode)

CPU_STP# Assertion (K7 Mode)

When CPU_STP# pin is asserted, all CPU outputs will be stopped after being sampled by two rising CPUC clock edges. The final state of the stopped CPU signal is CPUOD_T = LOW and CPUOD_C = LOW.

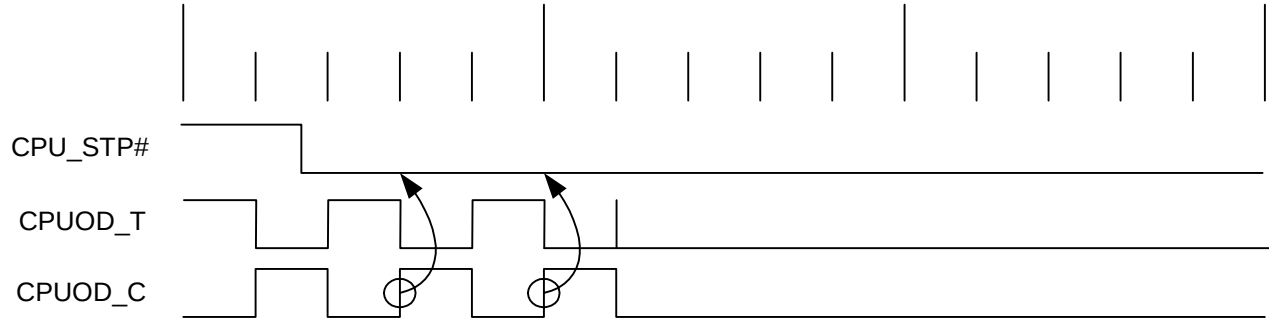


Figure 9. CPU_STP# Assertion Waveform (K7 Mode)

CPU_STP# Deassertion (K7 Mode)

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

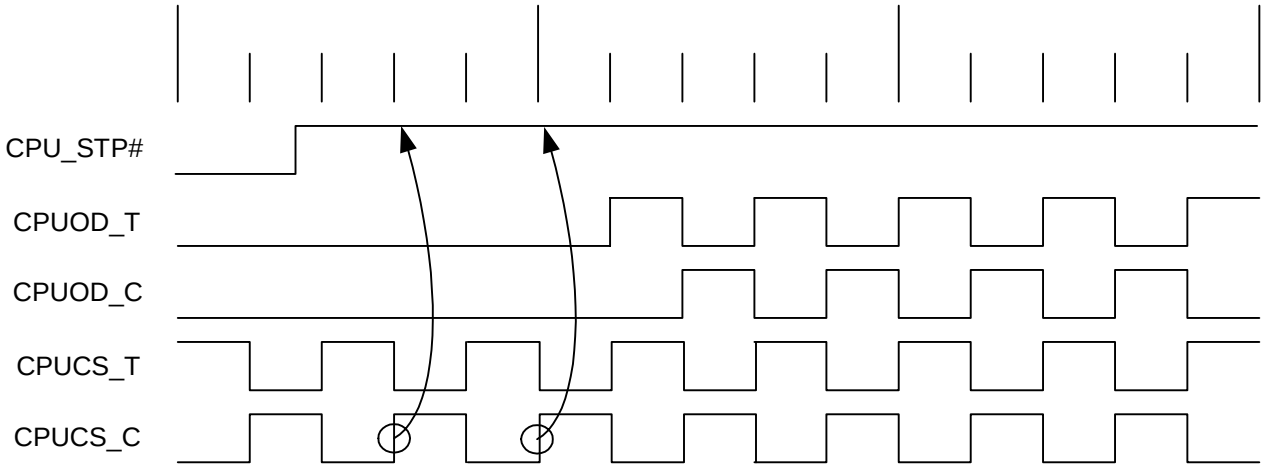


Figure 10. CPU_STP# Deassertion Waveform (K7 Mode)

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The setup time for capturing PCI_STP# going LOW is 10nsec (t_{setup}). The PCI_F clock will not be affected by this pin.

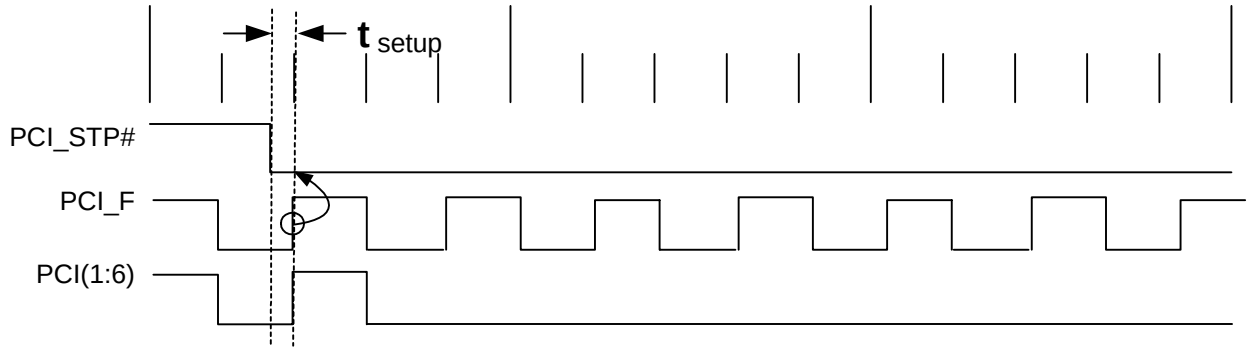


Figure 11. PCI_STP# Assertion Waveform

PCI_STP#- Deassertion

The deassertion of the PCI_STP# signal will cause all PCI clocks to resume running in a synchronous manner within one PCI clock period after PCI_STP# transitions to a HIGH level.

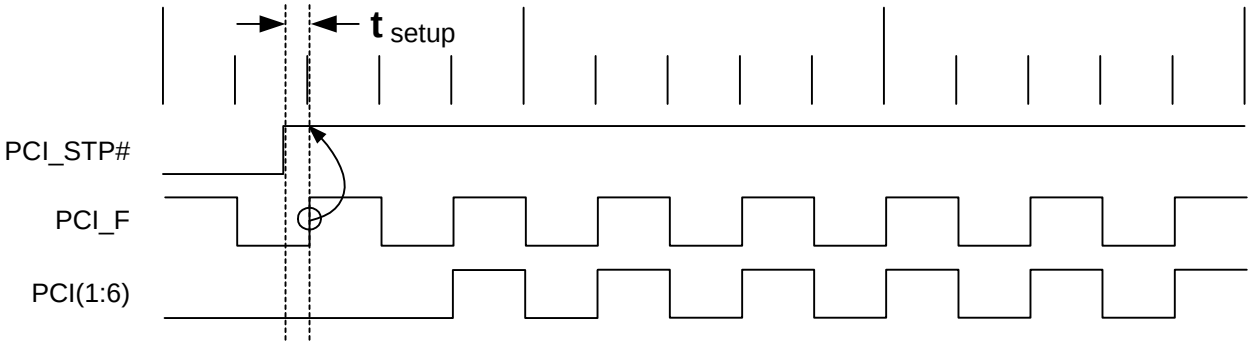


Figure 12. PCI_STP# Deassertion Waveform

Power Management Functions

All clocks can be individually enabled or stopped via the 2-wire control interface. All clocks maintain a valid HIGH period on transitions from running to stop and on transitions from stopped to running when the chip was not powered OFF.

Power Down Assertion (P4 Mode)

When PD# is sampled LOW by two consecutive rising edges of CPUC clock then all clocks must be held LOW on their next HIGH to LOW transition. CPUT clocks must be held with a value of 2 x Iref,

P4 Processor SELP4_K7# = 1.

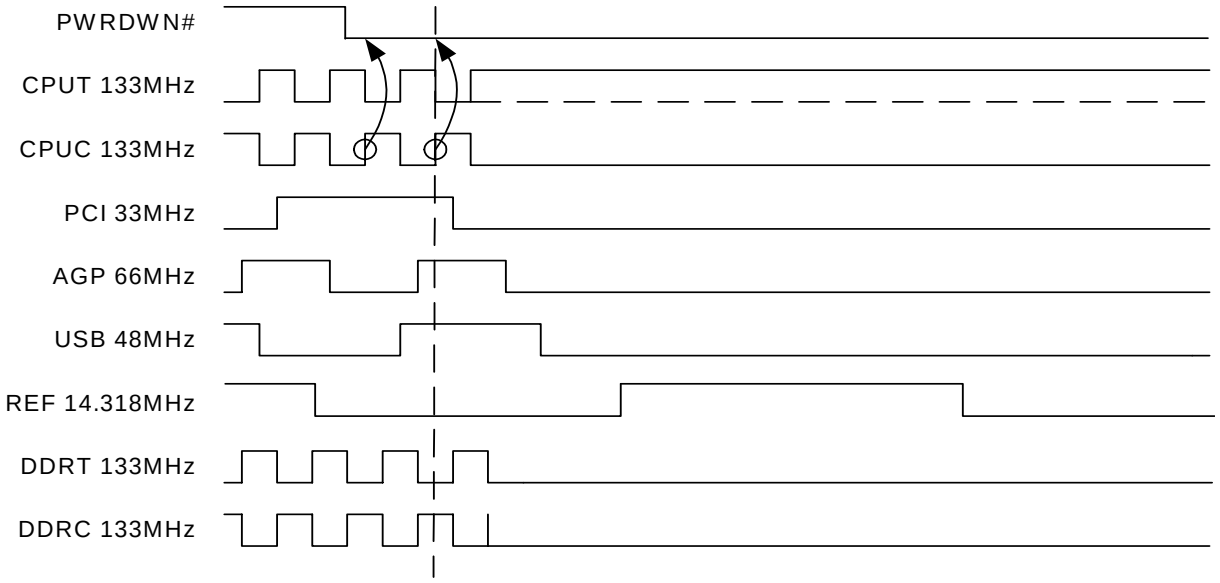


Figure 13. Power Down Assertion Timing Waveform (in P4 Mode)

Power-down Deassertion (P4 Mode)

The power-up latency needs to less than 1.5mS.

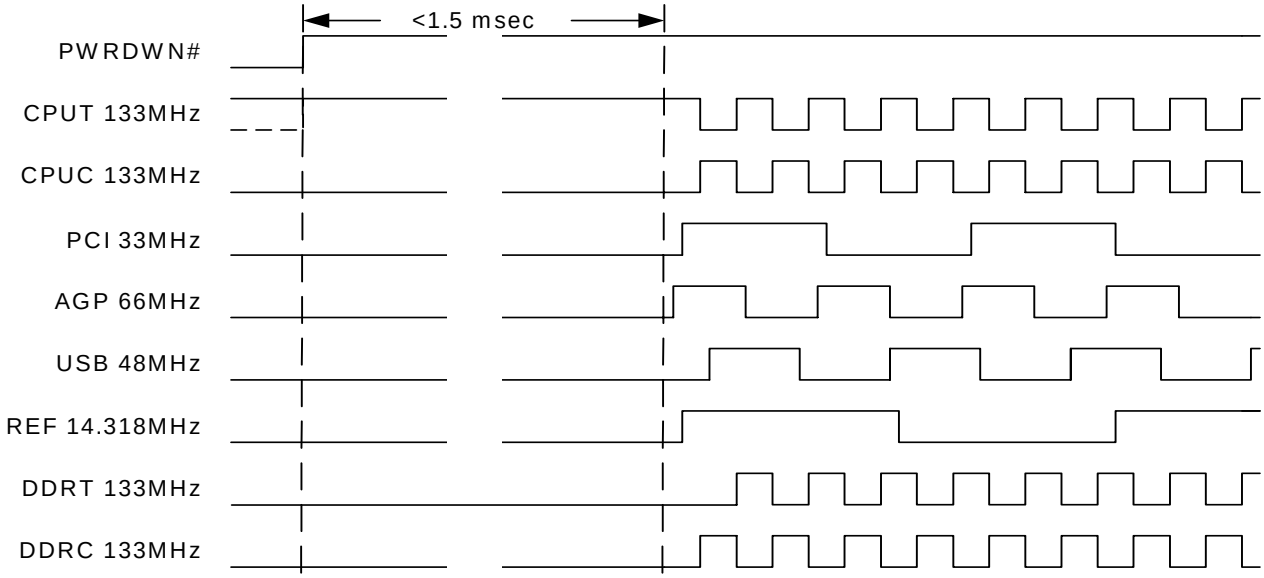


Figure 14. Power-down Deassertion Timing Waveform (in P4 Mode)

AMD K7 processor SELP4_K7# = 0

Power-down Assertion (K7 Mode)

When the PD# signal is asserted LOW, all clocks are disabled to a LOW level in an orderly fashion prior to removing power from the CPU. When PD# is sampled LOW by two consecutive rising edges of the CPUCS_C clock, then all affected clocks are stopped in a LOW state after the next HIGH to LOW transition or remains LOW. When in power-down (and before power is removed), all outputs are synchronously stopped in a LOW state (see *Figure 15* below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I2C function is also disabled.

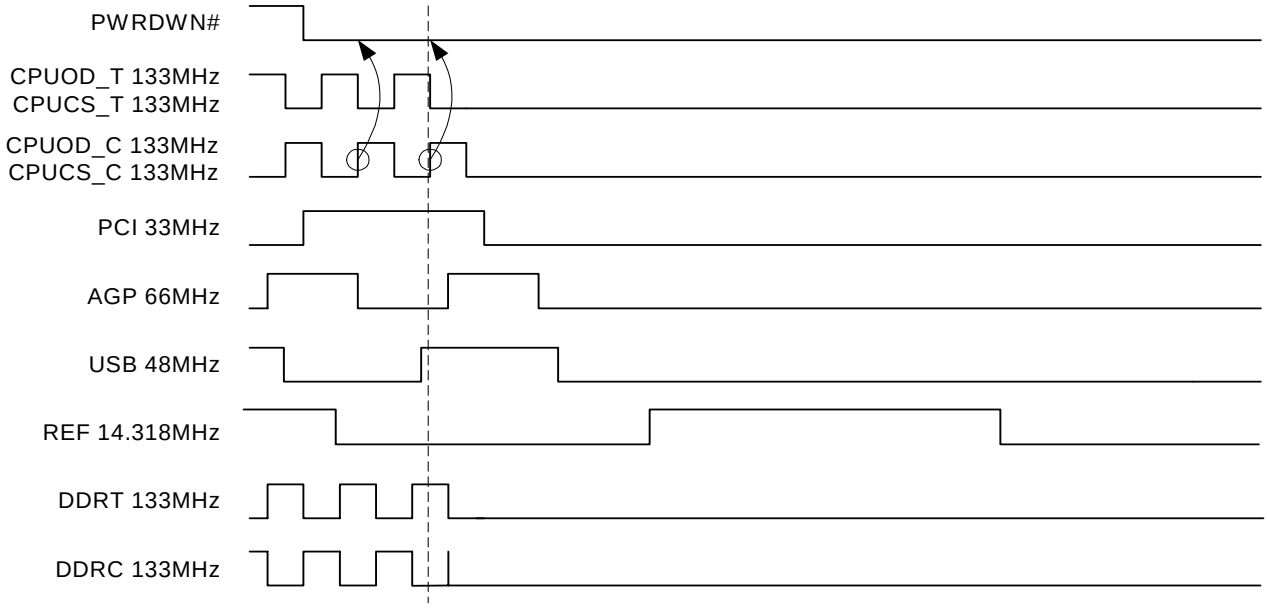


Figure 15. Power-down Assertion Timing Waveform (in K7 Mode)

Power Down Deassertion (K7 Mode)

When deasserted PD# to HIGH level, all clocks are enabled and start running on the rising edge of the next full period in order to guarantee a glitch-free operation, no partial clock pulses.

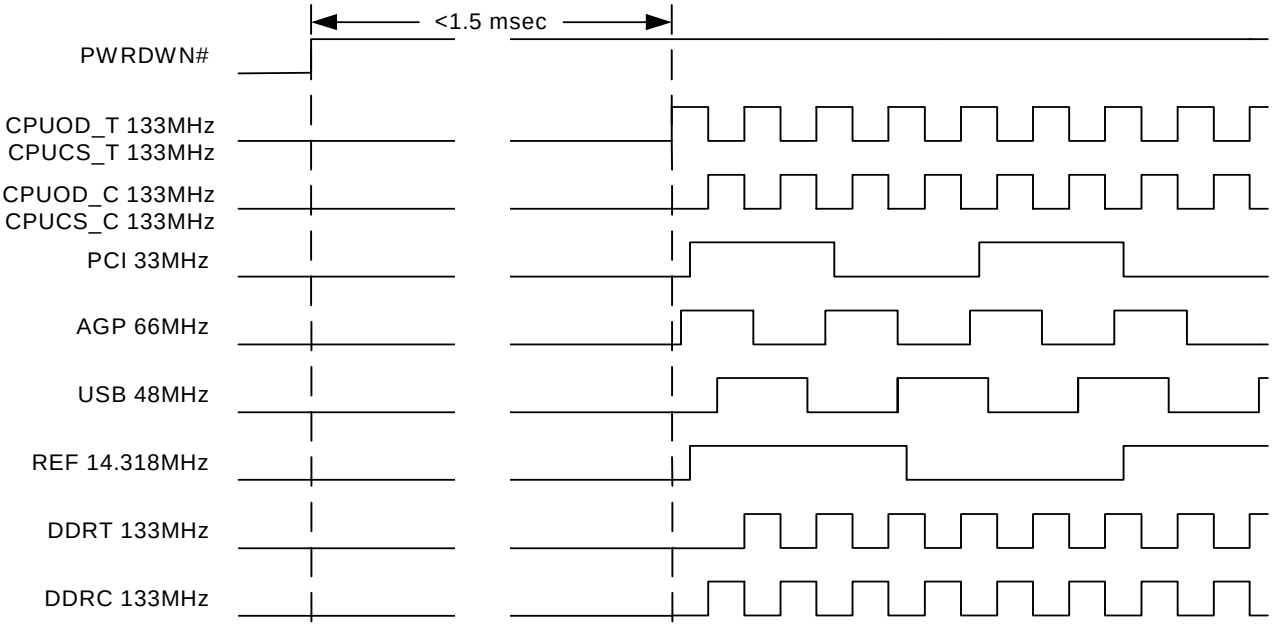


Figure 16. Power-down Deassertion Timing Waveform (in K7 Mode)

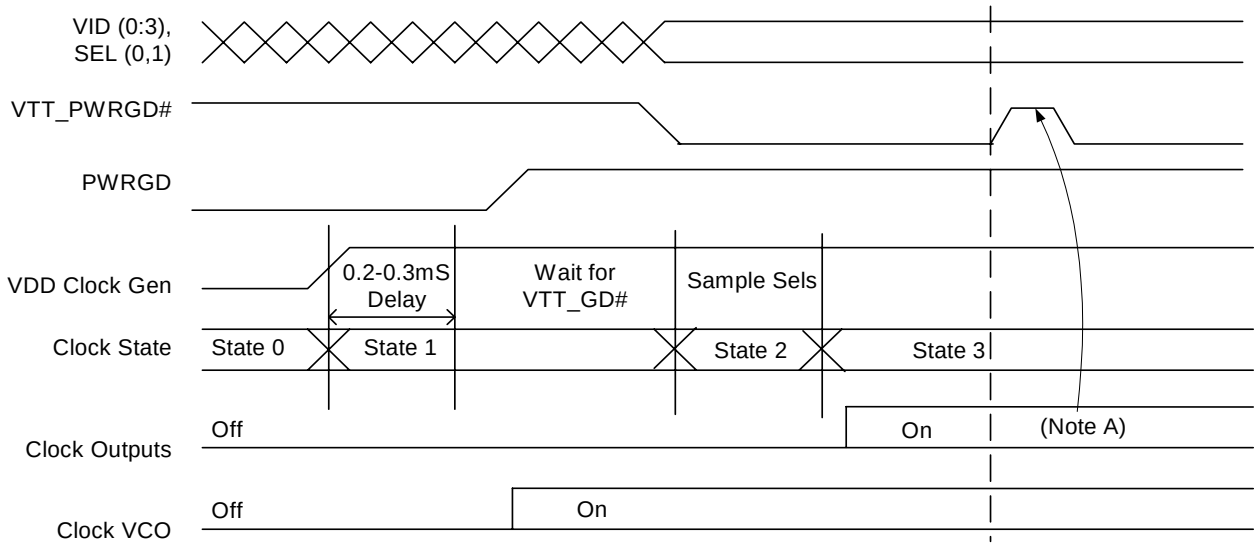


Figure 17. VTT_PWGD# Timing Diagram (With Advanced PIII Processor SELP4_K7# = 1)[28]

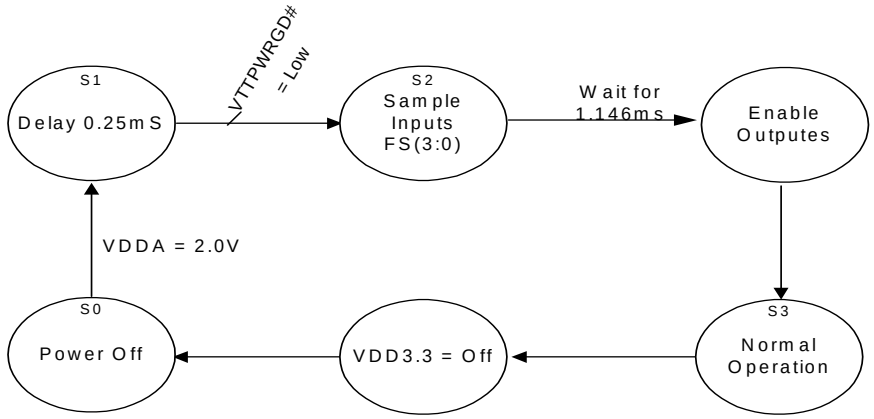


Figure 18. Clock Generator Power-up/Run State Diagram (with P4 Processor SELP4_K7# = 1)

Ordering Information

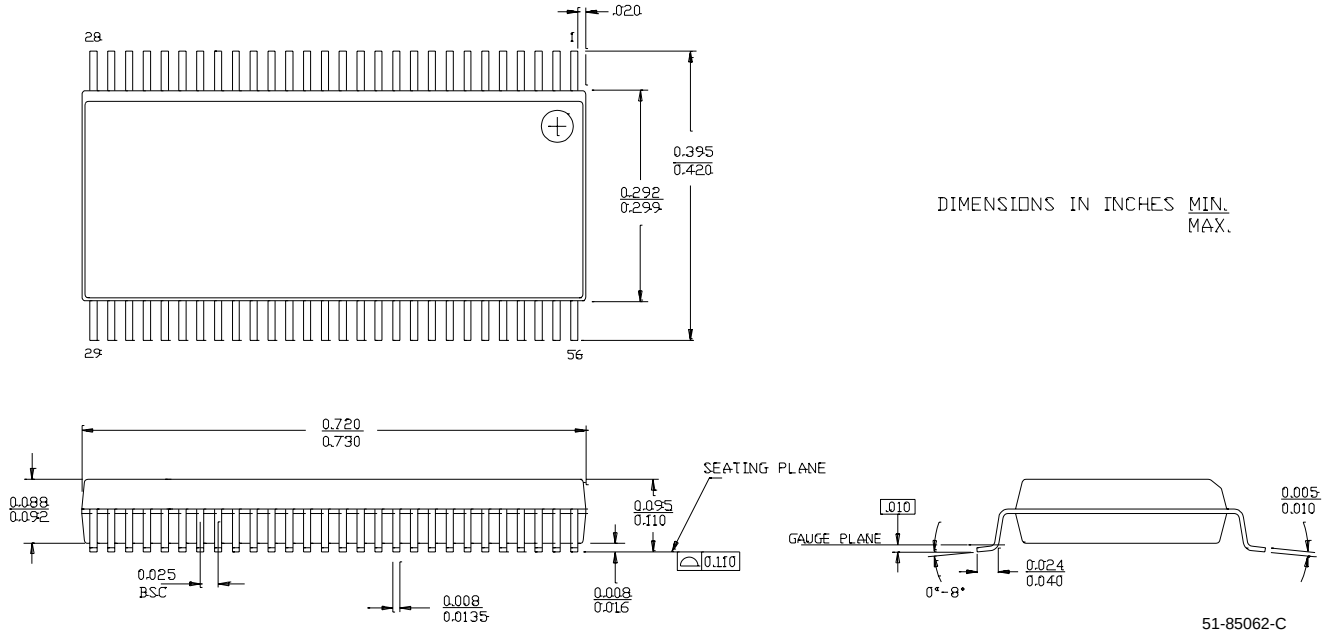
Part Number	Package Type	Product Flow
CY28347OC	56-pin Shrunk Small Outline Package (SSOP)	Commercial, 0° to 70°C
CY28347OCT	56-pin Shrunk Small Outline Package (SSOP)-Tape and Reel	Commercial, 0° to 70°C
CY28347ZC	56-pin Thin Shrunk Small Outline package (TSSOP)	Commercial, 0° to 70°C
CY28347ZCT	56-pin Thin Shrunk Small Outline package (TSSOP)-Tape and Reel	Commercial, 0° to 70°C

Note:

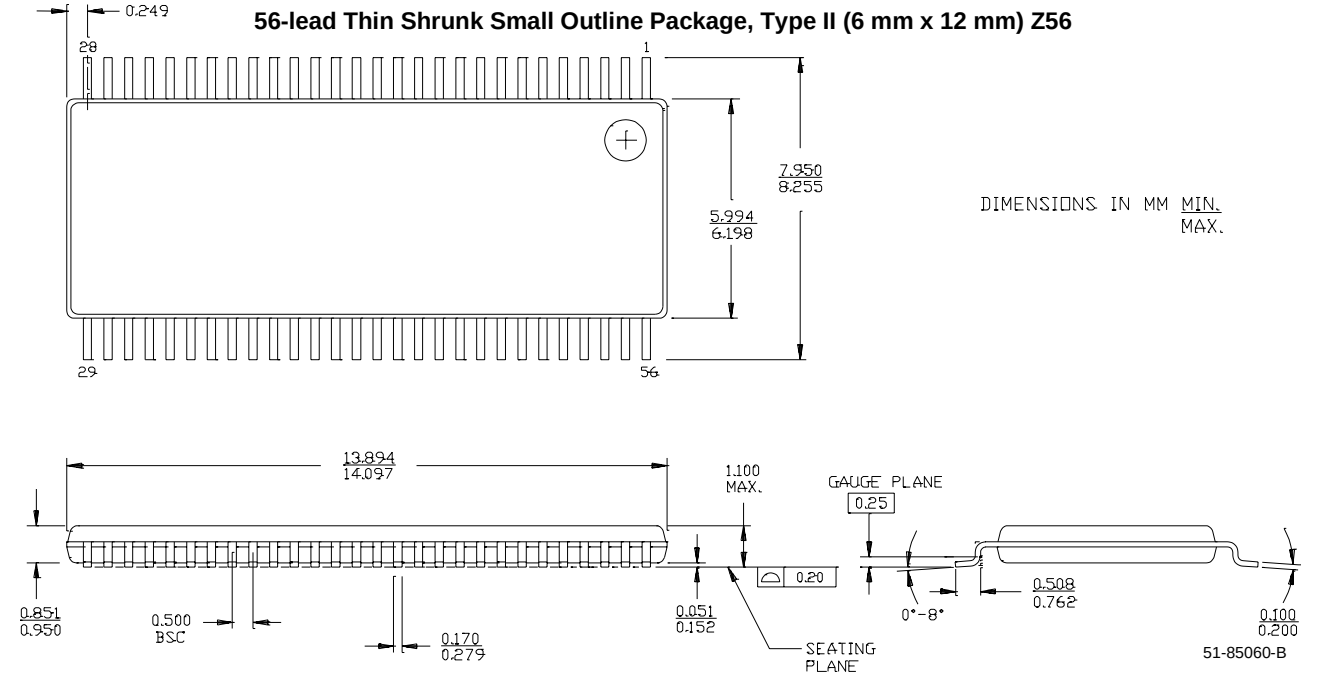
28. This time diagram shows that VTT_PWRGD# transits to a logic LOW in the first time at power up. After the first HIGH to LOW transition of VTT_PWRGD#, device is not affected, VTT_PWRGD# is ignored.

Package Drawing and Dimensions

56-lead Shrunk Small Outline Package O56



56-lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



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