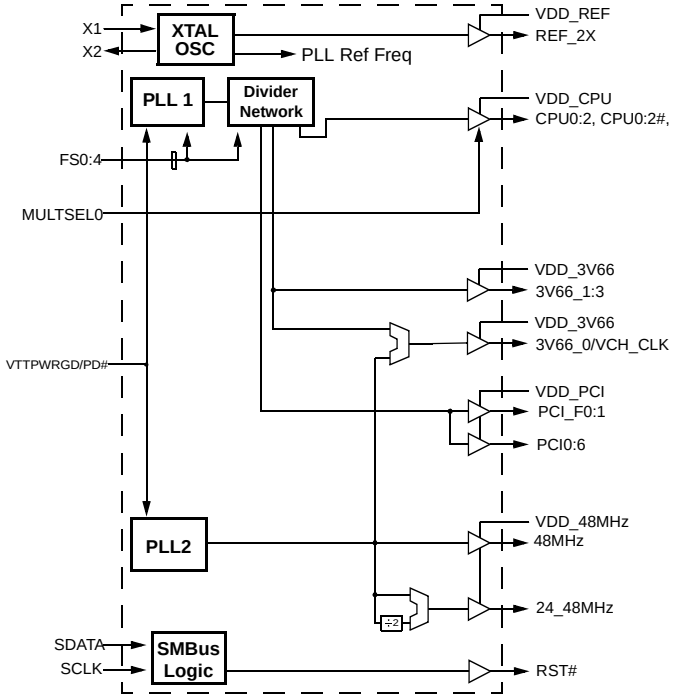
FTG for Intel Pentium 4 CPU and Chipsets

Features

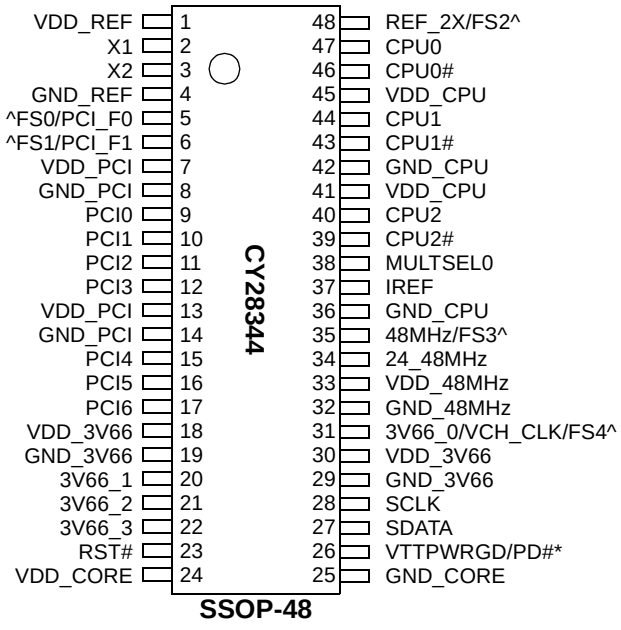
- **Compatible to Intel® CK-Titan and CK-408 Clock Synthesizer/Driver Specifications**
- **System frequency synthesizer for Intel Brookdale (845) and Brookdale G Pentium® 4 Chipsets**
- **Programmable clock output frequency with less than 1MHz increment**
- **Integrated fail-safe Watchdog timer for system recovery**
- **Automatically switch to HW-selected or SW-programmed clock frequency when Watchdog timer time-out**
- **Capable of generating system RESET after a Watchdog timer time-out occurs or a change in output frequency via SMBus interface**
- **Support SMBus byte Read/Write and block Read/Write operations to simplify system BIOS development**
- **Vendor ID and Revision ID support**
- **Programmable drive strength support**
- **Programmable output skew support**
- **Power management control inputs**
- **Available in 48-pin SSOP**

CPU	3V66	PCI	REF	48M
×3	×4	×9	×1	×2

Block Diagram



Pin Configuration[1]



SSOP-48

Note:

1. Signals marked with "*" and "^," respectively, have internal pull-up and pull-down resistors.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
X1	2	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	3	O	***Crystal Connection:*** Connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
REF_2X/FS2	48	I/O	***Reference Clock/Frequency Select 2:*** 3.3V 14.318-MHz clock output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table.
MULTSEL0	38	I	***Current Multiplier Selection 0:*** 3.3V input to select the current multiplier for CPU clock outputs. The MULTSEL0 is as follows: MULTSEL0 0 = Ioh is 4 × IREF 1 = Ioh is 6 × IREF
CPU0:2, CPU0:2#	47, 44, 40, 46, 43,39	O	***CPU Clock Outputs:*** Frequency is set by the FS0:4 inputs or through serial input interface.
3V66_1:3	20, 21, 22	O	***66MHz Clock Outputs:*** 3.3V 66-MHz clock.
3V66_0/VCH_CLK/FS4	31	I/O	***66MHz Clock Output/Frequency Select 4:*** 3.3V 66-MHz or 48-MHz clock output. The selection is determined by the control byte register. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table.
PCI_F0/FS0	5	I/O	***Free-running PCI Output 0/Frequency Select 0:*** 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table.
PCI_F1/FS1	6	I/O	***Free-running PCI Output 1/Frequency Select 1:*** 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table.
PCI0:6	9, 10, 11, 12, 15, 16, 17	O	***PCI Clock Output 0 to 6:*** 3.3V PCI clock outputs.
48MHz/FS3	35	I/O	***48MHz Output/Frequency Select 3:*** 3.3V fixed 48-MHz, non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table.
24_48MHz	34	I/O	***24 or 48MHz Output:*** 3.3V fixed 24-MHz or 48-MHz non-spread spectrum output.
SCLK	28	I	***SMBus Clock Input:*** Clock pin for serial interface.
SDATA	27	I/O	***SMBus Data Input:*** Data pin for serial interface.
RST#	23	O (open-drain)	***System Reset Output:*** Open-drain system reset output.
IREF	37	I	***Current Reference for CPU output:*** A precision resistor is attached to this pin, which is connected to the internal current reference.
VTT_PWRGD/PD#	26	I	***Powergood from Voltage Regulator Module (VRM)/PD#:*** 3.3V LVTTL input. VTT_PWRGD# is a level sensitive strobe used to determine when FS0:4 and MULTSEL0 inputs are valid and OK to be sampled (Active HIGH).
VDD_REF, VDD _PCI, VDD_48MHz, VDD_3V66, VDD_CPU	1, 7, 13, 18, 30, 33, 41, 45	P	***3.3V Power Connection:*** Power supply for CPU outputs buffers, 3V66 output buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V.
VDD_48MHz	33	P	***3.3V Power Connection:*** 48MHz output buffers. Connect to 3.3V.
GND_PCI, GND_48MHz, GND_3V66, GND_CPU, GND_REF,	4, 8, 14, 19, 29, 32, 36, 42	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Pin Definitions (continued)

Pin Name	Pin No.	Pin Type	Pin Description
VDD_CORE	24	P	***3.3V Analog Power Connection:*** Power supply for core logic, PLL circuitry. Connect to 3.3V.
GND_CORE	25	G	***Analog Ground Connection:*** Ground for core logic, PLL circuitry.

Swing Select Functions (SW control)

SW_MULTSEL1	SW_MULTSEL0	Board Target Trace/Term Z	Reference R, IREF = VDD/(3*Rr)	Output Current	V_{OH} @ Z
0	**0**	**50 Ohm**	**Rr = 221 1%, IREF = 5.00 mA**	**I_{OH} = 4*Iref**	**1.0V @ 50**
0	0	60 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 4*Iref	1.2V @ 60
0	1	50 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 5*Iref	1.25V @ 50
0	1	60 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 5*Iref	1.5V @ 60
1	0	50 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 6*Iref	1.5V @ 50
1	0	60 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 6*Iref	1.8V @ 60
1	1	50 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 7*Iref	1.75V @ 50
1	1	60 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 7*Iref	2.1V @ 60
0	0	50 Ohm	Rr = 475 1%, IREF = 2.32 mA	I_{OH} = 4*Iref	0.47V @ 50
0	0	60 Ohm	Rr = 475 1%, IREF = 2.32 mA	I_{OH} = 4*Iref	0.56V @ 60
0	1	50 Ohm	Rr = 475 1%, IREF = 2.32 mA	I_{OH} = 5*Iref	0.58V @ 50
0	**1**	**60 Ohm**	**Rr = 475 1%, IREF = 2.32 mA**	**I_{OH} = 5*Iref**	**0.7V @ 60**
1	**0**	**50 Ohm**	**Rr = 475 1%, IREF = 2.32 mA**	**I_{OH} = 6*Iref**	**0.7V @ 50**
1	0	60 Ohm	Rr = 475 1%, IREF = 2.32 mA	I_{OH} = 6*Iref	0.84V @ 60
1	1	50 Ohm	Rr = 475 1%, IREF = 2.32 mA	I_{OH} = 7*Iref	0.81V @ 50
1	**1**	**60 Ohm**	**Rr = 475 1%, IREF = 2.32 mA**	**I_{OH} = 7*Iref**	**0.97V @ 60**

Swing Select Functions (HW control)

MULTSEL0	Board Target Trace/Term Z	Reference R, IREF = VDD/(3*Rr)	Output Current	V_{OH} @ Z
0	**50 Ohm**	**Rr = 221 1%, IREF = 5.00 mA**	**I_{OH} = 4*Iref**	**1.0V @ 50**
0	60 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 4*Iref	1.2V @ 60
1	50 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 6*Iref	1.5V @ 50
1	60 Ohm	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 6*Iref	1.8V @ 60

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc. can be individually enabled or disabled.

The registers associated with the Serial Data Interface initializes to it's default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte Write, byte Read, block Write and block Read operation from the controller. For block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte Write and byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block Write and block Read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte Write and byte Read protocol.

The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Descriptions
7	0 = Block Read or block Write operation 1 = Byte Read or byte Write operation
6:0	Byte offset for byte Read or byte Write operation. For block Read or block Write operations, these bits should be "0000000"

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bit	2:8	Slave address – 7 bit
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bit "00000000" stands for block operation	11:18	Command Code – 8 bit "00000000" stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave – 8 bits
...	Data Byte N – 8 bits	47	Acknowledge
...	Acknowledge from slave	48:55	Data byte from slave – 8 bits
...	Stop	56	Acknowledge
		...	Data bytes from slave/acknowledge
		...	Data byte N from slave – 8 bits
		...	Not acknowledge
		...	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bit	2:8	Slave address – 7 bit
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bit “1xxxxxxx” stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bit “1xxxxxxx” stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not acknowledge
		39	Stop

Data Byte Configuration Map

Data Byte 0

Bit	Pin#	Name	Description	Power On Default
Bit 7	--	SEL3	SW Frequency selection bits. See *Table 4*.	0
Bit 6	--	SEL2		0
Bit 5	--	SEL1		0
Bit 4	--	SEL0		0
Bit 3	--	FS_Override	0 = Select operating frequency by FS[4:0] input pins 1 = Select operating frequency by SEL[4:0] settings	0
Bit 2	--	SEL4	SW Frequency selection bits. See *Table 4*.	0
Bit 1	--	Spread Spectrum Enable	0 = OFF; 1 = Enabled	0
Bit 0	--	Reserved	Reserved	0

Data Byte 1

Bit	Pin#	Name	Description	Power On Default
Bit 7	40, 39	CPU2, CPU2#	(Active/Inactive)	1
Bit 6	44, 43	CPU1, CPU1#	(Active/Inactive)	1
Bit 5	47, 46	CPU0, CPU0#	(Active/Inactive)	1
Bit 4	--	Latched FS4 input	Latched FS[4:0] inputs. These bits are Read-only.	X
Bit 3	--	Latched FS3 input		X
Bit 2	--	Latched FS2 input		X
Bit 1	--	Latched FS1 input		X
Bit 0	--	Latched FS0 input		X

Data Byte 2

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Reserved	Reserved	0
Bit 6	17	PCI6	(Active/Inactive)	1
Bit 5	16	PCI5	(Active/Inactive)	1
Bit 4	15	PCI4	(Active/Inactive)	1
Bit 3	12	PCI3	(Active/Inactive)	1
Bit 2	11	PCI2	(Active/Inactive)	1
Bit 1	10	PCI1	(Active/Inactive)	1
Bit 0	9	PCI0	(Active/Inactive)	1

Data Byte 3

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	34	24_48MHz	(Active/Inactive)	1
Bit 6	35	48MHz	(Active/Inactive)	1
Bit 5	--	Reserved	Reserved	0
Bit 4	--	Reserved	Reserved	0
Bit 3	31	3V66_0/VCH_CLK	0 = 66 MHz; 1 = 48 MHz	0
Bit 2	31	3V66_0/VCH_CLK	(Active/Inactive)	1
Bit 1	6	PCI_F1	(Active/Inactive)	1
Bit 0	5	PCI_F0	(Active/Inactive)	1

Data Byte 4

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	MULTSEL_Override	This bit control the selection of IREF multiple. 0 = HW control; IREF multiplier is determined by MULTSEL[0:1] input pins 1 = SW control; IREF multiplier is determined by Byte[4], Bit[5:6].	0
Bit 6	--	SW_MULTSEL1	IREF multiplier 00 = Ioh is 4 × IREF 01 = Ioh is 5 × IREF 10 = Ioh is 6 × IREF 11 = Ioh is 7 × IREF	0
Bit 5	--	SW_MULTSEL0		0
Bit 4	48	REF_2X	(Active/Inactive) Drive	1
Bit 3	--	REF_DRV	0 = Normal, 1 = HIGH	0
Bit 2	22	3V66_3	(Active/Inactive)	1
Bit 1	21	3V66_2	(Active/Inactive)	1
Bit 0	20	3V66_1	(Active/Inactive)	1

Data Byte 5

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Spread Option 1	“00” = ± 0.25% “01” = – 0.5% “10” = ±0.5% “11” = ±0.38%	0
Bit 6	--	Spread Option 0		0
Bit 5	--	Reserved	Reserved	0
Bit 4	--	Reserved	Reserved	0
Bit 3	--	Reserved	Reserved	0
Bit 2	--	Reserved	Reserved	0
Bit 1	--	Reserved	Reserved	0
Bit 0	34	24_ 48MHZ	0 = 24 MHz 1 = 48 MHz	1

Data Byte 6

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7		Revision_ID3	Revision ID bit[3]	0
Bit 6		Revision_ID2	Revision ID bit[2]	0
Bit 5		Revision_ID1	Revision ID bit[1]	0
Bit 4		Revision_ID0	Revision ID bit[0]	0
Bit 3		Vendor_ID3	Bit[3] of Cypress Vendor ID. This bit is Read-only.	1
Bit 2		Vendor_ID2	Bit[2] of Cypress Vendor ID. This bit is Read-only.	0
Bit 1		Vendor _ID1	Bit[1] of Cypress Vendor ID. This bit is Read-only.	0
Bit 0		Vendor _ID0	Bit[0] of Cypress Vendor ID. This bit is Read-only.	0

Data Byte 7

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Reserved	Reserved	0
Bit 6	--	Reserved	Reserved	0
Bit 5	--	Reserved	Reserved	0
Bit 4	--	Reserved	Reserved	0
Bit 3	--	Reserved	Reserved	0
Bit 2	--	Reserved	Reserved	0
Bit 1	--	Reserved	Reserved	0
Bit 0	--	Reserved	Reserved	0

Data Byte 8

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Reserved	Reserved	0
Bit 6	--	Reserved	Reserved	0

Data Byte 8 (continued)

Bit	Pin#	Name	Pin Description	Power On Default
Bit 5	--	WD_TIMER4	These bits store the time-out value of the Watchdog timer. The scale of the timer is determine by the pre-scaler. The timer can support values from 150 ms – 4.8 sec when the pre-scaler is set to 150 ms. If the pre-scaler is set to 2.5 sec, it can support a value from 2.5 – 80 seconds. When the Watchdog timer reaches "0", it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled.	1
Bit 4	--	WD_TIMER3		1
Bit 3	--	WD_TIMER2		1
Bit 2	--	WD_TIMER1		1
Bit 1	--	WD_TIMER0		1
Bit 0	--	WD_PRE_SCALER	0 = 150 ms 1 = 2.5 sec	0

Data Byte 9

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	48MHz_DRV	48MHz and 24_48MHz clock output drive strength 0 = Normal 1 = High Drive	0
Bit 6	--	PCI_DRV	PCI clock output drive strength 0 = Normal 1 = High Drive	0
Bit 5	--	3V66_DRV	3V66 clock output drive strength 0 = Normal 1 = High Drive	0
Bit 4	--	RST_EN_WD	This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs. 0 = Disabled 1 = Enabled	0
Bit 3	--	RST_EN_FC	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled	0
Bit 2	--	WD_TO_STATUS	Watchdog Timer Time-out Status bit 0 = No time-out occurs (Read); Ignore (Write) 1 = time-out occurred (Read); Clear WD_TO_STATUS (Write)	0
Bit 1	--	WD_EN	0 = Stop and re-load Watchdog timer 1 = Enable Watchdog timer. It will start counting down after a frequency change occurs. **Note**: CY28344 will generate system reset, reload a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog timer time-out occurs. Under recovery frequency mode, CY28344 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28344 from its recovery frequency mode by clearing the WD_EN bit.	0
Bit 0	--	Reserved	Reserved	0

Data Byte 10

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	CPU_Skew2	CPU skew control 000 = Normal 001 = –150 ps 010 = –300 ps 011 = –450 ps 100 = +150 ps 101 = +300 ps 110 = +450 ps 111 = +600 ps	0
Bit 6	--	CPU_Skew1		0
Bit 5	--	CPU_Skew0		0
Bit 4	--	Reserved	Reserved	0
Bit 3	--	PCI_Skew1	PCI skew control 00 = Normal 01 = –500 ps 10 = Reserved 11 = +500 ps	0
Bit 2	--	PCI_Skew0		0
Bit 1	--	3V66_Skew1	3V66 skew control 00 = Normal 01 = –150 ps 10 = +150 ps 11 = +300 ps	0
Bit 0	--	3V66_Skew0		0

Data Byte 11

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	ROCV_FREQ_N7	If ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When FS_Override bit is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.	0
Bit 6	--	ROCV_FREQ_N6		0
Bit 5	--	ROCV_FREQ_N5		0
Bit 4	--	ROCV_FREQ_N4		0
Bit 3	--	ROCV_FREQ_N3		0
Bit 2	--	ROCV_FREQ_N2		0
Bit 1	--	ROCV_FREQ_N1		0
Bit 0	--	ROCV_FREQ_N0		0

Data Byte 12

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	ROCV_FREQ_SEL	ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL. 0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]	0

Data Byte 12 (continued)

Bit	Pin#	Name	Pin Description	Power On Default
Bit 6	--	ROCV_FREQ_M6	If ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency.when a Watchdog timer time-out occurs. The setting of FS_Override bit determine the frequency ratio for CPU and other output clocks. When FS_Override bit is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.	0
Bit 5	--	ROCV_FREQ_M5		0
Bit 4	--	ROCV_FREQ_M4		0
Bit 3	--	ROCV_FREQ_M3		0
Bit 2	--	ROCV_FREQ_M2		0
Bit 1	--	ROCV_FREQ_M1		0
Bit 0	--	ROCV_FREQ_M0		0

Data Byte 13

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	CPU_FSEL_N7	If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.	0
Bit 6	--	CPU_FSEL_N6		0
Bit 5	--	CPU_FSEL_N5		0
Bit 4	--	CPU_FSEL_N4		0
Bit 3	--	CPU_FSEL_N3		0
Bit 2	--	CPU_FSEL_N2		0
Bit 1	--	CPU_FSEL_N1		0
Bit 0	--	CPU_FSEL_N0		0

Data Byte 14

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Pro_Freq_EN	Programmable output frequencies enabled 0 = disabled 1 = enabled	0
Bit 6	--	CPU_FSEL_M6	If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.	0
Bit 5	--	CPU_FSEL_M5		0
Bit 4	--	CPU_FSEL_M4		0
Bit 3	--	CPU_FSEL_M3		0
Bit 2	--	CPU_FSEL_M2		0
Bit 1	--	CPU_FSEL_M1		0
Bit 0	--	CPU_FSEL_M0		0

Data Byte 15

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Reserved	Reserved	0
Bit 6	--	Reserved	Reserved	0
Bit 5	--	Reserved	Reserved	0
Bit 4	--	Reserved	Reserved	0
Bit 3	--	Reserved	Reserved	0
Bit 2	--	Reserved	Reserved	0
Bit 1	--	Vendor Test Mode	Reserved. Write with “1”	1
Bit 0	--	Vendor Test Mode	Reserved. Write with “1”	1

Data Byte 16

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Reserved	Reserved	0
Bit 6	--	Reserved	Reserved	0
Bit 5	--	Reserved	Reserved	0
Bit 4	--	Reserved	Reserved	0
Bit 3	--	Reserved	Reserved	0
Bit 2	--	Reserved	Reserved	0
Bit 1	--	Reserved	Reserved	0
Bit 0	--	Reserved	Reserved	0

Data Byte 17

Bit	Pin#	Name	Pin Description	Power On Default
Bit 7	--	Reserved	Reserved	0
Bit 6	--	Reserved	Reserved	0
Bit 5	--	Reserved	Reserved	0
Bit 4	--	Reserved	Reserved	0
Bit 3	--	Reserved	Reserved	0
Bit 2	--	Reserved	Reserved	0
Bit 1	--	Reserved	Reserved	0
Bit 0	--	Reserved	Reserved	0

Table 4. Frequency Selection Table

Input Conditions					Output Frequency			
FS4	FS3	FS2	FS1	FS0				PLL Gear Constants (G)
SEL4 Bit[2]	SEL3 Bit[7]	SEL2 Bit[6]	SEL1 Bit[5]	SEL0 Bit[4]	CPU	3V66	PCI	
0	0	0	0	0	100.90	67.27	33.63	48.00741
0	0	0	0	1	100.00	66.67	33.33	48.00741
0	0	0	1	0	103.00	68.67	34.33	48.00741
0	0	0	1	1	105.00	70.00	35.00	48.00741
0	0	1	0	0	107.00	71.33	35.67	48.00741
0	0	1	0	1	109.00	72.67	36.33	48.00741
0	0	1	1	0	111.00	74.00	37.00	48.00741
0	0	1	1	1	114.00	76.00	38.00	48.00741
0	1	0	0	0	117.00	78.00	39.00	48.00741
0	1	0	0	1	120.00	80.00	40.00	48.00741
0	1	0	1	0	127.00	84.67	42.33	48.00741
0	1	0	1	1	130.00	86.67	43.33	48.00741
0	1	1	0	0	133.33	88.89	44.44	48.00741
0	1	1	0	1	170.00	56.67	28.33	48.00741
0	1	1	1	0	180.00	60.00	30.00	48.00741
0	1	1	1	1	190.00	63.33	31.67	48.00741
1	0	0	0	0	133.90	66.95	33.48	48.00741
1	0	0	0	1	133.33	66.67	33.33	48.00741
1	0	0	1	0	120.00	60.00	30.00	48.00741
1	0	0	1	1	125.00	62.50	31.25	48.00741
1	0	1	0	0	134.90	67.45	33.73	48.00741
1	0	1	0	1	137.00	68.50	34.25	48.00741
1	0	1	1	0	139.00	69.50	34.75	48.00741
1	0	1	1	1	141.00	70.50	35.25	48.00741
1	1	0	0	0	143.00	71.50	35.75	48.00741
1	1	0	0	1	145.00	72.50	36.25	48.00741
1	1	0	1	0	150.00	75.00	37.50	48.00741
1	1	0	1	1	155.00	77.50	38.75	48.00741
1	1	1	0	0	160.00	80.00	40.00	48.00741
1	1	1	0	1	170.00	85.00	42.50	48.00741
1	1	1	1	0	66.67	66.67	33.34	48.00741
1	1	1	1	1	200.00	66.67	33.33	48.00741

Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency
Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 – 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or getting unstable. System BIOS or other control software can enable the Watchdog timer before they attempt to make a frequency change. If the system hangs and a Watchdog timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All the related registers are summarized in the following table.

Register Summary	
Name	**Description**
Pro_Freq_EN	Programmable output frequencies enabled 0 = disabled (default) 1 = enabled When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used. When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs.
FS_Override	When Pro_Freq_EN is cleared or disabled, 0 = Select operating frequency by FS input pins (default) 1 = Select operating frequency by SEL bits in SMBus control bytes When Pro_Freq_EN is set or enabled, 0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default) 1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes
CPU_FSEL_N, CPU_FSEL_M	When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block Write to update both registers within the same SMBus bus operation. The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.
ROCV_FREQ_SEL	ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL. 0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]
ROCV_FREQ_N[7:0], ROCV_FREQ_M[6:0]	When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block Write to update both registers within the same SMBus bus operation.
WD_EN	0 = Stop and re-load Watchdog timer 1 = Enable Watchdog timer. It will start counting down after a frequency change occurs.
WD_TO_STATUS	Watchdog Timer Time-out Status bit 0 = No time-out occurs (Read); Ignore (Write) 1 = time-out occurred (Read); Clear WD_TO_STATUS (Write)

Register Summary (continued)	
Name	**Description**
WD_TIMER[4:0]	These bits store the time-out value of the Watchdog timer. The scale of the timer is determined by the prescaler. The timer can support a value of 150 ms – 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec – 80 sec. When the Watchdog timer reaches “0,” it will set the WD_TO_STATUS bit.
WD_PRE_SCALER	0 = 150 ms 1 = 2.5 sec
RST_EN_WD	This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs. 0 = Disabled 1 = Enabled
RST_EN_FC	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled

Program the CPU Output Frequency

When the programmable output frequency feature is enabled (Pro_Freq_EN bit is set), the CPU output frequency is determined by the following equation:

Fcpu = G * (N+3)/(M+3) .

“N” and “M” are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

“G” stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 4*.

The ratio of (N+3) and (M+3) needs to be greater than “1” [(N+3)/(M+3) > 1].

The following table lists set of N and M values for different frequency output ranges.This example uses a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

Table 5. Examples of N and M Value for Different CPU Frequency Range

Frequency Ranges	Gear Constants	Fixed Value for M-Value Register	Range of N-Value Register for Different CPU Frequency
50 MHz – 129 MHz	48.00741	93	97 – 255
130 MHz – 248 MHz	48.00741	45	127 – 245

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage .....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation.....1Ω

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .....> 2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DD_REF}, V_{DD_PCI},VDD_CORE, V_{DD_3V66}, $V_{DD\_48\ MHz}$, V_{DD_CPU},	3.3V Supply Voltages	3.135	3.465	V
$V_{DD\_48\ MHz}$	48 MHz Supply Voltage	2.85	3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_{in}	Input Pin Capacitance		5	pF
C_{XTAL}	XTAL Pin Capacitance		22.5	pF
C_L	Max. Capacitive Load on 48 MHz, REF PCICLK, 3V66		 20 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$		2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Pads			0.8	V
V_{OH}	High-level Output Voltage	48 MHz, REF, 3V66	I_{OH} = –1 mA	2.4		V
		PCI	I_{OH} = –1 mA	2.4		V
V_{OL}	Low-level Output Voltage	48 MHz, REF, 3V66	I_{OL} = 1 mA		0.4	V
		PCI	I_{OL} = 1 mA		0.55	V
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$		–5	5	mA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$		–5	5	mA
I_{OH}	High-level Output Current	CPU For I_{OH} = 6*IRef Configuration	Type X1, V_{OH} = 0.65V	12.9		mA
			Type X1, V_{OH} = 0.74V		14.9	
		REF, 48 MHz	Type 3, V_{OH} = 1.00V	–29		
			Type 3, V_{OH} = 3.135V		–23	
		3V66, PCI	Type 5, V_{OH} = 1.00V	–33		
			Type 5, V_{OH} = 3.135V		–33	
I_{OL}	Low-level Output Current	REF, 48 MHz	Type 3, V_{OL} = 1.95V	29		mA
			Type 3, V_{OL} = 0.4V		27	
		3V66, PCI,	Type 5, V_{OL} =1.95 V	30		
			Type 5, V_{OL} = 0.4V		38	
I_{OZ}	Output Leakage Current	Three-state			10	mA
I_{DD3}	3.3V Power Supply Current	VDD_CORE/VDD3.3 = 3.465V, F_{CPU} = 133 MHz			250	mA
I_{DDPD3}	3.3V Shutdown Current	VDD_CORE/VDD3.3 = 3.465V			20	mA

Switching Characteristics[2] Over the Operating Range, PCI ,3V66 Clock Outputs.(Lump CapacitanceTest Load = 20 pF)

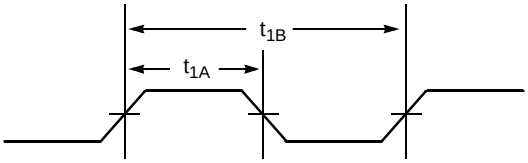
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[3]	Measured at 1.5V	45	55	%
t_3	USB, REF, DOT	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	ps
t_3	PCI,3V66	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t_5	3V66[0:1]	3V66-3V66 Skew	Measured at 1.5V		500	ps
t_5	66BUFF[0:2]	66BUFF-66BUFF Skew	Measured at 1.5V		175	ps
t_6	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_7	3V66 ,PCI	3V66-PCI Clock Jitter	3V66 leads. Measured at 1.5V	1.5	3.5	ns
t_9	3V66	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		250	ps
t_9	USB, DOT	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		350	ps
t_9	PCI	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		500	ps
t_9	REF	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		1000	ps
CPU 1.0V Switching Characteristics						
t_2	CPU	RiseTime	Measured differential waveform from –0.35V to +0.35V	175	467	ps
t_3	CPU	Fall Time	Measured differential waveform from –0.35V to +0.35V	175	467	ps
t_4	CPU	CPU-CPU Skew	Measured at Crossover		150	ps
t_8	CPU	Cycle-Cycle Clock Jitter	Measured at Crossover $t_{8 =} t_{8A} – t_{8B}$		150	ps
	CPU	Rise/Fall Matching	Measured with test loads[5]		325	mV
V_{oh}	CPU	High-level Output Voltage including overshoot	Measured with test loads[5]	0.92	1.45	V
V_{ol}	CPU	Low-level Output Voltage including undershoot	Measured with test loads[5]	-0.2	0.35	V
$V_{crossover}$	CPU	Crossover Voltage	Measured with test loads[5]	0.51	0.76	V
CPU 0.7V Switching Characteristics						
t_2	CPU	RiseTime	Measured single ended waveform from 0.175V to 0.525V	175	700	ps
t_3	CPU	Fall Time	Measured single ended waveform from 0.175V to 0.525V	175	700	ps
t_4	CPU	CPU-CPU Skew	Measured at Crossover		150	ps
t_8	CPU	Cycle-Cycle Clock Jitter	Measured at Crossover $t_{8 =} t_{8A} – t_{8B}$ With all outputs running		150	ps
	CPU	Rise/Fall Matching	Measured with test loads[3,4]		20	%
V_{oh}	CPU	High-level Output Voltage including overshoot	Measured with test loads[4]		0.85	V
V_{ol}	CPU	Low-level Output Voltage including undershoot	Measured with test loads[4]	-0.15		V
$V_{crossover}$	CPU	Crossover Voltage	Measured with test loads[4]	0.28	0.43	V

Notes:

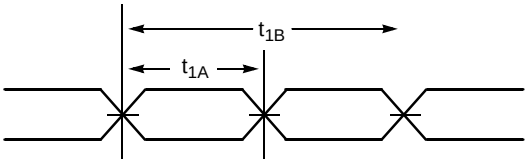
2. All parameters specified with loaded outputs.
3. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
4. Determined as a fraction of 2*(Trp – Trn)/(Trp +Trn) Where Trp is a rising edge and Trp is an intersecting falling edge.
5. The 0.7V test load is R_s = 33.2 ohm, R_p = 49.9 ohm in test circuit.
6. The 1.0V test load is shown on test circuit page.

Switching Waveforms

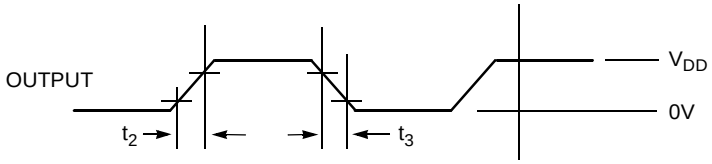
Duty Cycle Timing (Single-Ended Output)



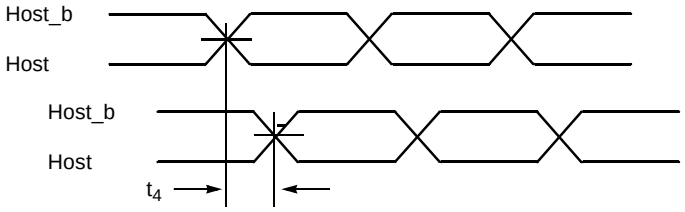
Duty Cycle Timing (CPU Differential Output)



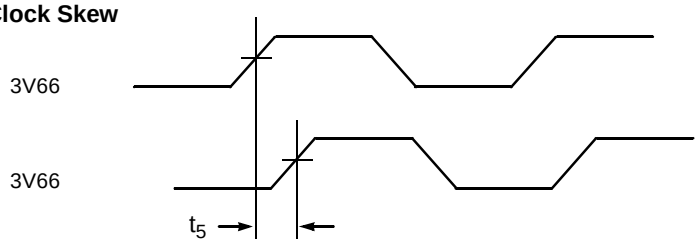
All Outputs Rise/Fall Time



CPU-CPU Clock Skew

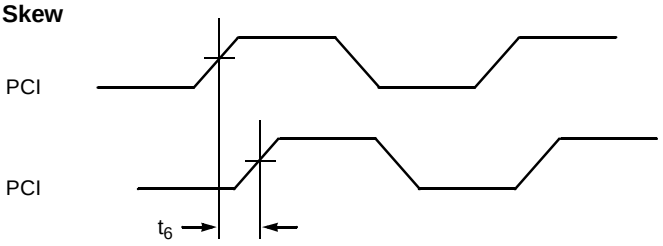


3V66-3V66 Clock Skew

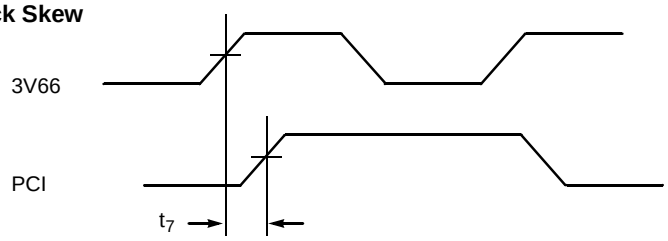


Switching Waveforms (continued)

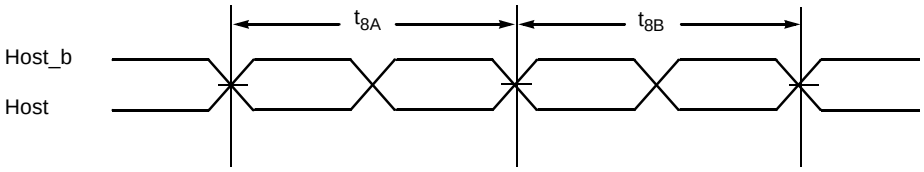
PCI-PCI Clock Skew



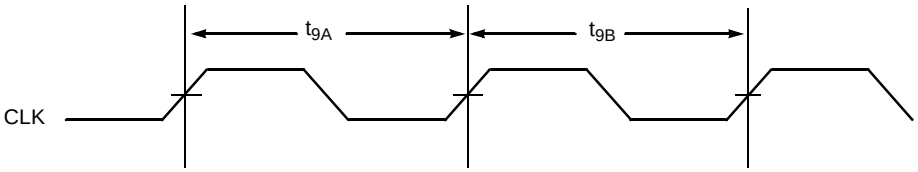
3V66-PCI Clock Skew



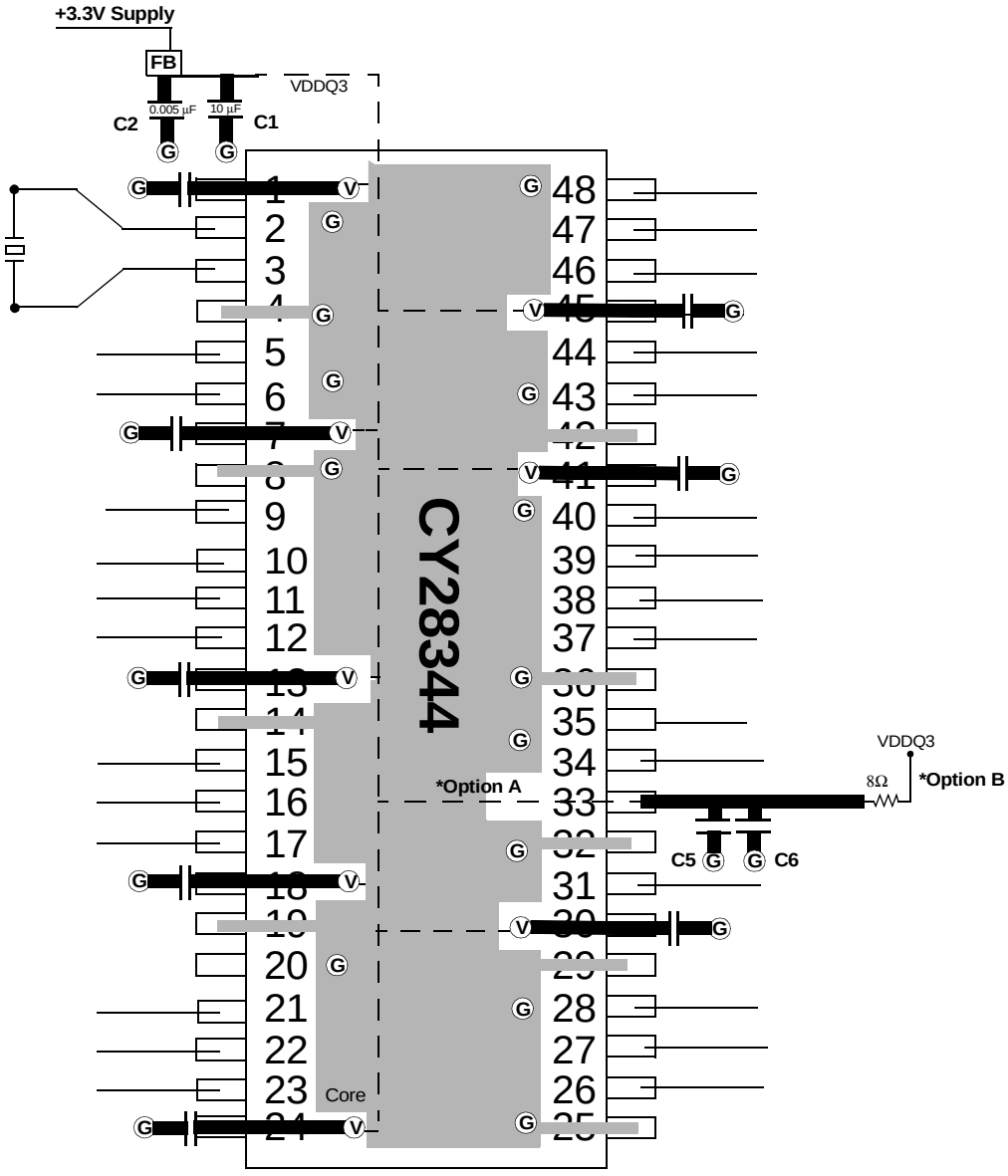
CPU Clock Cycle-Cycle Jitter



Cycle-Cycle Clock Jitter

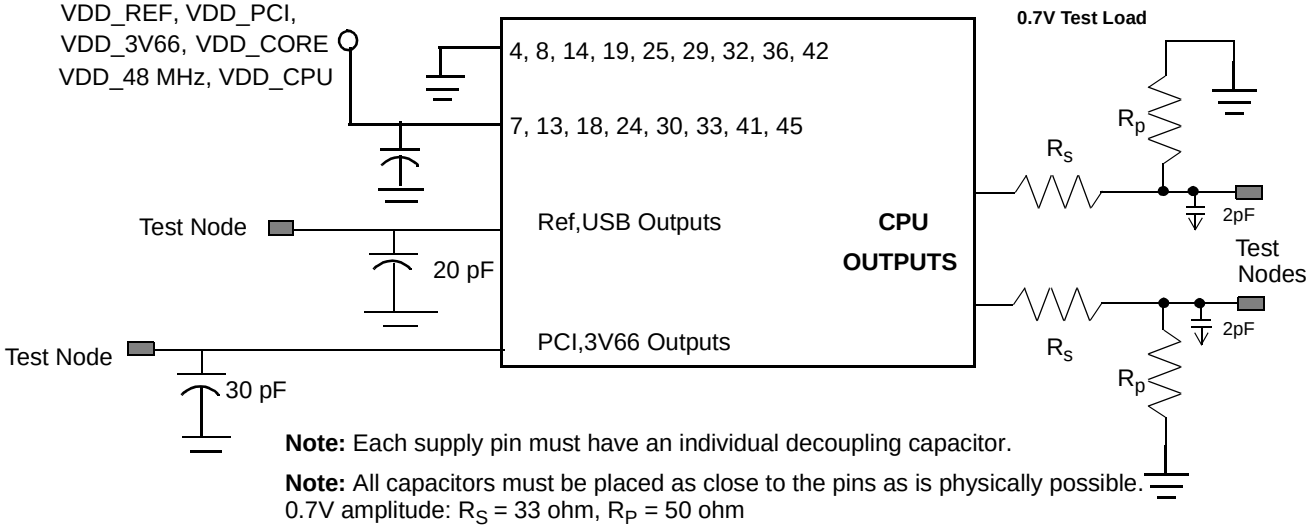


Layout Example



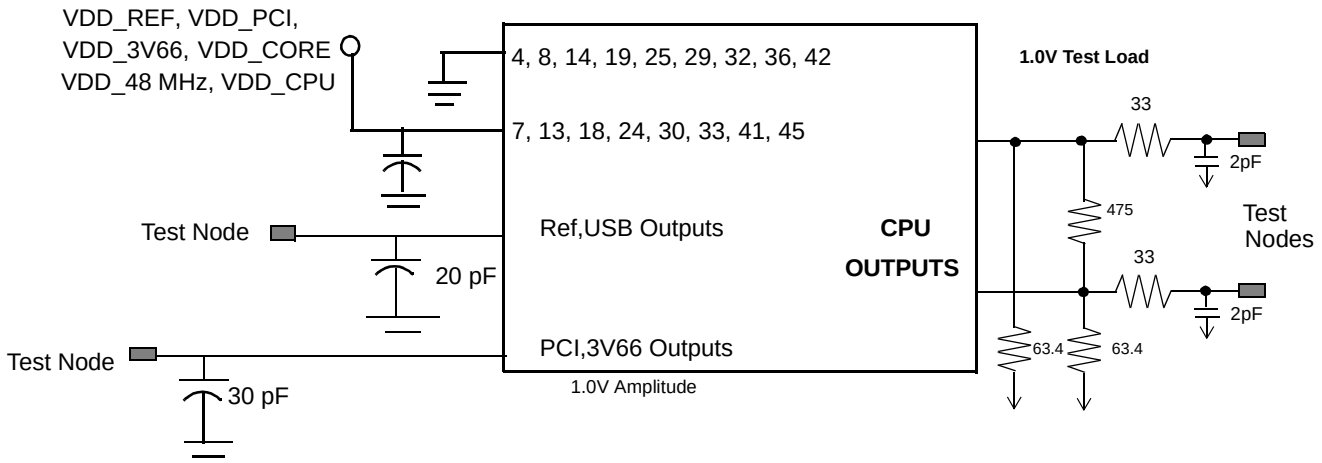
FB = Dale ILB1206 – 300 or 2TDKACB2012L – 120 or 2 Murata BLM21B601S
Ceramic Caps C1 = 10 – 22 µF C2 = 0.005 µF C5 = 0.1 µF C6 = 10 µF
Ⓖ= VIA to GND plane layer Ⓥ= VIA to respective supply plane layer
Note. Each supply plane or strip should have a ferrite bead and capacitors.
* If on-board video uses 48 MHz or Dot clock uses Option B
All bypass caps on V_{DD} pin = 0.1 uF Low ESR

Test Circuit



Note: Each supply pin must have an individual decoupling capacitor.

Note: All capacitors must be placed as close to the pins as is physically possible.
0.7V amplitude: R_S = 33 ohm, R_P = 50 ohm

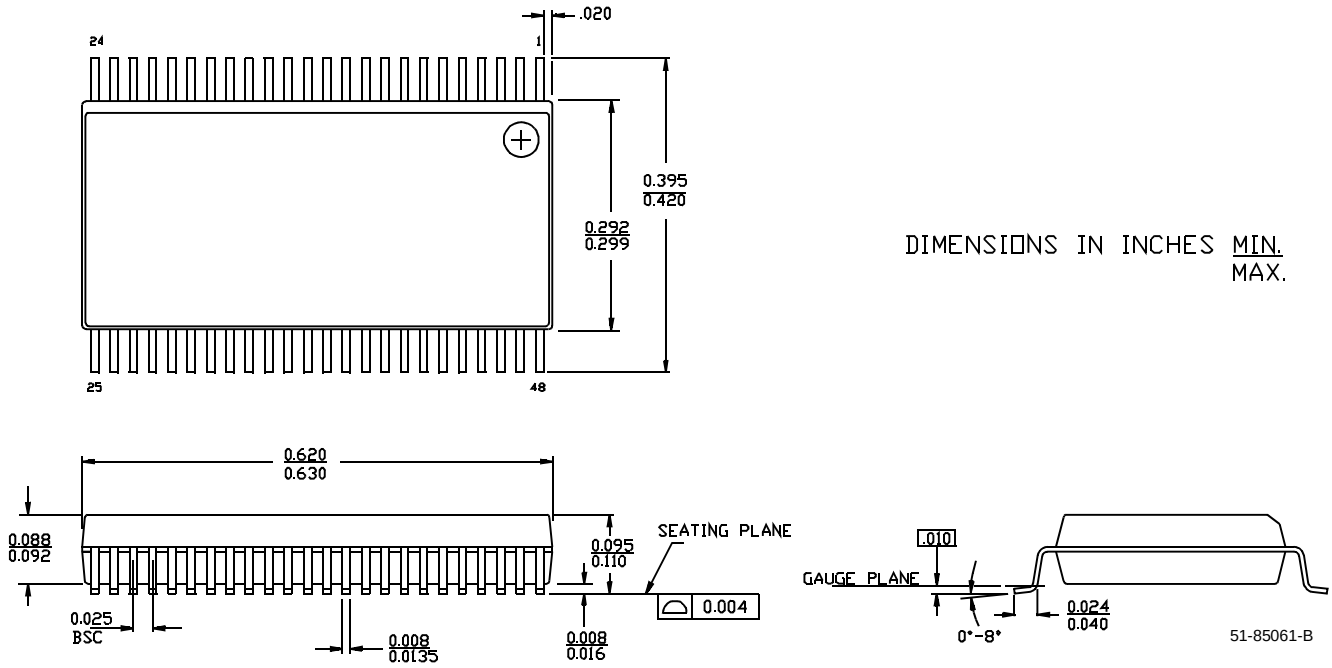


Ordering Information

Ordering Code	Package Type	Operating Range
CY28344PVC	48-pin Small Shrunk Outline Package (SSOP)	Commercial

Package Diagram

48-lead Shrunk Small Outline Package O48



Document Title: CY28344 FTG for Intel Pentium 4 CPU and Chipsets Document Number: 38-07113				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110805	12/11/01	IKA	Adding switching characteristics. Added notes to operating conditions.