



CYPRESS

CY28330

Clock Generator for AMD™ Hammer

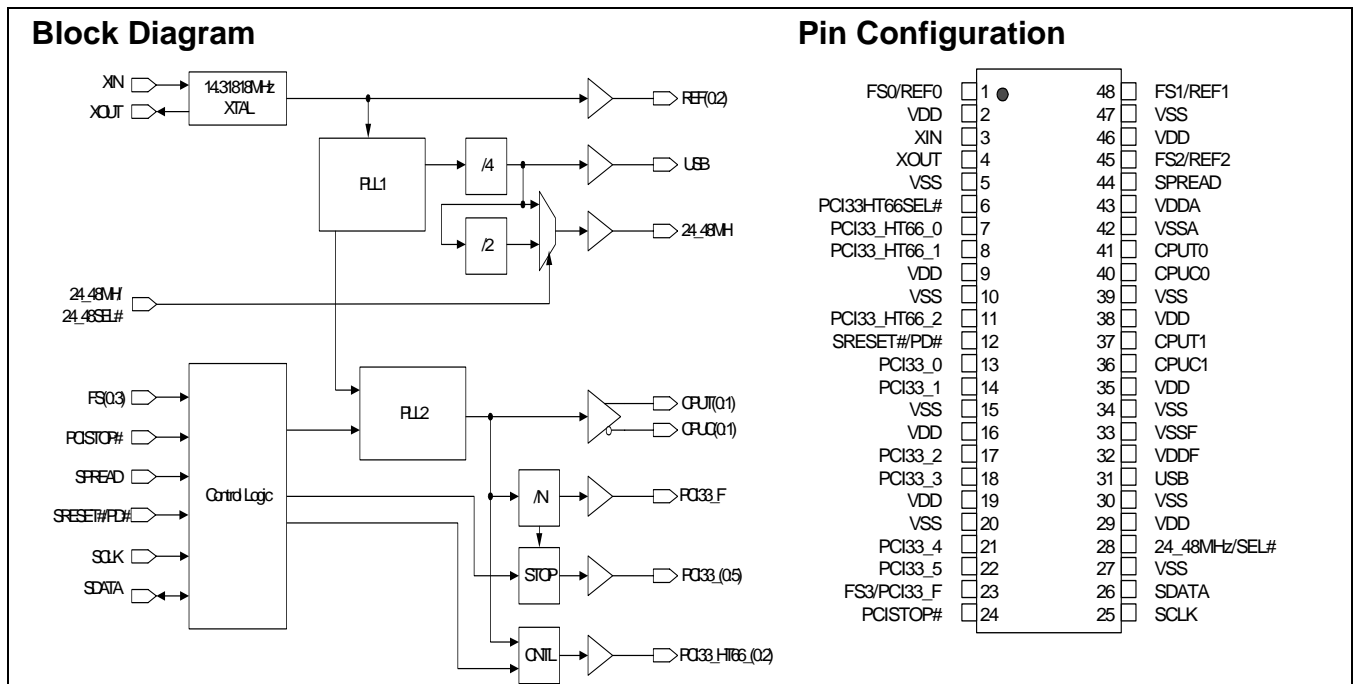
Features

- Supports AMD hammer CPU
- Two differential pair CPU clocks
- Six low-skew/low-jitter PCI clocks
- One free-running PCI clock
- Three low-skew/low-jitter AGP/HT clocks
- 148M output for USB
- One programmable 24M or 48M for FDC
- Three REF 14.318-MHz clocks
- Dial-a-Frequency™ programmability
- Cypress Spread Spectrum for best electromagnetic interference (EMI) reduction
- SMBus register-programmable options
- 5V-tolerance SCLK and SDATA lines
- 3.3V operation
- Power management control pins
- 48-pin SSOP package

Table 1. Frequency Table (MHz)^[1]

FS (3:0)	CPU	PCI HT SEL	PCI HT	PCI	VC0	CPU Div	PCI HT Div	PCI Div
0000	Hi-Z	X	Hi-Z	Hi-Z				
0001	XIN	0	XIN/3	XIN/6				
0001	XIN	1	XIN/6	XIN/6				
0010								
0011								
0100	100.0	0/1	66.7/33.3	33.31	200	2	3/6	6
0101	133.3	0/1	66.7/33.3	33.31	266.6	2	4/8	8
0110	166.7	0/1	66.7/33.3	33.31	333.3	2	5/10	10
0111	200.0	0/1	66.7/33.3	33.31	400.0	2	6/12	12
1000	105.0	0/1	70.0/35.0	35.00	210.0	2	3/6	6
1001	110.0	0/1	73.3/36.7	36.67	220.0	2	3/6	6
1010	115.0	0/1	76.7/38.3	38.33	230.0	2	3/6	6
1011	120.0	0/1	60.0/30.0	30.00	240.0	2	4/8	8
1100	140.0	0/1	70.0/35.0	35.00	280.0	2	4/8	8
1101	150.0	0/1	60.0/30.0	30.00	300.0	2	5/10	10
1110	160.0	0/1	64.0/32.0	32.00	320.0	2	5/10	10
1111	180.0	0/1	60.0/30.0	30.00	360.0	2	6/12	12

1. All outputs except X_{OUT} will be three-stated when FS(3:0) = 0000.



Pin Description

Pin	Name	PWR	I/O	Description
3	XIN	V _{DD}	I	Oscillator Buffer Input. Connect to a crystal or to an external clock.
4	XOUT	V _{DD}	O	Oscillator Buffer Output. Connect to a crystal. Do not connect when an external clock is applied at X _{IN} .
41, 37	CPUT(0:1)	V _{DDC}	O	CPU clock outputs 0 and 1: push-pull “true” output of differential pair.
40, 36	CPUC(0:1)	V _{DDC}	O	CPU clock outputs 0 and 1: push-pull “compliment” output of differential pair.
23	PCI33_F		O	3.3V free-running PCI clock output.
13, 14, 17, 18, 21, 22	PCI33(0:5)		O	3.3V PCI clock outputs controlled by PCISTOP#.
7, 8, 11	PCI33_HT66(0:2)	V _{DDD}	O	3.3V PCI 33 MHz or HyperTransport™ 66 (HT66) Clock Outputs. This group is selectable between 33 MHz and 66 MHz based upon the state of the PCI33HT66SEL#.
6	PCI33_HT66SEL#	V _{DDD}	I/PU	This input selects the output frequency of PCI33_HT66 outputs to either 33 MHz or 66 MHz. There is an internal 100K-ohm pull-up resistor. This pin will be externally strapped LOW using a 10K-ohm resistor to V _{SS} . 0 = 66 MHz, 1 = 33 MHz.
31	USB		O	3.3V USB clock output at 48 MHz.
28	24_48/SEL#		I/O	3.3v Super I/O clock output. At power-up this pin is sensed to determine whether the output is 24 MHz or 48 MHz. There is an internal 100K-ohm pull-up resistor. This pin will be externally strapped LOW using a 10K-ohm resistor to V _{SS} . 0 = 48 MHz, 1 = 24 MHz.
1, 48, 45	REF(0:2)/FS(0:2)		I/O	3.3V Reference Clock Output. At power-up this pin is sensed to determine the CPU output frequency. There is an internal 100K-ohm pull-up resistor. These pins will be externally strapped LOW using a 10K-ohm resistor to V _{SS} . See Table 1.
44	SPREAD		I	Spread Spectrum Clock Enable. At power-up this pin is sensed to determine whether spread spectrum clocking is enabled on all output except the USB and 24_48/SEL#. There is an internal 100K-ohm pull-up resistor. This pin will be externally strapped LOW using a 10K-ohm resistor to V _{SS} . 0 = disable, 1 = enable.
24	PCISTOP#		I	Control for PCI33(0:5) and PCI33_HT66(0:2) Outputs. Active LOW control input to halt all 33-MHz PCI clocks except PCI33_F. Only the PCI33_HT66 outputs that are running at 33 MHz will be stopped. The outputs will be glitch-free when turning off and turning on.
12	NC			Pin reserved for vendor specific purpose.
26	SDATA		I/O	Data pin for SMBus (rev2.0). There is an internal 100K-ohm pull-up resistor.
25	SCLK		I	Clock pin for SMBus (rev2.0). There is an internal 100K-ohm pull-up resistor.
2, 9, 16, 19, 29, 35, 38, 46	VDD		PWR	Power connection to 3.3V for the core.
5, 10, 15, 20, 27, 30, 34, 39, 47	VSS		GND	Power connection to ground for the core section of the chip.
43	VDDA		PWR	Power connection to 3.3V for the analog section of the chip.
42	VSSA		GND	Power connection to ground for the analog section of the chip.
32	VDDF		PWR	Power connection to 3.3V for the 48-MHz phase locked loop (PLL) section of the chip.
33	VSSF		GND	Power connection to ground for the 48-MHz PLL section of the chip.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc., can be individually enabled or disabled.

The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operation from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The Block Write and Block Read protocol is outlined in *Table 3*, while *Table 4* outlines the corresponding Byte Write and Byte Read protocol.

The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation
(6:0)	Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be "0000000"

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8-bit "00000000" stands for block operation	11:18	Command Code – 8-bit "00000000" stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data byte N/Slave acknowledge...	39:46	Data byte from slave – 8 bits
....	Data byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Stop	56	Acknowledge
		Data bytes from slave/acknowledge
		Data byte N from slave – 8 bits
		Not acknowledge
		Stop

Table 4. Byte Read and Byte Write Protocol^[2]

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8-bit “1xxxxxx” stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8-bit “1xxxxxx” stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not acknowledge
		39	Stop

Serial Control Registers

Byte 0: Frequency and Spread Spectrum Control Register

Bit	@Pup	Description
7	Inactive = 0	Write Disable (Write Once). A 1 written to this bit after a 1 has been written to Byte0 bit0 will permanently disable modification of all configuration registers until the part has been powered off. Once the clock generator has been Write Disabled, the SMBus controller should still accept and acknowledge subsequent write cycles but it should not modify any of the registers.
6	Inactive = 0	Spread Spectrum Enable (0 = disable, 1 = enable). This bit provides a software-programmable control for spread spectrum clocking. See <i>Table 5</i> . The readback version of this bit is the hardware strapped value such that the software has the ability to know each state, either by readback or by writing the SSE bit.
5	FS4 pin	FS(4) (reserved for mapping to a larger FS table via programmable FS bit only).
4	FS3 pin	FS(3) (corresponds to Frequency Selection. See <i>Table 1</i> .
3	FS2 pin	FS(2) (corresponds to Frequency Selection. See <i>Table 1</i> .
2	FS1 pin	FS(1) (corresponds to Frequency Selection. See <i>Table 1</i> .
1	FS0 pin	FS(0) (corresponds to Frequency Selection. See <i>Table 1</i> .
0	Inactive = 0	Write Enable. A 1 written to this bit after power-up will enable modification of all configuration registers and subsequent 0's written to this bit will disable modification of all configuration except this single bit. Note that block write transactions to the interface will complete, however unless the interface has been previously un-locked, the writes will have no effect. The effect of writing this bit does not take effect until the subsequent block write command.

Table 5. Spread Spectrum Enable

Pin 44	B0b6	Spread Enable
0	0	Off
0	1	On
1	0	On
1	1	On

Note:

- The Write address is D2 and the Read address is D3.

Byte 1: PCI Clock Control Register

Bit	@Pup	Pin#	Name	Test Condition
7	1	H/W	PCI33_HT66_1	Enable (1 = Enabled, 0 = Disabled)
6	1		PCI33_HT66_0	Enable (1 = Enabled, 0 = Disabled)
5	1		PCI33_5	Enable (1 = Enabled, 0 = Disabled)
4	1		PCI33_4	Enable (1 = Enabled, 0 = Disabled)
3	1		PCI33_3	Enable (1 = Enabled, 0 = Disabled)
2	1		PCI33_2	Enable (1 = Enabled, 0 = Disabled)
1	1		PCI33_1	Enable (1 = Enabled, 0 = Disabled)
0	1		PCI33_0	Enable (1 = Enabled, 0 = Disabled)

Byte 2: PCI Clock, USB, 24-MHz–48-MHz, REF(0:2) Control Register

Bit	@Pup	Test Condition
7	active = 1	Reserved. CPUT/C(1) shutdown. This bit can be optionally used to disable the CPUT/C(1) clock pair. During shutdown, CPUT= LOW and CPUC = HIGH
6	active = 1	Reserved. CPUT/C(0) shutdown. This bit can be optionally used to disable the CPUT/C(0) clock pair. During shutdown, CPUT = LOW and CPUC = HIGH
5	active = 1	REF(2) enable (1 = Enabled, 0 = Disabled)
4	active = 1	REF(1) enable (1 = Enabled, 0 = Disabled)
3	active = 1	REF(0) enable (1 = Enabled, 0 = Disabled)
2	active = 1	24_48MHz enable ((1 = Enabled, 0 = Disabled)
1	active = 1	USB enable (1 = Enabled, 0 = Disabled)
0	active = 1	PCI33_HT66(2) enable (1 = Enabled, 0 = Disabled)

Byte 3: PCI Clock Free Running Select Control Register

Bit	@Pup	Description
7	Inactive = 0	Reserved for vendor specific functions
6	Inactive = 0	Reserved for vendor specific functions
5	Inactive = 0	PCI(5) free-running enable (1 = Free running, 0 = Disabled)
4	Inactive = 0	PCI(4) free-running enable (1 = Free running, 0 = Disabled)
3	Inactive = 0	PCI(3) free-running enable (1 = Free running, 0 = Disabled)
2	Inactive = 0	PCI(2) free-running enable (1 = Free running, 0 = Disabled)
1	Inactive = 0	PCI(1) free-running enable (1 = Free running, 0 = Disabled)
0	Inactive = 0	PCI(0) free-running enable (1 = Free running, 0 = Disabled)

Byte 4: Pin-latched/Real-time State (and one free-running control)

Bit	@Pup	Description
7	active = 1	Reserved. PCI33_F output enable. This bit can be optional used to disable the PCI33_F output.
6	active = 1	SPREAD pin state, not latched
5	active = 1	24_48SEL# pin power-up latched state
4	active = 1	PCI33_HT66SEL# pin statement latched
3	FS2 pin	FS(2) power-up latched state
2	FS1 pin	FS(1) power-up latched state
1	FS0 pin	FS(0) power-up latched state
0	FS3 pin	FS(3) power-up latched state

Byte 5: Clock Vendor ID

Bit	@Pup	Description
7	varies	Vendor ID, 001 = reserved, 111 = reserved
6		Vendor ID
5		Vendor ID
4		Device Revision ID
3		Device Revision ID
2		Device Revision ID
1		Device Revision ID
0		Device Revision ID

Byte 6: SSCG, Dial-a-Skew™ and Dial-a-Ratio™ Register

Bit	@Pup	Description
7	0	SS_MODE; 0 = down spread, 1 = center spread See <i>Table 6</i> .
6	0	SST1 Select spread percentage. See <i>Table 6</i> .
5	0	SST0 Select spread percentage. See <i>Table 6</i> .
4	0	48MHz_1_EN; 0 = disabled, 1 = enabled if no external pull-up is connected. 0 = enabled, 1 = disabled if external pull-up exists.
3	0	DASAG1; Programming these bits allows shifting the skew of the HT66(0:2) signals relative to their default value. See <i>Table 7</i> .
2	0	DASAG0; Programming these bits allows shifting the skew of the HT66(0:2) signals relative to their default value. See <i>Table 7</i> .
1	0	DARAG1; Programming these bits allows shifting the ratio of the HT66(0:2) signals relative to their default value. See <i>Table 8</i> .
0	0	DARAG0; Programming these bits allows shifting the ratio of the HT(0:2) signals relative to their default value. See <i>Table 8</i> .

Table 6. Spread Spectrum Table

SS_Mode (B6b7)	SST1 (B6b6)	SST0 (B6b5)	% Spread
0	0	0	–1.5%
0	0	1	–1.0%
0	1	0	–0.7%
0	1	1	–0.5%
1	0	0	±0.75%
1	0	1	±0.5
1	1	0	±0.35%
1	1	1	± 0.25%

Table 7. Dia-a-Skew CPU to HT66

DASAG(1:0)	HT66 Skew Shift
00	Default
01	–150 ps
10	+ 150ps
11	+ 300 ps

Table 8. Dia-a-Ratio CPU to HT66

DASAG(1:0)	CPU/HT66 Ratio
00	Frequency selection default
01	2/1
10	2.5/1
11	3/1

Byte 7: Watchdog Control Register

Bit	@Pup	Name	Description
7	1	Pin 12 Mode Select	SRESET#; 1 = pin 12 is the input pin that functions as a PD# signal. 0 = pin 12 is the output pin as SRESET# signal.
6	0	Frequency Reversion	This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only. 0 = selects frequency of existing hardware setting. 1 = selects frequency of the second to last software setting (the setting prior to the one that caused a system reboot).
5	0		For test, always program to "0."
4	0	WD Time-out	This bit is set to "1" when the Watchdog times out. It is reset to "0" when the system clears the WD time stamps (WD3:0).
3	0	WD3	This bit allows the selection of the time stamp for the Watchdog timer. See <i>Table 9</i> .
2	0	WD2	This bit allows the selection of the time stamp for the Watchdog timer. See <i>Table 9</i> .
1	0	WD1	This bit allows the selection of the time stamp for the Watchdog timer. See <i>Table 9</i> .
0	0	WD0	This bit allows the selection of the time stamp for the Watchdog timer. See <i>Table 9</i> .

Table 9. Watchdog Time Stamp

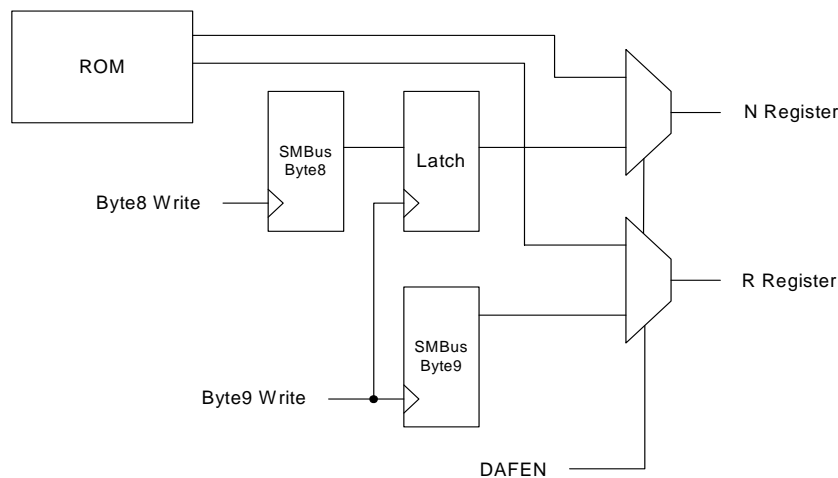
WD3	WD2	WD1	WD0	Function
0	0	0	0	Off
0	0	0	1	1 second
0	0	1	0	2 seconds
0	0	1	1	3 seconds
0	1	0	0	4 seconds
0	1	0	1	5 seconds
0	1	1	0	6 seconds
0	1	1	1	7 seconds
1	0	0	0	8 seconds
1	0	0	1	9 seconds
1	0	1	0	10 seconds
1	0	1	1	11 seconds
1	1	0	0	12 seconds
1	1	0	1	13 seconds
1	1	1	0	14 seconds
1	1	1	1	15 seconds

Byte 8: Dial-a-Frequency Control Register N

Bit	@Pup	Description
7	0	For test, always program to "0." PLL leakage test. 1 = test mode, 0 = normal.
6	N6	These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency with great accuracy. All other synchronous clocks (clocks that are generated from the same PLL such as PCI) remain at their existing ratios relative to the CPU clock.
5	N5	
4	N4	
3	N3	
2	N2	
1	N1	
0	N0	

Byte 9: Dial-a-Frequency Control Register R

Bit	@Pup	Description
7	0	CPU output skew; 0 = normal, 1 = -200 ps Pin 41 to Pin 7
6	R5	These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency with great accuracy. All other synchronous clocks (clocks that are generated from the same PLL such as PCI) remain at their existing ratios relative to the CPU clock.
5	R4	
4	R3	
3	R2	
2	R1	
1	R0	
0	0	When this bit = 1, it enables the Dial-a-Frequency N and R bits to be multiplexed into the internal N and R registers. When this bit = 0, the ROM based N and R values are loading into the internal N and R registers.


Figure 1. Dial-a-Frequency Feature

The SMBus controlled Dial-a-Frequency feature is available in this device via Bytes 8 and Byte 9.

P is a PLL constant that depends on the frequency selection prior to accessing the Dial-a-Frequency feature.

Table 10.

FS(3:0)	P
XXXX	95995000

Operation

Pin strapping on any configuration pin is based on a 10K ohm resistor connected to either 3.3V (V_{DD}) or ground (V_{SS}). When the V_{DD} supply goes above 2.0V, the power-on-reset circuitry latches all of the configuration bits into their respective registers and then allows the outputs to be enabled. The output may not occur immediately after this time as the PLL needs to be locked and will not output an invalid frequency. The CPU frequencies are defined from the hardware-sampled inputs. Additional frequencies and operating states can be selected through the SMBus programmable interface.

Spread spectrum modulation is required for all outputs derived from the internal CPU PLL2 (see the block diagram on page 1). This include the CPU(0:1), PCI33(0:5), PCI33_F and PCI33_HT66(0:2). The REF (0:2), USB and 24_48 clocks are not affected by the spread spectrum modulation. The spread spectrum modulation is set for both center and down modes using linear and Lexmark profiles for amounts of 0.5% and 1.0% at a 33-KHz rate.

The CPU clock driver is of a push-pull type for the differential outputs, instead of the Athlon open-drain style. The CPU clock termination has been derived such that a 15-40 ohm, 3.3V output driver can be used for the CPU clock.

The PCISTOP# signal provides for synchronous control over the any output, except the PCI33_F, that is running at 33 MHz. If the PCI33_HT66 outputs are configured to run at 66 MHz will not be stopped by this signal. The PCISTOP# signal is sampled by an internal PCI clock such that once it is sensed LOW or active, the 33-MHz signals are stopped on the next HIGH to LOW transition such that there is always a valid HIGH signal.

Absolute Maximum Ratings

Parameter	Description	Rating	Unit
V_{DD} , V_{DDA} , V_{DDF}	Supply voltage	-0.5 to 3.8	V
V_{IN1} , V_{IN2}	Input voltage	-0.5 to 3.8	V
TSTG	Storage temperature	-65 to +150	°C
ESD protection	Input ESD (HBN)	> 2,000	V

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD} , V_{DDA} , V_{DDF}	Supply voltage	3.135	3.3	3.465	V
T_A	Operating temperature, ambient	0		70	°C
F_{input}	Input frequency (crystal or reference)	10	14.318	16	MHz

SCLK and SDATA Input Electrical Characteristics (5V-tolerant)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Supply voltage		$V_{SS} - 0.3$		0.8	V
V_{IH}	Input voltage		2.0		$V_{DD} + 0.3$	V
I_{IL} , I_{IH}	Input HIGH/LOW current	$0 < V_{IN} < V_{DD}$			± 5	μA
V_{OL}	Output HIGH voltage	$I_{OL} = 1.75 \text{ mA}$	$V_{SS} - 0.3$		0.4	V
I_{OL}	Output LOW voltage	$V_O = 0.8 \text{ V}$	2		6	mA

DC Parameters (all outputs loaded)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW voltage	Note 3	$V_{SS} - 0.3$		0.8	V
V_{IH}	Input HIGH voltage		2.0		$V_{DD} + 0.3$	V
I_{IL}	Input LOW current (@ $V_{IL} = V_{SS}$)	For internal pull-up resistors ^[4]			-50	μA
I_{IH}	Input HIGH current (@ $V_{IH} = V_{DD}$)				50	μA
I_{OZ}	Three-state leakage current				10	μA
$I_{DD3.3V}$	Dynamic supply current	CPU(0:1) @ 200 MHz		250		mA
$I_{PD3.3V}$	Power-down supply current				2	mA
C_{IN}	Input pin capacitance				5	pF
C_{OUT}	Output pin capacitance				6	pF
L_{PIN}	Pin inductance				7	nH
C_{XTAL}	Crystal pin capacitance	Measured from pin to ground.	27	36	45	pF
V_{BIAS}	Crystal DC bias voltage		$0.3V_{DD}$	$V_{DD/2}$	$0.7V_{DD}$	V
T_{XS}	Crystal start-up time	From stable 3.3V power supply.			40	μs

AC Parameters

Parameter	Description	Conditions	PCI133_HT66 = 66MHz			
			Min.	Typ.	Max.	Unit
T_R	Output rise edge rate	Measured @ the hammer test load using $V_{OCM} \pm 400 \text{ mV}$, 0.850V to 1.650V	2		7	V/ns
T_F	Output fall edge rate	Measured @ the hammer test load using $V_{OCM} \pm 400 \text{ mV}$, 1.650V to 0.850V	2		7	V/ns

Notes:

- Applicable to input signals: SPREAD, PCISTOP#, 24-48/Sel#.
- Internal pull-up and pull-down resistors have a typical value of 250 Ω .

AC Parameters

Parameter	Description	Conditions	PCI133_HT66 = 66MHz			
			Min.	Typ.	Max.	Unit
V _{DIFF}	Differential voltage	Measured @ the hammer test load (single-ended)	0.4	1.25	2.3	V
DV _{DIFF}	Change in VDIFF_DC magnitude	Measured @ the hammer test load (single-ended)	-150		150	mV
VCM	Common mode voltage	Measured @ the hammer test load (single-ended)	1.05	1.25	1.45	V
ΔVCM	Change in VCM	Measured @ the hammer test load (single-ended)	-200		200	mV
T _D	Duty cycle	Measured at VOX	45	50	53	%
T _{JC}	Jitter, cycle-to-cycle	Measured at VOX	0	100	200	ps
T _{JA}	Jitter, accumulated	Measured at VOX	-1000		1000	ps
T _{JSC_OP}	Spectral content noise near hammer frequency		TBD		TBD	dB
T _{JSC_DC}	Spectral content noise from 0-200 MHz	Noise floor measured with Spread Spectrum on between 0 – 200MHz. Measured with a 3.3V PECL differential buffer inline with CPU clock output	TBD		TBD	dB
T _{FS}	Frequency stabilization from power-up	Measure from full supply voltage	0		3	ms
R _{ON}	Output impedance	Average value during switching transition	15	35	55	Ω

Table 11. PCI/HyperTransport Clock Outputs

Parameter	Description	Conditions	PCI33, PCI33_HT = 33 MHz			PCI33_HT = 66 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{OL}	Output LOW voltage	I _{OL} = 9.0mA	–		0.4			0.4	V
V _{OH}	Output HIGH voltage	I _{OH} = -12.0mA	2.4			2.4		–	V
I _{OL}	Output LOW current	V _O = 0.8V	10			10		–	mA
I _{OH}	Output HIGH current	V _O = 2.0V			-15			-15	mA
F	Frequency actual			33.33			66.67		MHz
T _R	Output rise edge rate	Measured from 20%–60%	1		4	1		4	V/ns
T _F	Output fall edge rate	Measured from 60%–20%	1		4	1		4	V/ns
T _D	Duty cycle	Measured at 1.5V	45		55	45		55	%
T _{JC}	Jitter, cycle-to-cycle	Measured at 1.5V	0		250	0		250	ps
T _{JA}	Jitter cccumulated	Measured at 1.5V	-1000		1000	-1000		1000	ps
T _{FS}	Frequency stabilization from power-up	Measure from full supply voltage	0		3			3	ms
R _{ON}	Output impedance	Average value during switching transition	12	15	55	12	15	55	Ω

Table 12. REF(0:2) Clock Outputs

Parameters	Description	Test Conditions	PCI133_HT66 = 66 MHz			
			Min.	Typ.	Max.	Unit
V _{OL}	Output LOW voltage	I _{OL} = 9.0 mA			0.4	V
V _{OH}	Output HIGH voltage	I _{OH} = -12.0 mA	2.4			V
I _{OL}	Output LOW current	V _O = 0.8V	16			mA
I _{OH}	Output HIGH current	V _O = 2.0V			-22	mA
F	Frequency, actual			14.318		MHz

Table 12. REF(0:2) Clock Outputs

Parameters	Description	Test Conditions	PCI133_HT66 = 66 MHz			
			Min.	Typ.	Max.	Unit
T_R	Output rise edge rate	Measured from 20%–60%	0.5		2	V/ns
T_F	Output fall edge rate	Measured from 60%–20%	0.5		2	V/ns
T_D	Duty cycle	Measured at 1.5V	45		55	%
T_{JC}	Jitter, cycle-to-cycle	Measured at 1.5V	0	500	1000	ps
T_{JA}	Jitter, accumulated	Measured at 1.5V	–1000		1000	ps
T_{FS}	Frequency stabilization from power-up	Measure from full supply voltage	0		3	mS
R_{ON}	Output impedance	Average value during switching transition	20	24	60	W

Table 13. USB, 24_24 Clock Outputs

Parameters	Description	Conditions	PCI33, PCI33_HT = 33 MHz			PCI33_HT = 66 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OL}	Output LOW voltage	$I_{OL} = 9.0\text{ mA}$			0.4			0.4	V
V_{OH}	Output HIGH voltage	$I_{OH} = -12.0\text{ mA}$	2.4			2.4			V
I_{OL}	Output LOW current	$V_O = 0.8\text{ V}$	16			16			mA
I_{OH}	Output HIGH current	$V_O = 2.0\text{ V}$			–22			–22	mA
F	Frequency actual			24.004			48.008		MHz
T_R	Output rise edge rate	Measured from 20%– 80%	0.5		2	0.5		2	V/ns
T_F	Output fall edge rate	Measured from 80%–20%	0.5		2	0.5		2	V/ns
T_D	Duty cycle	Measured at 1.5V	45		55	45		55	%
T_{JC}	Jitter, cycle-to-cycle 24_48 MHz	Measured at 1.5V	0	250	500	0	250	500	ps
T_{JC}	Jitter, cycle-to-cycle USB	Measured at 1.5V				0		100	ps
T_{JA}	Jitter, accumulated	Measured at 1.5V	–1000		1000	–1000		1000	ps
T_{FS}	Frequency stabilization from power_up	Measure from full supply voltage	0		3	0		3	ms
R_{ON}	Output impedance	Average value during switching transition.	20	24	60	20	24	60	Ω

Table 14. Skew ^[5]

Parameters	Description	Conditions	Skew Window	Unit
TSK_CPU_CPU	CPU-to-CPU skew, time-independent	Measured @ crossing points for CPUT rising edges ¹	250	ps
TSK_CPU_PCI33	CPU-to-PCI33 skew, time-independent	Measured @ crossing points for CPUT rising edge and 1.5V PCI clocks	500	ps
TSK_PCI33_PCI33	PCI33-to-PCI33 skew, time-independent	Measured between rising @ 1.5V	500	ps
TSK_PCI33_HT66	PCI33-to-HT66 skew, time-independent	Measured between rising @ 1.5V	500	ps
TSK_CPU_HT66	CPU-to-HT66 skew, time-independent	Measured @ crossing points for CPUT rising edge and 1.5V for HyperTransport clocks	500	ps
TSK_HT66_HT66	HT66-to-HT66 skew, time-independent	Measured between rising @ 1.5V	500	ps

Note:

5. All skews in this skew budget are measured from the first referenced signal to the next. Therefore, this skew specifies the maximum skew window between these two signals to be 500 ps whether the CPU crossing leads or lags the PCI clock. This should not be interpreted to mean that the PCI33 edge could either be 500 ps before the CPU clock to 500 ps after the clock, thus defining a 1000-ps window in which the PCI33 clock edge could fall.

Table 14. Skew (continued)^[5]

Parameters	Description	Conditions	Skew Window	Unit
TSK_CPU_CPU	CPU-to-CPU skew, time-variant	Measured @ crossing points for CPUT rising edges	200	ps
TSK_CPU_PCI33	CPU-to-PCI33 skew, time-variant	Measured @ crossing points for CPUT rising edge and 1.5V PCI clocks	200	ps
TSK_PCI33_PCI33	PCI33-to-PCI33 skew, time-variant	Measured between rising @ 1.5V	200	ps
TSK_PCI33_HT66	PCI33-to-HT66 skew, time-variant	Measured between rising @ 1.5V	200	ps
TSK_CPU_HT66	CPU-to-HT66 skew, time-variant	Measured @ crossing points for CPUT rising edge and 1.5V for HyperTransport clocks	200	ps
TSK_HT66_HT66	HT66-to-HT66 skew, time-variant	Measured between rising @ 1.5V	200	ps

Table 15.

Clock Name	Max Load (in pF) ^[6]
CPU(0:1), USB 24_48, REF (0:2)	20
PC133(0:5), PC133_F, PCI33_HT66(0:2)	30

Note:

6. The above loads are positioned near each output pin when tested.

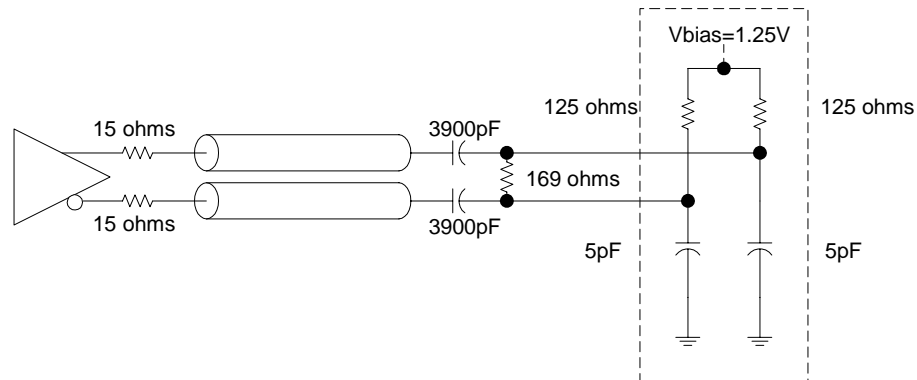


Figure 2. Test Load Configuration

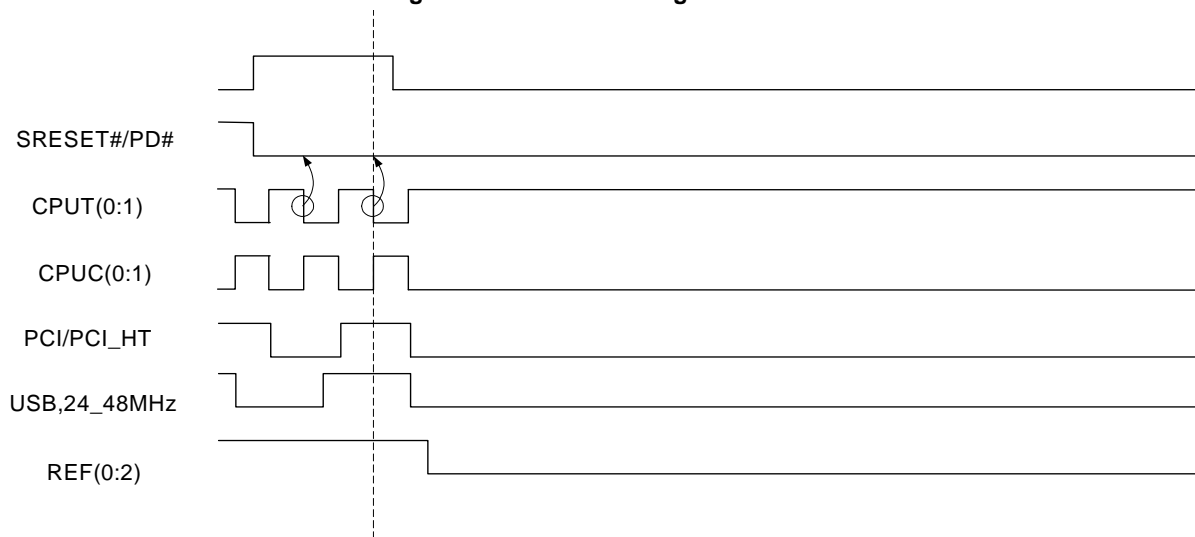


Figure 3. PD# Assertion Waveform

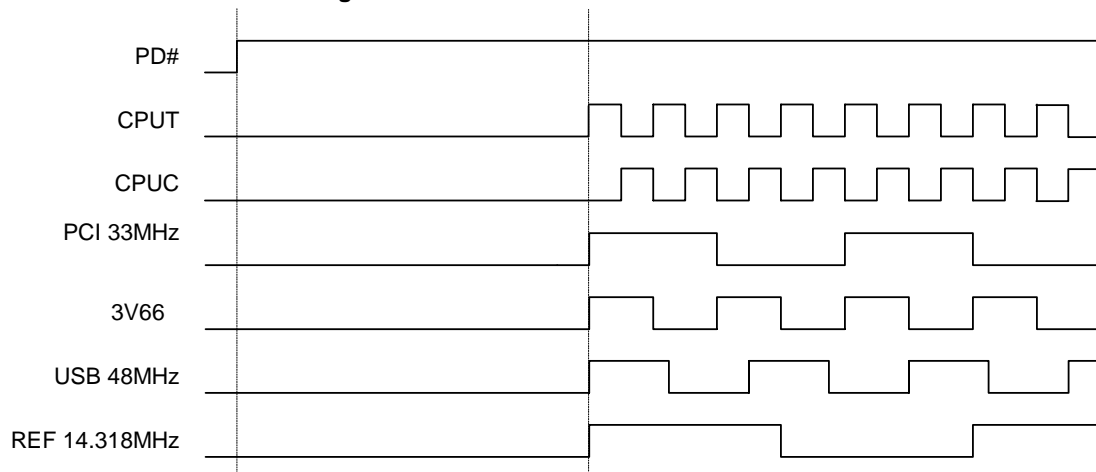


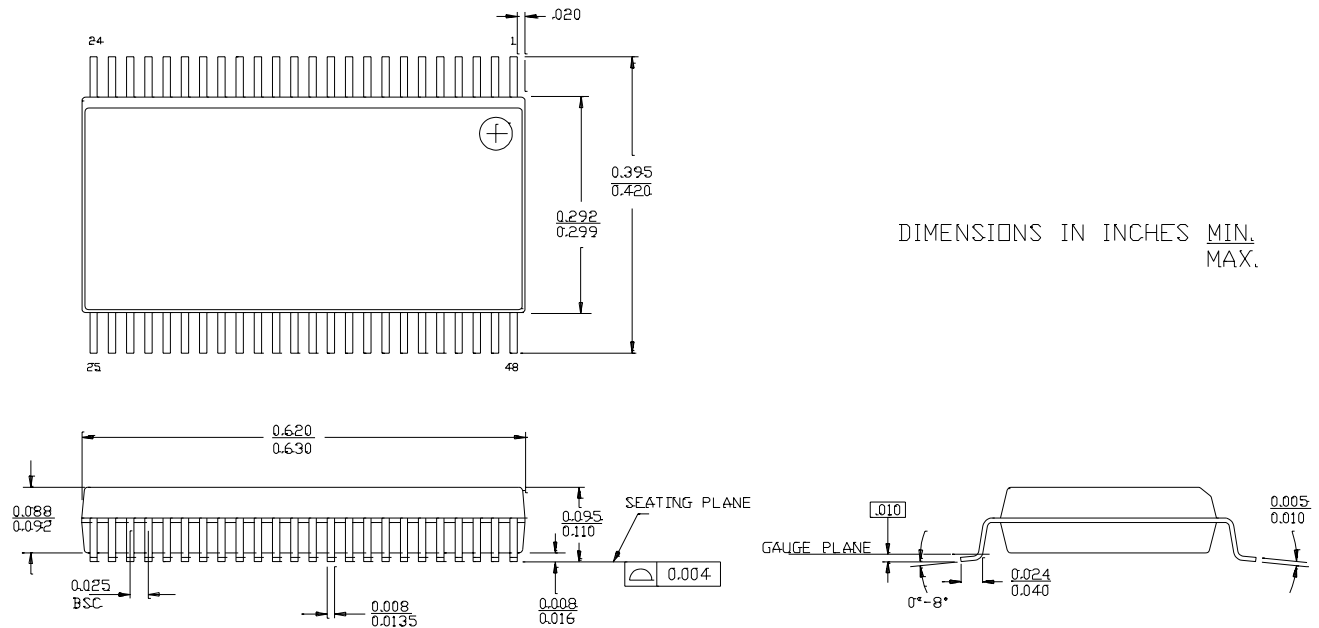
Figure 4. PD# Deassertion Waveform

Ordering Information

Part Number	Package Type	Product Flow
CY28330OC	48-pin SSOP	Commercial, 0° to 70°C
CY28330OCT	48-pin SSOP – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-lead Shrink Small Outline Package O48



51-85061-C

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Document Title: CY28330 Clock Generator for AMD™ Hammer
Document Number: 38-07366

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112782	03/01/02	DMG	New Data Sheet