



CYPRESS

CY26503

533-MHz Dual Direct Rambus™ Clock Generator

Features

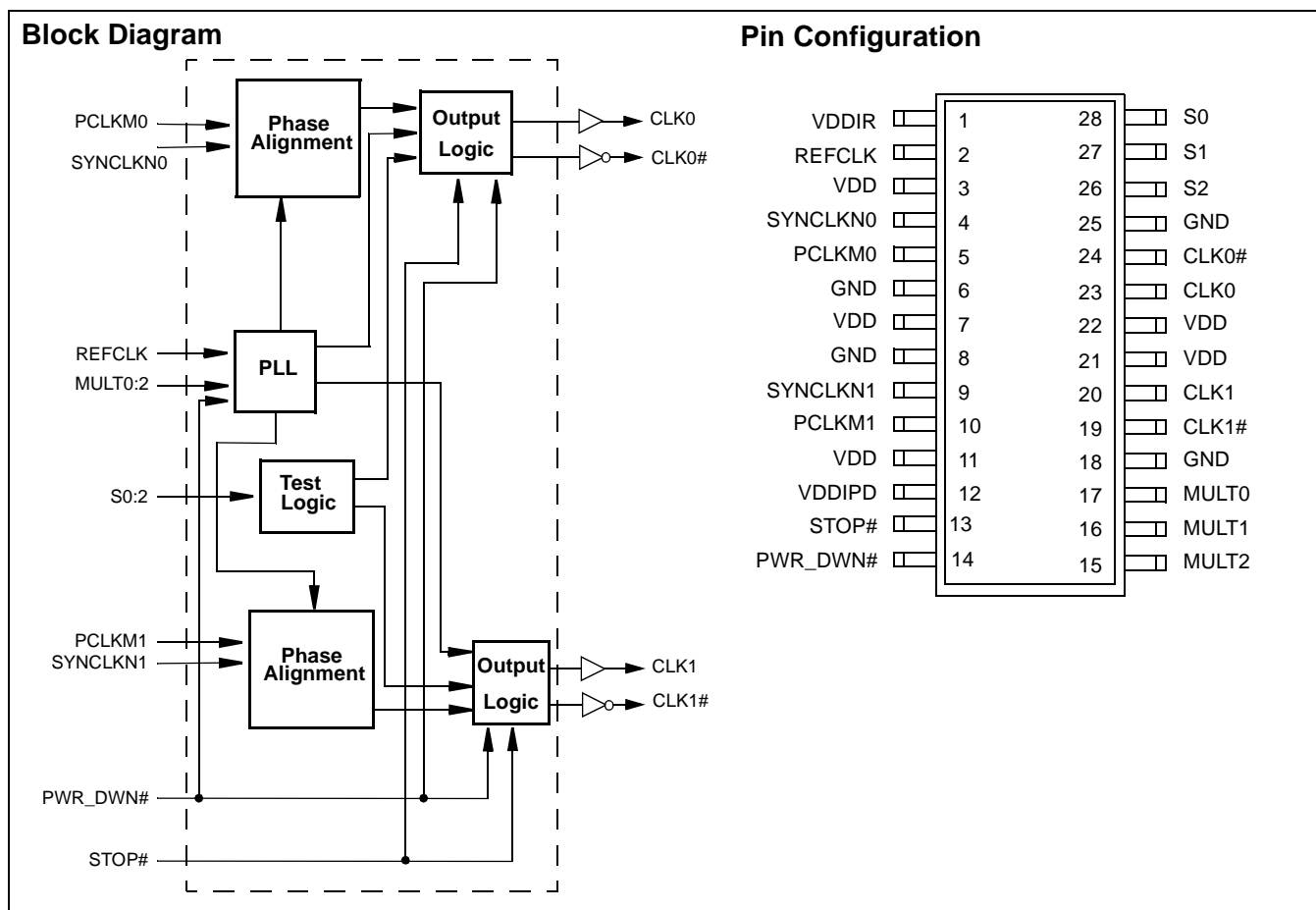
- **Differential clock source for 800-MHz and 1066-MHz Direct Rambus™ memory subsystem**
- **Provide synchronization flexibility: the Rambus® channel can also be synchronous to an external system or processor clock**
- **Power-managed output allows Rambus Channel clock to be turned off to minimize power consumption for mobile applications**
- **Low-power CMOS design packaged in a 28-pin, 173-mil TSSOP package**

Overview

The Cypress CY26503 provides dual-channel differential clock signals for a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus Channel clock to an external system clock but can also be used in systems that do not require synchronization of the Rambus clock.

Key Specifications

Supply Voltage: $V_{DD} = 3.3V \pm 0.165V$
Operating Temperature: $0^{\circ}C$ to $+70^{\circ}C$
Input Threshold: 1.5V typical
Maximum Input Voltage: $V_{DD} + 0.5V$
Maximum Input Frequency: 100 MHz
Output Duty Cycle: 40%/60% worst case
Output Type: Rambus signaling level (RSL)



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description																																													
REFCLK	2	I	Reference Clock Input: Reference clock input, normally supplied by a system frequency synthesizer (Cypress CY2220).																																													
PCLKM0:1	5, 10	I	Phase Detector Input 0:1: The phase difference between this signal and SYNCLKN is used to synchronize the Rambus Channel Clock with the system clock. Both PCLKM and SYNCLKN are provided by the Gear Ratio Logic in the memory controller. If the Gear Ratio Logic is not used, this pin would be connected to ground.																																													
SYNCLKN0:1	4, 9	I	Phase Detector Input 0:1: The phase difference between this signal and PCLKM is used to synchronize the Rambus Channel clock with the system clock. Both PCLKM and SYNCLKN are provided by the Gear Ratio Logic in the memory controller. If the Gear Ratio Logic is not used, this pin would be connected to ground.																																													
STOP#	13	I	Clock Output Enable: When this input is driven to active LOW, it disables the differential Rambus Channel clocks.																																													
PWR_DWN#	14	I	Active LOW Power-Down: When this input is driven to active LOW, it disables the differential Rambus Channel clocks and places the CY26503 in power-down mode.																																													
MULT 0:2	17, 16, 15	I	PLL Multiplier Select: These inputs select the PLL prescaler and feedback dividers to determine the multiply ratio for the PLL for the input REFCLK. <table><tr><td>MULT0</td><td>MULT1</td><td>MULT2</td><td>A</td><td>B</td></tr><tr><td>0</td><td>0</td><td>0</td><td>4</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>9</td><td>2</td></tr><tr><td>0</td><td>1</td><td>0</td><td>6</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>TBD</td><td>TBD</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8</td><td>3</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16</td><td>3</td></tr><tr><td>1</td><td>1</td><td>0</td><td>8</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>TBD</td><td>TBD</td></tr></table>	MULT0	MULT1	MULT2	A	B	0	0	0	4	1	0	0	1	9	2	0	1	0	6	1	0	1	1	TBD	TBD	1	0	0	8	3	1	0	1	16	3	1	1	0	8	1	1	1	1	TBD	TBD
MULT0	MULT1	MULT2	A	B																																												
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1	1	1	TBD	TBD																																												
CLK0, CLK0#, CLK1, CLK1#	23, 24, 20, 19	O	Complementary Output Clock: Differential Rambus Channel clock outputs.																																													
S0, S1, S2	28, 27, 26	I	Mode Control Input: These inputs control the operating mode of the CY26503. <table><tr><td>S0</td><td>S1</td><td>S2</td><td>MODE</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Normal</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Bypass</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Test</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Vendor Test A</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Vendor Test B</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>X</td><td>Output Test (OE)</td></tr></table>	S0	S1	S2	MODE	0	0	0	Normal	1	0	0	Bypass	1	1	0	Test	0	0	1	Vendor Test A	1	0	1	Vendor Test B	1	1	1	Reserved	0	1	X	Output Test (OE)													
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VDDIR	1	RefV	Reference for Refclk: Voltage reference for input reference clock.																																													
VDDIPD	12	RefV	Reference for Phase Detector: Voltage reference for phase detector inputs and STOP#.																																													
VDD	3, 7, 11, 21, 22	P	Power Connection: Power supply for core logic and output buffers. Connected to 3.3V supply.																																													
GND	6, 8, 18, 25	G	Ground Connection: Connect all ground pins to the common system ground plane.																																													

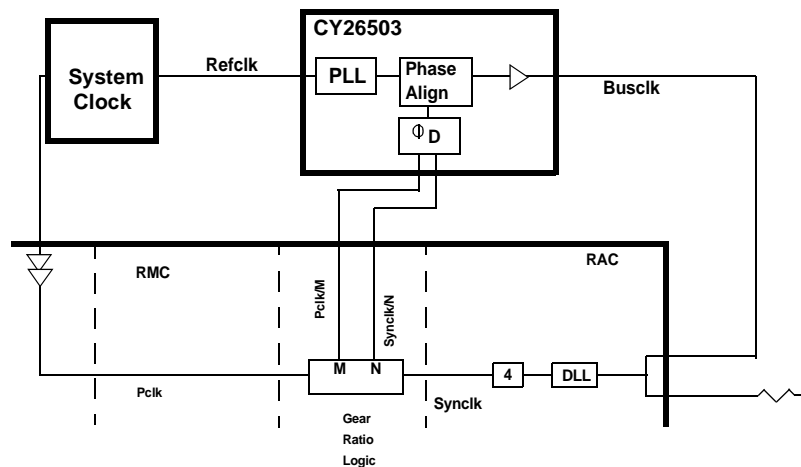


Figure 1. DDLL System Architecture

DDLL System Architecture and Gear Ratio Logic

Figure 1 shows the Distributed Delay Lock Loop (DDLL) system architecture, including the main system clock source, the Direct Rambus clock generator (DRCG), and the core logic that contains the Rambus Access Cell (RAC), the Rambus Memory Controller (RMC), and the Gear Ratio Logic. (This diagram abstractly represents the differential clocks as a single Busclk wire.)

The purpose of the DDLL is to frequency-lock and phase-align the core logic and Rambus clocks (PCLK and SYNCLK) at the RMC/RAC boundary in order to allow data transfers without incurring additional latency. In the DDLL architecture, a PLL is used to generate the desired Busclk frequency, while a distributed loop forms a DLL to align the phase of Pclk and Synclk at the RMC/RAC boundary.

The main clock source drives the system clock (Pclk) to the core logic, and also drives the reference clock (Refclk) to the DRCG. For typical Intel architecture platforms, Refclk will be half the CPU front side bus frequency. A PLL inside the DRCG multiplies Refclk to generate the desired frequency for Busclk, and Busclk is driven through a terminated transmission line (Rambus Channel). At the mid-point of the channel, the RAC senses Busclk using its own DLL for clock alignment, followed by a fixed divide-by-4 that generates Synclk.

Pclk is the clock used in the memory controller (RMC) in the core logic, and Synclk is the clock used at the core logic

interface of the RAC. The DDLL together with the Gear Ratio Logic enables users to exchange data directly from the Pclk domain to the Synclk domain without incurring additional latency for synchronization. In general, Pclk and Synclk can be of different frequencies, so the Gear Ratio Logic must select the appropriate M and N dividers such that the frequencies of Pclk/M and Synclk/N are equal. In one interesting example, Pclk = 133 MHz, Synclk = 100 MHz, and M = 4 while N = 3, giving Pclk/M = Synclk/N = 33 MHz. This example of the clock waveforms with the Gear Ratio Logic is shown in Figure 2.

The output clocks from the Gear Ratio Logic, Pclk/M, and Synclk/N, are output from the core logic and routed to the DRCG Phase Detector (ϕ_D) inputs. The routing of Pclk/M and Synclk/N must be matched in the core logic as well as on the board.

After comparing the phase of Pclk/M vs. Synclk/N, the DRCG Phase Detector (ϕ_D) drives a phase aligner that adjusts the phase of the DRCG output clock, Busclk. Since everything else in the distributed loop is fixed delay, adjusting Busclk adjusts the phase of Synclk and thus the phase of Synclk/N. In this manner the distributed loop adjusts the phase of Synclk/N to match that of Pclk/M, nulling the phase error at the input of the DRCG Phase Detector (ϕ_D). When the clocks are aligned, data can be exchanged directly from the Pclk domain to the Synclk domain.

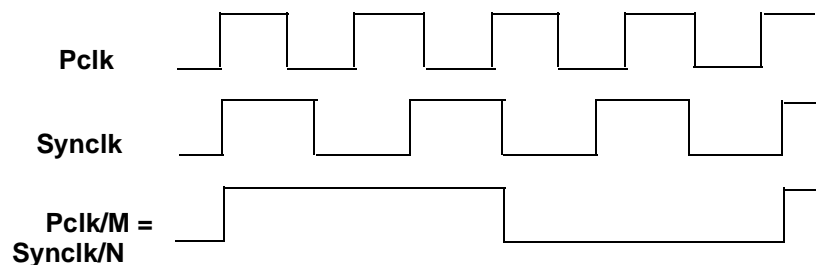


Figure 2. Gear Ratio Timing Diagram

Table 3. Bypass and Test Mode Selection

Mode	S0	S1	S2	By Pclk (int.)	CLK	CLK#
Normal	0	0	0	Gnd	PAClk	PAClk#
Bypass	1	0	0	PLLCIk	PLLCIk	PLLCIk#
Test	1	1	0	RefClk	RefClk	RefClk#
Vendor Test A	0	0	1	-	-	-
Vendor Test B	1	0	1	-	-	-
Reserved	1	1	1	-	-	-
Output Test (OE)	0	1	X	-	Hi-Z	RefClk#

Table 4 shows the logic for selecting the power-down mode, using the PWR_DWN# input signal. PWR_DWN# is active LOW (enabled when 0). When PWR_DWN# is disabled, the DRCG is in its normal mode. When PWR_DWN# is enabled, the DRCG is put into a powered-off state, and the CLK and CLK# outputs are three-stated.

Table 4. PWR_DWN# Mode Selection

Mode	PWR_DWN#	CLK	CLK#
Normal	1	PAClk	PAClk#
Power-Down	0	GND	GND

Table of Frequencies and Gear Ratios

Table 5 shows several supported Pclk and Busclk frequencies, the corresponding A and B dividers required in

Table 5. Frequencies, Dividers, and Gear Ratios

Pclk	Refclk	Busclk	Syncclk	A	B	M	N	Ratio	F@PD
67	33	267	67	8	1	2	2	1.0	33
100	50	300	75	6	1	8	6	1.33	12.5
100	50	400	100	8	1	4	4	1.0	25
133	67	267	67	4	1	4	2	2.0	33
133	67	400	100	6	1	8	6	1.33	16.7

the DRCG PLL, and the corresponding M and N dividers in the gear ratio logic. The column Ratio gives the Gear Ratio as defined Pclk/Syncclk (same as M and N). The column F@PD gives the divided down frequency (in MHz) at the Phase Detector (ϕ_D), where $F@PD = PCLK/M = SYNCCLK/N$.

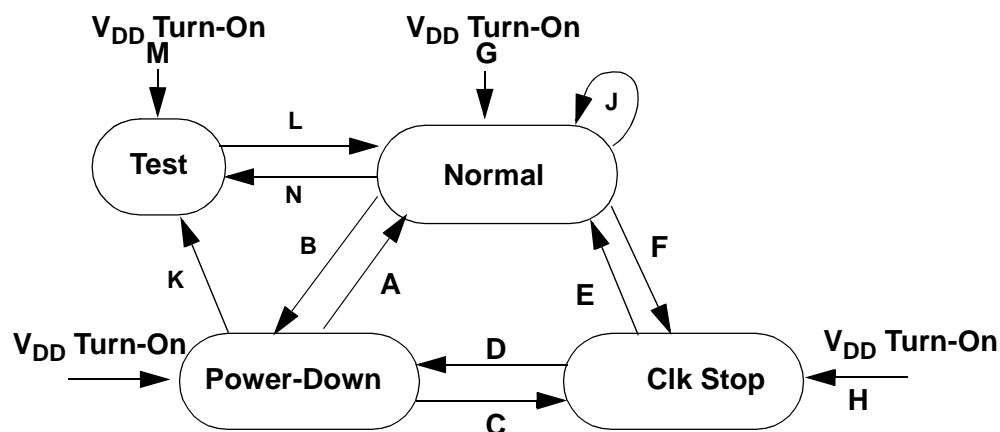
State Transitions

The clock source has three fundamental operating states. Figure 4 shows the state diagram with each transition labelled A through H. Note that the clock source output may NOT be glitch-free during state transitions.

Upon powering up the device, the device can enter any state, depending on the settings of the control signals, PWR_DWN# and STOP#.

In Power-Down mode, the clock source is powered down with the control signal, PWR_DWN#, equal to 0. The control signals S0, S1 and S2 must be stable before power is applied to the device, and can only be changed in power-down mode (PWR_DWN# = 0). The reference inputs, VDDIR and VDDIPD, may remain on or may be grounded during the power-down mode.

The control signals MULT0, MULT1, and MULT2 can be used in two ways. If they are changed during power-down mode, then the power-down transition timings determine the settling time of the DRCG. However, the MULT0, MULT1, and MULT2 control signals can also be changed during Normal mode. When the MULT control signals are "hot swapped" in this manner, the MULT transition timings determine the settling time of the DRCG.


Figure 4. Clock Source State Diagram

In Clk Stop mode, the clock source is on, but the output is disabled (STOP# asserted). The VDDIPD reference input may remain on or may be grounded during the Clk Stop mode. The VDDIR reference input must remain on during the Clk Stop mode.

In Normal mode, the clock source is on, and the output is enabled.

Table 6 lists the control signals for each state.

Table 6. Control Signals for Clock Source States

State	PWR_DWN#	STOP#	Clock Source	Output Buffer
Power-down	0	X	OFF	Ground
Clk Stop	1	0	ON	Disabled
Normal	1	1	ON	Enabled

Timing Diagrams

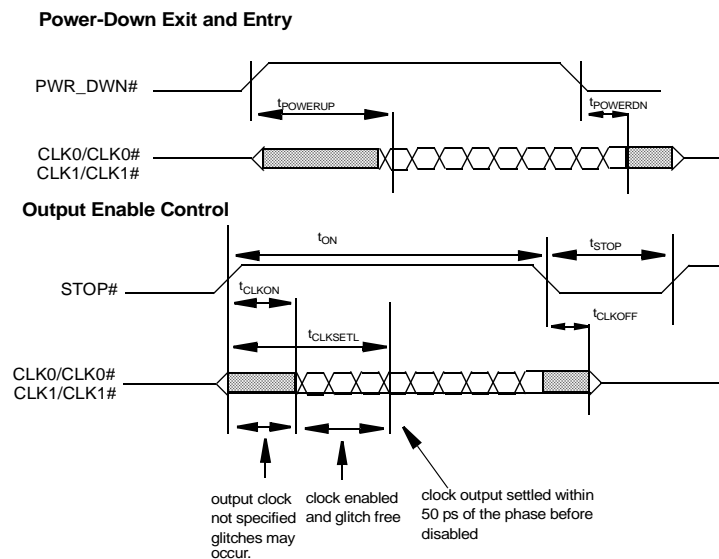


Figure 5. State Transition Timing Diagrams

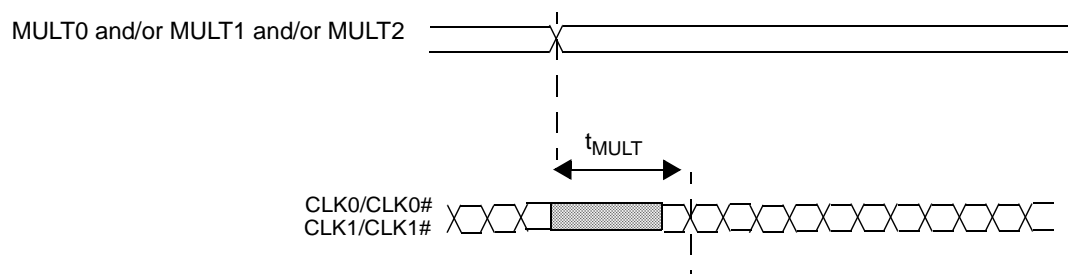


Figure 6. Multiply Transition Timing

Table 7. State Transition Latency Specifications

Transition	From	To	Transition Latency		Description
			Parameter	Max.	
A	Power-down	Normal	t_{POWERUP}	3 ms	Time from PWR_DWN# to rising edge CLK/CLK# output settled (excluding t_{DISTLOCK})
C	Power-down	Clk Stop	t_{POWERUP}	3 ms	Time from PWR_DWN# rising edge until the internal PLL and clock has turned ON and settled.
K	Power-down	Test	t_{POWERUP}	3 ms	Time from PWR_DWN# rising edge to CLK/CLK# output settled (excluding t_{DISTLOCK}).
G	V _{DD} on	Normal	t_{POWERUP}	3 ms	Time from VDD is applied and settled until CLK/CLK# output settled (excluding t_{DISTLOCK}).
H	V _{DD} on	Clk Stop	t_{POWERUP}	3 ms	Time from VDD is applied and settled until internal PLL and clock has turned ON and settled.
M	V _{DD} on	Test	t_{POWERUP}	3 ms	Time from VDD is applied and settled until internal PLL and clock has turned ON and settled.
J	Normal	Normal	t_{MULT}	1 ms	Time from when MULT0, MULT1, or MULT2 changed until CLK/CLK# output resettled (excluding t_{DISTLOCK}).
E	Clk Stop	Normal	t_{CLKON}	10 ns	Time from STOP# rising edge until CLK/CLK# provides glitch-free clock edges.
E	Clk Stop	Normal	t_{CLKSETL}	20 cycles	Time from STOP# rising edge to CLK/CLK# output settled to within 50 ps of the phase before CLK/CLK# was disabled.
F	Normal	Clk Stop	t_{CLKOFF}	5 ns	Time from STOP# falling edge to CLK/CLK# output disabled.
L	Test	Normal	t_{CTL}	3 ms	Time from when S0, S1, or S2 is changed until CLK/CLK# output has resettled (excluding t_{DISTLOCK}).
N	Normal	Test	t_{CTL}	3 ms	Time from when S0, S1, or S2 is changed until CLK/CLK# output has resettled (excluding t_{DISTLOCK}).
B,D	Normal or Clk Stop	PWR_DW N#	t_{POWERDN}	1 ms	Time from PWR_DWN# falling edge to the device in PWR_DWN#.

Figure 5 shows that the CLK Stop to Normal transition goes through three phases. During t_{CLKON} , the clock output is not specified and can have glitches. For $t_{\text{CLKON}} < t < t_{\text{CLKSETL}}$, the clock output is enabled and must be glitch-free. For $t > t_{\text{CLKSETL}}$, the clock output phase must be settled to within

50 ps of the phase before the clock output was disabled. At this time, the clock output must also meet the voltage and timing specifications of Table 13. The outputs are in a high-impedance state during the Clk Stop mode.

Table 8. Distributed Loop Lock Time Specification

Parameter	Min.	Max.	Unit	Description
t_{DISTLOCK}		5	ms	Time from when CLK/CLK# output is settled to when the phase error between SYNCLKN and PCLKM falls within the $t_{\text{ERR,PD}}$ spec in Table 13.

Table 9. Supply and Reference Current Specification

Parameter	Description	Min.	Max.	Unit
$I_{\text{POWERDOWN}}$	"Supply" current in power-down state ($\text{PWR_DWN\#} = 0$)		1.2	mA
I_{CLKSTOP}	"Supply" current in Clk Stop state ($\text{STOP\#} = 0$)		175	mA
I_{NORMAL}	"Supply" current in Normal state ($\text{STOP\#} = 1, \text{PWR_DWN\#} = 1$)		225	mA
$I_{\text{REF,PWDN}}$	Current at VDDIR or VDDIPD reference pin in PWR_DWN# state ($\text{PWR_DWN\#} = 0$)		50	μA
$I_{\text{REF,NORM}}$	Current at VDDIR or VDDIPD reference pin in Normal or Clk Stop state ($\text{PWR_DWN\#} = 1$)		4	mA

Table 10 represents stress ratings only, and functional operation at the maximums is not guaranteed.

Table 10. Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
VDD, ABS	Max. voltage on V _{DD} with respect to ground	-0.5	4.0	V
V _I , ABS	Max. voltage on any pin with respect to ground	-0.5	VDD+0.5	V

Table 11 gives the nominal values of the external components and their maximum acceptable tolerance, assuming $Z_{\text{CH}} = 28\Omega$.

Table 11. External Component Values

Parameter	Description	Test Load	Recommended Value	Tolerance	Unit
R_S	Serial Resistor	47	39	$\pm 5\%$	Ω
R_P	Parallel Resistor	47	51	$\pm 5\%$	Ω
C_F	Edge Rate Filter Capacitor	Note 1	Note 1	$\pm 10\%$	pF
C_{MID}	AC Ground Capacitor	100 pF	0.1	$\pm 20\%$	μF

Note:

- Do not populate C_F . Leave pads for future use.

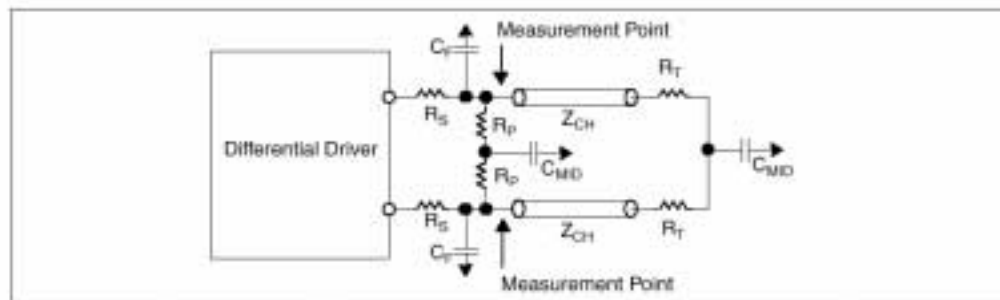
Clock Output Driver
Clock Output Driver

Figure 7. Example System Clock Driver Equivalent Circuit

Table 12. Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Operating Temperature	0	70	°C
$t_{CYCLE,IN}$	Refclk Input Cycle Time	10	40	ns
$t_{J,IN}$	Input Cycle-to-Cycle Jitter ^[2]		250	ps
DC_{IN}	Input Duty Cycle over 10,000 Cycles	40	60	% t_{CYCLE}
FM_{IN}	Input Frequency of Modulation	30	33	kHz
PM_{IN} ^[3]	Modulation Index for Triangular Modulation		0.6	%
	Modulation Index for Non-Triangular Modulation		0.5 ^[4]	%
$t_{CYCLE,PD}$	Phase Detector Input Cycle Time at PCLKM & SYNCLKN	30	100	ns
$t_{ERR,INIT}$	Initial Phase error at Phase Detector Inputs	-0.5	0.5	$t_{CYCLE,PD}$
$DC_{IN,PD}$	Phase Detector Input Duty Cycle over 10,000 Cycles	25	75	$t_{CYCLE,PD}$
$t_{I,SR}$	Input Slew Rate (measured at 20%-80% of input voltage) for PCLKM, SYNCLKN, and REFCLK	1	4	V/ns
$C_{IN,PD}$	Input Capacitance at PCLKM, SYNCLKN, and REFCLK ^[5]		7	pF
$\Delta C_{IN,PD}$	Input Capacitance matching at PCLKM and SYNCLKN ^[5]		0.5	pF
$C_{IN,CMOS}$	Input Capacitance at CMOS pins (excluding PCLKM, SYNCLKN, and REFCLK) ^[5]		10	pF
V_{IL}	Input (CMOS) Signal Low Voltage		0.3	VDD
V_{IH}	Input (CMOS) Signal High Voltage	0.7	-	VDD
$V_{IL,R}$	Refclk Input Low Voltage		0.3	V_{DDIR}
$V_{IH,R}$	Refclk Input High Voltage	0.7	-	V_{DDIR}
$V_{IL,PD}$	Input Signal Low Voltage for PD Inputs and STOP#		0.3	V_{DDIPD}
$V_{IH,PD}$	Input Signal High Voltage for PD Inputs and STOP#	0.7	-	V_{DDIPD}
V_{DDIR}	Input Supply Reference for REFCLK	1.235	3.465	V
V_{DDIPD}	Input Supply Reference for PD Inputs	1.235	2.625	V

Table 13. Device Characteristics

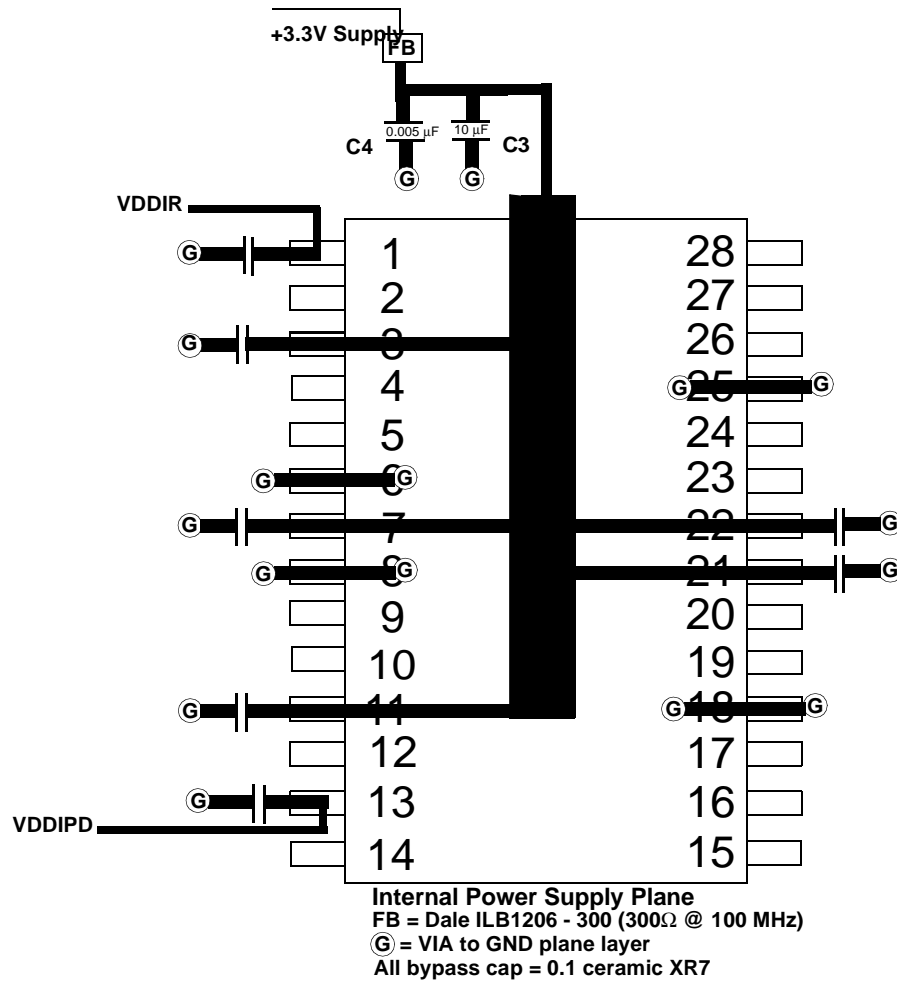
Parameter	Description	Min.	Max.	Unit
t_{CYCLE}	Clock Cycle Time	1.87	3.75	ns
t_J	Cycle-to-Cycle Jitter at CLK/CLK# ^[6]		40	ps
$V_{X,STOP}$	Output Voltage during Clk Stop (STOP#=0)	1.1	2.0	V
V_X	Differential Output Crossing-Point Voltage	1.3	1.8	V
V_{COS}	Output Voltage Swing (p-p single-ended) ^[7]	1.1	1.5	V
V_{OH}	Output High Voltage		2.5	V
V_{OL}	Output Low voltage	0.6		V
$I_{OZ,STOP}$	Output Current during Clk Stop (STOP# = 0)		500	μA
DC	Output Duty Cycle over 10,000 Cycles	40	60	% t_{CYCLE}
$t_{DC,ERR}$	Output Cycle-to-Cycle Duty Cycle Error		50	ps
t_R, t_F	Output Rise and Fall Times (measured at 20%–80% of output voltage)	300	550	ps
$t_{CR,CF}$	Difference between Output Rise and Fall Times on the Same Pin of a Single Device (20%–80%)		100	ps

Notes:

- Refclk jitter measured at $V_{DDIR}(\text{nom})/2$.
- If input modulation is used: input modulation is allowed but not required.
- The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew, which cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.
- Capacitance measured at Freq = 1 MHz, DC bias = 0.9V and $V_{AC} < 100$ mV.
- Output Jitter spec measured at $t_{CYCLE} = 1.87$ ns.
- $V_{COS} = V_{OH} - V_{OL}$.

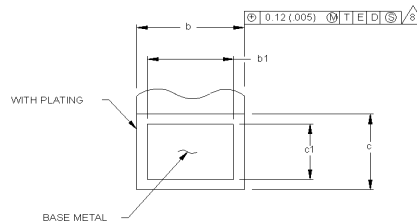
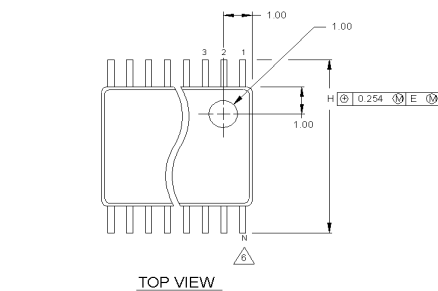
Ordering Information

Ordering Code	Package Type	Temperature Range
CY26503ZC	28-pin TSSOP (173 mils)	0°C to 70°C, Commercial

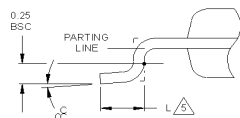
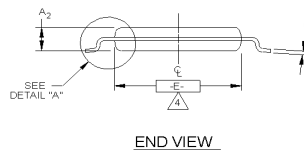
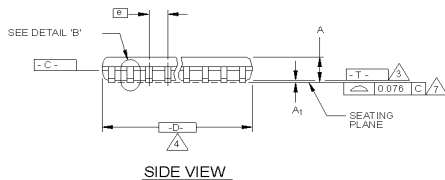
Layout Example


Package Diagram

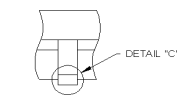
28-pin Thin Small Shrink Outline Package (TSSOP, 173 mils)



(SEE NOTE 9)



(SCALE: 30/1)



(SCALE: 30/1)
DAMBAR PROTRUSION

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.275±0.0127 (0.0110±0.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1992.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS "B" AND "C".
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A			1.10	AA	2.90	3.00	3.10	8
A ₁	0.05	0.10	0.15	AB	4.90	5.00	5.10	14
A ₂	0.85	0.90	0.95	AC	4.90	5.00	5.10	16
b	0.19	-	0.30	AD	6.40	6.50	6.60	20
b ₁	0.19	0.22	0.25	AE	7.70	7.80	7.90	24
c	0.090	-	0.20	AF	9.60	9.70	9.80	28
c ₁	0.090	0.127	0.135					
D	SEE VARIATIONS			4				
E	4.30	4.40	4.50	4				
e	0.65 BSC							
H	6.25	6.40	6.50					
L	0.50	0.60	0.70	5				
N	SEE VARIATIONS			6				
α	0°	4°	8°					

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A			.0433	AA	.114	.118	.122	8
A ₁	.002	.004	.006	AB	.193	.197	.201	14
A ₂	.0335	.0354	.0374	AC	.193	.197	.201	16
b	.0075	-	.0118	AD	.252	.256	.260	20
b ₁	.0075	.0087	.0098	AE	.303	.307	.311	24
c	.0035	-	.0079	AF	.378	.382	.386	28
c ₁	.0035	.0050	.0053					
D	SEE VARIATIONS			4				
E	.169	.173	.177	4				
e	.0256 BSC							
H	.246	.252	.256					
L	.020	.024	.028	5				
N	SEE VARIATIONS			6				
α	0°	4°	8°					

VARIATION AF IS DESIGNED BUT NOT TOOLED

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