



CYPRESS

PRELIMINARY

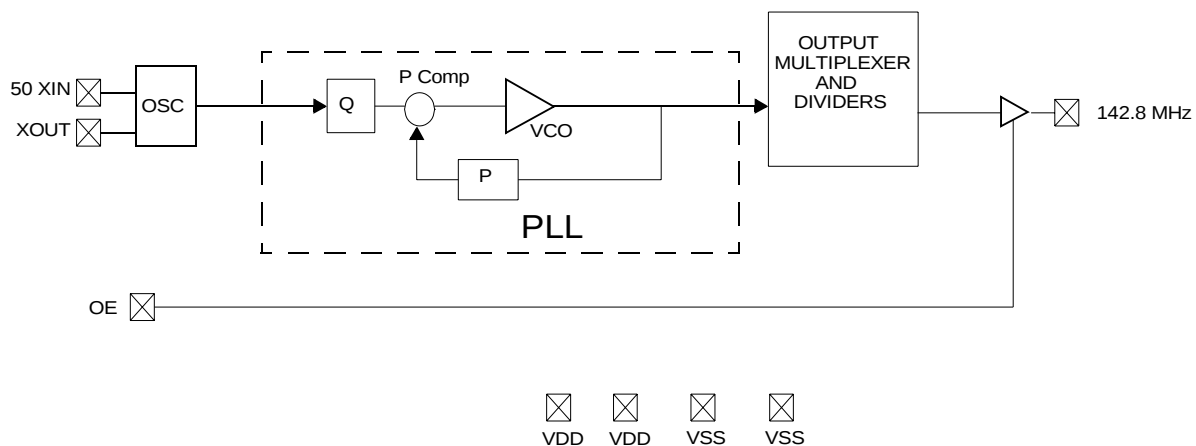
CY26187-2

Broadcom Reference Design Clock Generator

Features	Benefits
• Integrated phase-locked loop	Highest Performance PLL tailored for multimedia applications
• Low skew, low jitter, high accuracy outputs	Meets critical timing requirements in complex system designs
• 3.3V Operation	

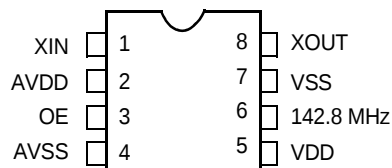
Part Number	Outputs	Broadcom Reference Design	Input Frequency	Output Frequencies
CY26187-2	1	BCM5680_5404	50 MHz	1 copy of 142.8 MHz (3.3V)

Logic Block Diagram



Pin Configuration

CY26187 8-pin SOIC



Summary

Name	Pin Number	Description
XIN ^[1]	1	Reference Crystal Input
AVDD	2	Analog Voltage Supply
OE	3	Output enable (0-off; 1-on)
AVSS	4	Ground
VDD	5	Voltage Supply
142.8 MHz	6	142.8-MHz clock output
VSS	7	Ground
XOUT ^[1]	8	Reference Crystal Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage		7.0	V
T _S	Storage Temperature ^[2]	–65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} – 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} – 0.3	V _{DD} + 0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0		70	C
C _{LOAD}	Max. Load Capacitance			15	pF
P _{max}	Max. Output Power Dissipation, 8-pin package			150	mW
f _{REF}	Reference Frequency		50		MHz

DC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
	Output High Current	V _{OH} = V _{DD} – 0.5, V _{DD} = 3.3V	12	24		mA
	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V	12	24		mA
	Input Capacitance				7	pF
	Input Leakage Current			5		μA
	I _{VDD}	3.3V, All outputs @ 10 MHz			35	mA

Notes:

1. Float XOUT pin if XIN is driven by reference clock (as opposed to crystal).
2. Rated for 10 years.

AC Electrical Characteristics (VDD = 3.3V) ^(3.)

Parameter	Name	Description	Min.	Typ.	Max.	Unit
	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V _{DD}	45	50	55	%
t3	Rising Edge Slew Rate	Output Clock Rise Time, 20%-80% of V _{DD}	0.8	1.4		V/ns
t4	Falling Edge Slew Rate	Output Clock Fall Time, 80% to 20% of V _{DD}	0.8	1.4		V/ns
t9	Clock Jitter	Peak to Peak period jitter			200	ps
t10	PLL Lock Time				3	ms

Note:

3. Not 100% tested.

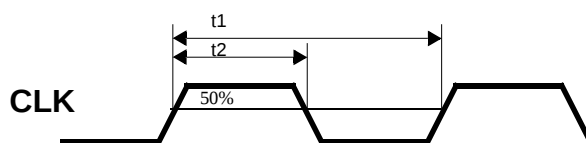
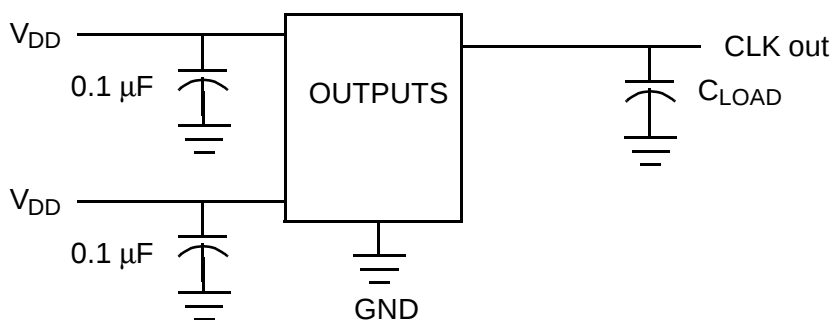
Test Circuit


Figure 1. Duty Cycle Definition; DC = t2/t1.

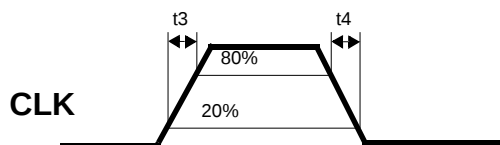


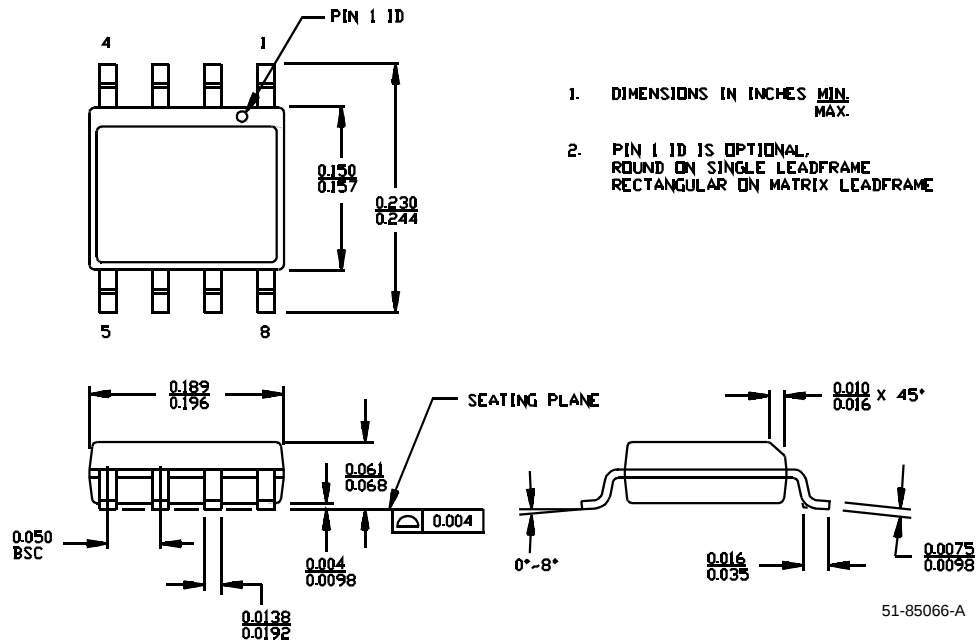
Figure 2. Rise and Fall Time Definitions.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26187SC-2	S8	8-Pin SOIC	Commercial	3.3V

Package Diagram

8-Lead (150-Mil) SOIC S8





Revision History

Document Title: CY26187-2 Broadcom Reference Design Clock Generator Document Number: 38-07131				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110096	02/19/02	CKN	New data sheet



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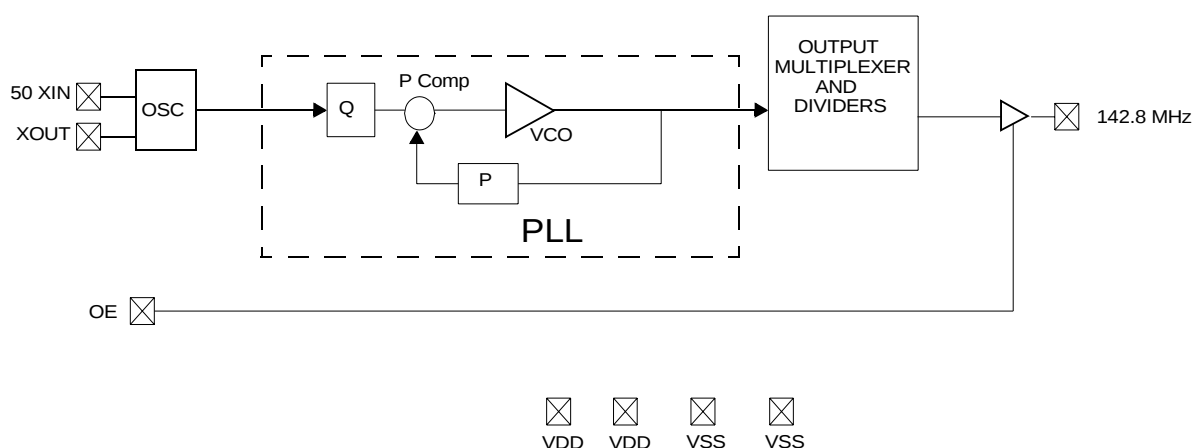
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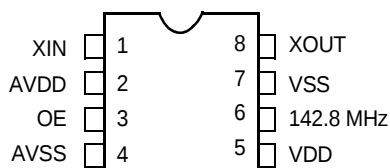
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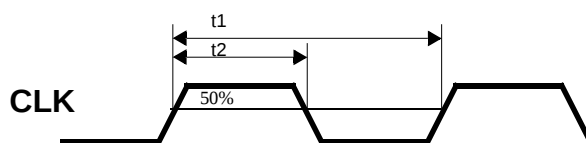
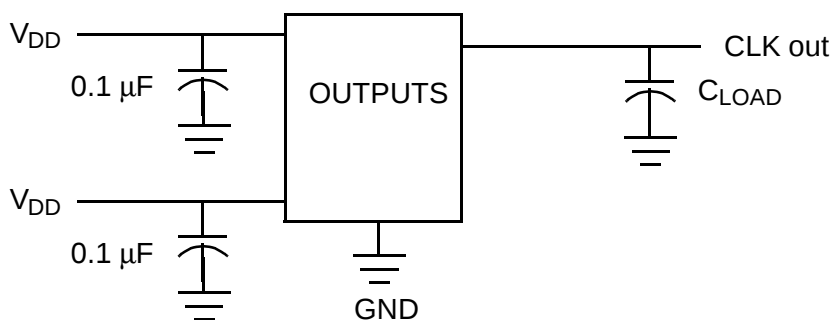
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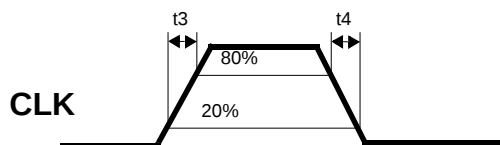


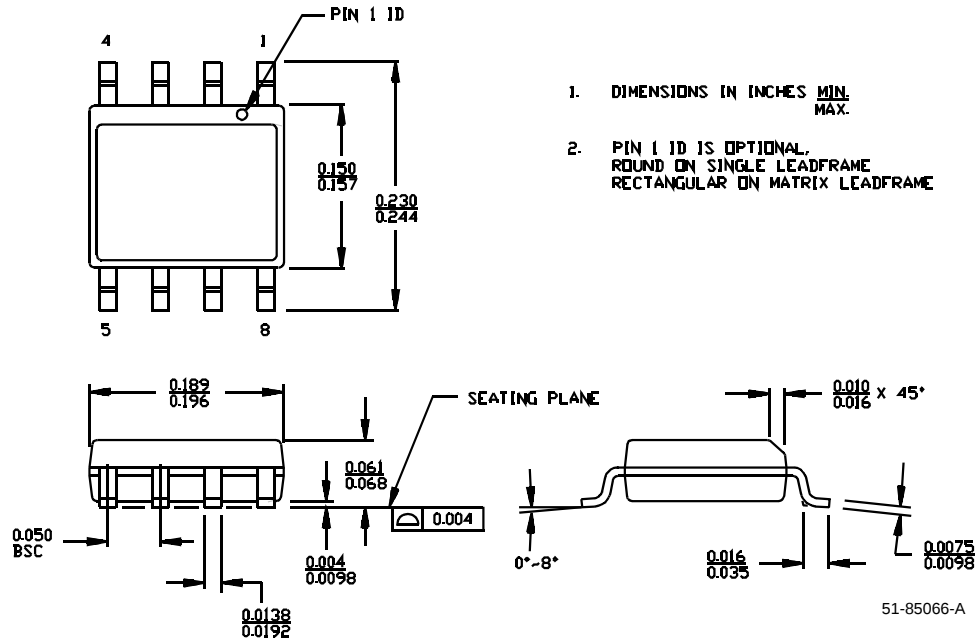
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