



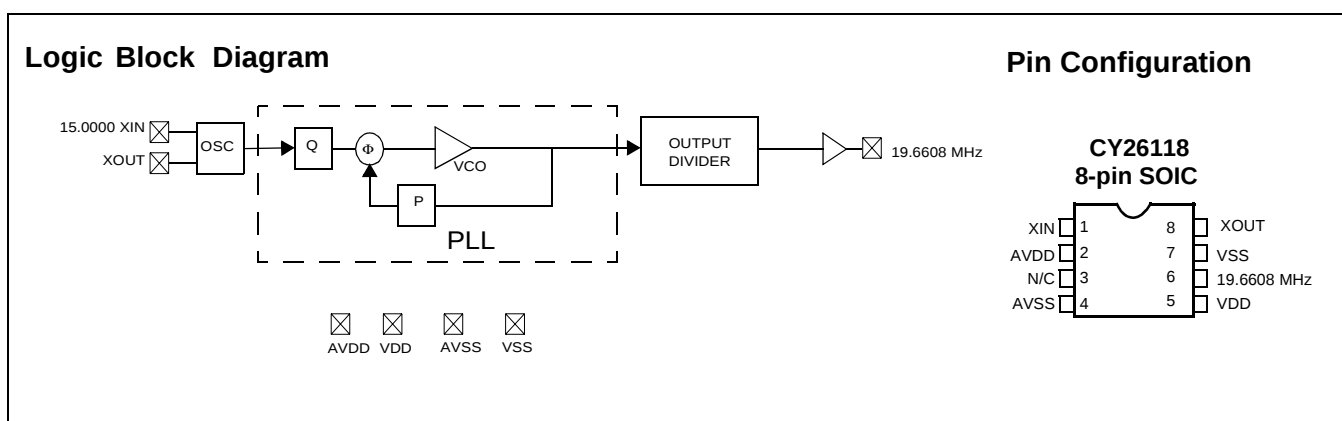
PRELIMINARY

CY26118

19.6608-MHz Clock Generator

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• 3.3V operation	

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY26118	1	15.0000 MHz	19.6608 MHz



Pin Summary

Name	Pin Number	Description
X _{IN}	1	15.000 MHz Reference Crystal Input
A _{VDD}	2	Analog Voltage Supply
N/C	3	No Connect
A _{VSS}	4	Analog Ground
V _{DD}	5	Output Voltage Supply
19.6608 MHz	6	19.6608-MHz clock output
V _{SS}	7	Output Ground
X _{OUT} ^[1]	8	Reference Crystal Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	° C
T _J	Junction Temperature		125	° C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electro-Static Discharge		2000	V

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	3.0	3.3	3.6	V
T _A	Ambient Temperature	0		70	° C
C _{LOAD}	Max Load Capacitance			15	pF
P _{max}	Max Output Power Dissipation, 8-pin package			150	° C/W
f _{REF}	Reference Frequency		15.000		MHz

DC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} = 3.3V	12	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V	12	24		mA
C _{IN}	Input Capacitance				7	pF
I _{IZ}	Input Leakage Current			5		mA
I _{DD}	Supply Current	Sum of Core and Output Current			20	mA

Notes:

1. Float X_{OUT} if X_{IN} is externally driven.
2. Rated for 10 years.

AC Electrical Characteristics ($V_{DD} = 3.3V$)

Parameter ^[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time 20% - 80% of V_{DD}	0.8	1.8		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time 80% to 20% of V_{DD}	0.8	1.8		V/ns
t_9	Clock Jitter	Peak-to-Peak period jitter		200		ps
t_{10}	PLL Lock Time				3	ms

Note:

3. Not 100% tested.

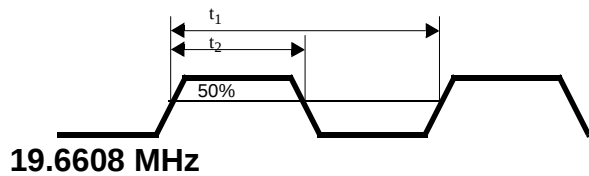


Figure 1. Duty Cycle Definition; $DC = t_2/t_1$

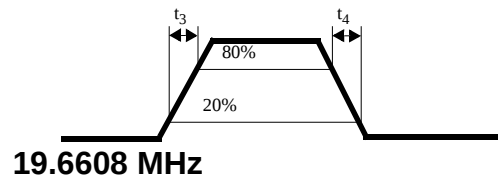
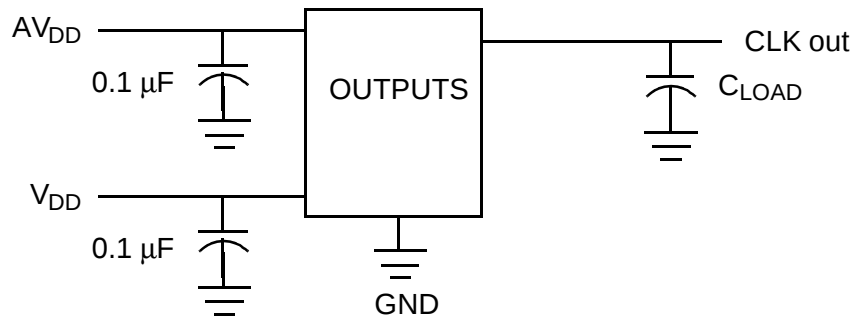


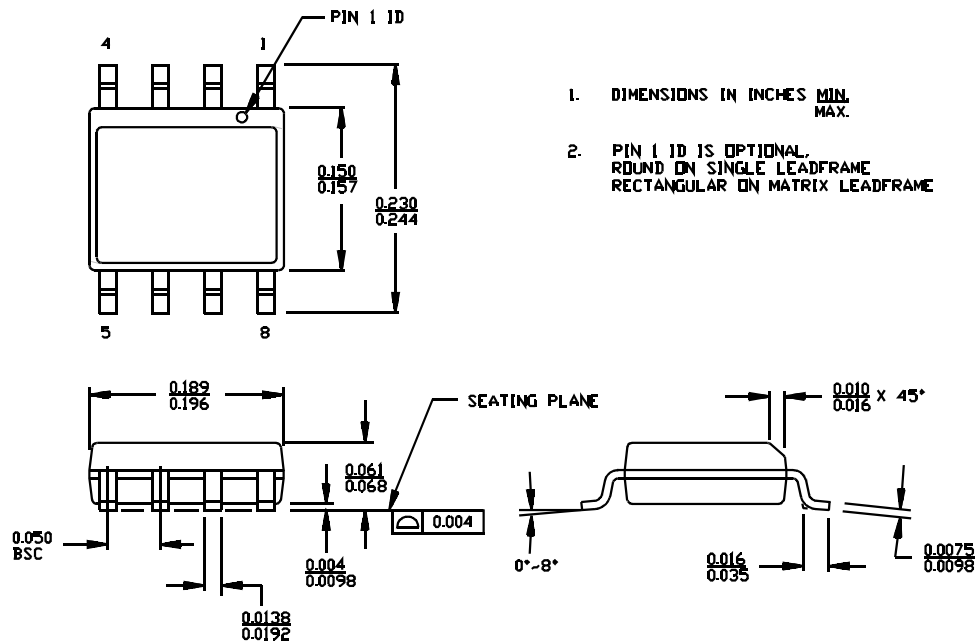
Figure 2. Rise and Fall Time Definitions

Test Circuit

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26118SC	S8	8-Pin SOIC	Commercial	3.3V

Pin Diagrams

8-Lead (150-Mil) SOIC S8





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CY26118

Document Title: CY26118 19.6608-MHz Clock Generator Document Number: 38-07274				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110764	02/06/02	CKN	New Data Sheet