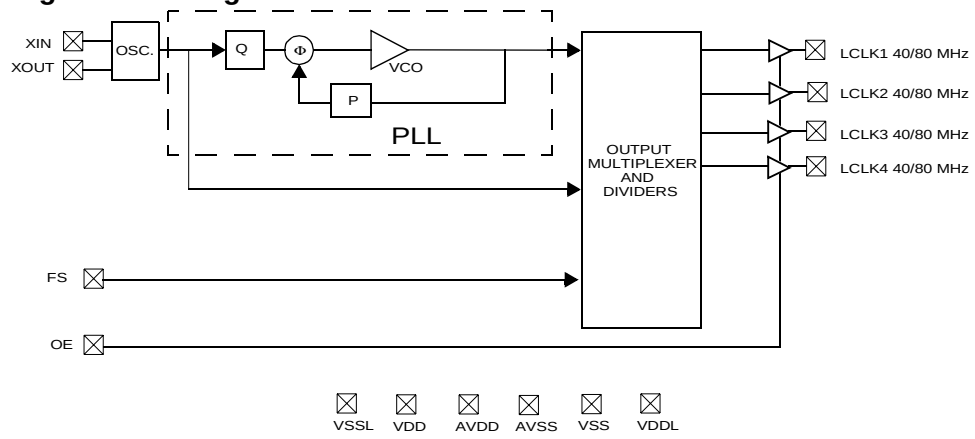
CY26113

One-PLL General Purpose Clock Generator

Features	Benefits
• **Integrated phase-locked loop**	Internal PLL with up to 333 MHz internal operation
• **Low skew, low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **Frequency Select Pin**	Dynamic frequency selection
• **3.3V Operation with 2.5V output options**	Enables application compatibility
• **16-TSSOP**	Industry standard package saves on board space

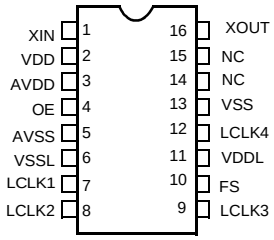
Part Number	Outputs	Input Frequency	Output Frequency Range
CY26113	4	25 MHz	4 x 40/80 MHz (selectable)

Logic Block Diagram



Pin Configurations

CY26113
16-pin TSSOP



Output	Pin	Default Frequency	Unit
LCLK 1	7	40/80 (selectable)	MHz
LCLK 2	8	40/80 (selectable)	MHz
LCLK 3	9	40/80 (selectable)	MHz
LCLK 4	12	40/80 (selectable)	MHz

Pin Definitions

Name	Pin Number	Description
XIN	1	Reference Input
VDD	2	Voltage Supply
AVDD	3	Analog Voltage Supply
OE	4	Output Enable, OE = 0 three-state; OE = 1 active
AVSS	5	Analog Ground
VSSL	6	LCLK Ground
LCLK1	7	Clock output 1–40/80 MHz
LCLK2	8	Clock output 2–40/80 MHz
LCLK3	9	Clock output 3–40/80 MHz
FS	10	Frequency Select Pin - FS = 0: 40 MHz. FS = 1: 80 MHz
VDDL	11	LCLK Voltage Supply (2.5V or 3.3V)
LCLK4	12	Clock output 4–40/80 MHz
VSS	13	Ground
NC	14	No Connect - Reserved
NC	15	No Connect - Reserved
XOUT[1]	16	Reference Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage		7.0	V
T_J	Junction Temperature		125	°C
	Digital Inputs	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DDL}	V_{SS} – 0.3	V_{DDL} +0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	3.0	3.3	3.6	V
VDDL	Operating Voltage	2.375	2.5	2.625	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance VDD/VDDL=3.3V			15	pF
C_{LOAD}	Max. Load Capacitance VDDL=2.5V			15	pF
f_{REF}	Driven Reference Frequency		25		MHz

Note:
1. Float XOUT if XIN is externally driven

DC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL}=3.3V$	12	24		mA
I_{OH}	Output High Current	$V_{OH} = V_{DDL} – 0.5$, $V_{DDL}=2.5V$	8	16		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5V$	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
C_{IN}	Input Capacitance	OE and FS Pins			7	pF
I_{IZ}	Input Leakage Current	OE and FS Pins		5		µA
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			22	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL}=3.6V$)			25	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL}=2.625V$)			20	mA

AC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
DC		Duty Cycle is defined in Figure 2; t1/t2 @ 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of $V_{DD}/V_{DDL} = 3.3V$	0.8	1.4		V/ns
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of $V_{DD}/V_{DDL} = 3.3V$	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t5	Skew	Delay between related outputs at rising edge			250	ps
t9	Clock Jitter	Peak to Peak period jitter			250	ps
t10	PLL Lock Time				3	ms

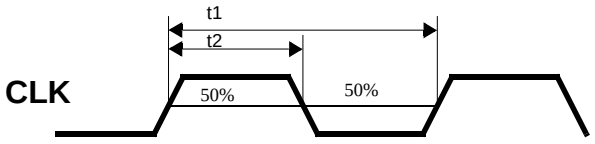


Figure 1. Duty Cycle Definition; DC = t2/t1.

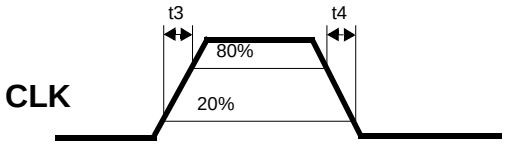
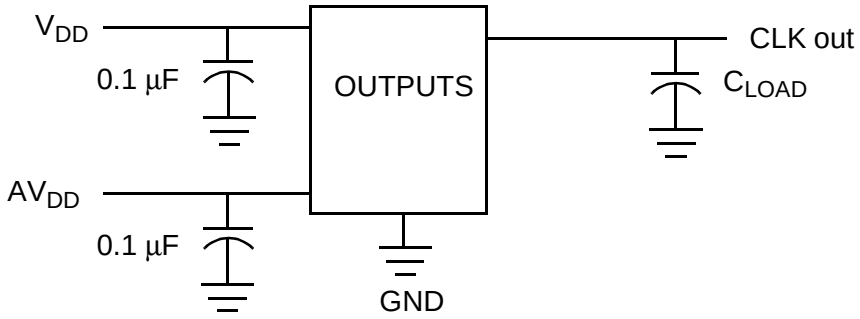


Figure 2. Rise and Fall Time Definitions.

Note:
2. Not 100% tested.

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26113ZC	Z16	16-Pin TSSOP	Commercial	3.3V

Document Title: CY26113 One-PLL General-Purpose Clock Generator Document Number: 38-07097				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107332	08/28/01	CKN	New Data Sheet