



Spread Spectrum Clock Generator

Pin Description

Pin	Name	Type	Description
1	Xin/CLK	I	Clock or Crystal connection input. Refer to <i>Table 1</i> for input frequency range selection.
2	VDD	P	Positive power supply.
3	GND	P	Power supply ground.
4	SSCLK	O	SSCG Modulated clock output.
5	SSCC	I	Spread Spectrum Clock Control (Enable/Disable) function. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally.
6	S1	I	Tri-level Logic input control pin used to select frequency and bandwidth. Frequency/bandwidth selection and tri-level logic programming. See <i>Figure 1</i> . Pin 6 has internal resistor divider network to V_{DD} and V_{SS} . Refer to <i>Block Diagram on page 1</i> .
7	S0	I	Tri-level Logic input control pin used to select Frequency and Bandwidth. Frequency/bandwidth selection and Tri-level Logic programming. See <i>Figure 1</i> . Pin 7 has internal resistor divider network to V_{DD} and V_{SS} . Refer to <i>Block Diagram on page 1</i> .
8	Xout	O	Oscillator output pin connected to crystal. Leave this pin unconnected If an external clock drives Xin/CLK.

General Description

The **CYPRESS CY25562** is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing electromagnetic interference (EMI) found in today's high-speed digital electronic systems.

The CY25562 uses a CYPRESS proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies of clock (SSCLK) is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading system performance.

The CY25562 is a very simple and versatile device to use. The frequency and spread % range is selected by programming S0 and S1 digital inputs. These inputs use three (3) logic states including High (H), Low (L), and Middle (M) logic levels to

select one of the nine available Spread % ranges. Refer to *Table 1* for programming details.

The CY25562 is intended for applications with a reference frequency in the range of 50 to 200 MHz.

A wide range of digitally selectable spread percentages is made possible by using tri-level (High, Low, and Middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread Spectrum Clock Control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

The CY25562 is available in an eight-pin SOIC package with a 0 to 70°C operating temperature range.

Refer to the CY25561 for applications with lower drive requirements and the CY25560 with lower drive and frequency requirements.

Table 1. Frequency and Spread % Selection (Center Spread)

50-100 MHz (Low Range)

Input Frequency (MHz)	S1=M S0=M (%)	S1=M S0=0 (%)	S1=1 S0=0 (%)	S1=0 S0=0 (%)	S1=0 S0=M (%)
50 - 60	4.3	3.9	3.3	2.9	2.7
60 - 70	4.0	3.6	3.1	2.6	2.5
70 - 80	3.8	3.4	2.9	2.5	2.4
80 - 100	3.5	3.1	2.7	2.2	2.1

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

100-200 MHz (High Range)

Input Frequency (MHz)	S1=1 S0=M (%)	S1=0 S0=1 (%)	S1=1 S0=1 (%)	S1=M S0=1 (%)
100 - 120	3.0	2.4	1.6	1.3
120 - 130	2.7	2.1	1.4	1.1
130 - 140	2.6	2.0	1.3	1.1
140 - 150	2.6	2.0	1.3	1.1
150 - 160	2.5	1.8	1.2	1.0
160 - 170	2.4	1.8	1.2	1.0
170 - 180	2.4	1.8	1.2	1.0
180 - 190	2.3	1.7	1.1	0.9
190 - 200	2.3	1.6	1.1	0.9

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

Tri-level Logic

With binary logic, four states can be programmed with two control lines, whereas tri-level logic can program nine logic states using two control lines. Tri-level logic in the CY25562 is implemented by defining a third logic state in addition to the standard logic “1” and “0.” Pins 6 and 7 of the CY25562 recognize a logic state by the voltage applied to the respective pin. These states are defined as “0” (Low), “M” (Middle), and

“1” (One). Each of these states have a defined voltage range that is interpreted by the CY25562 as “0,” “M,” or “1” logic state. Refer to *Table 2* for voltage ranges for each logic state. The CY25562 has two equal value resistors connected internally to pin 6 and pin 7, which produce the default “M” state. Pins 6 and/or 7 can be tied directly to ground or V_{DD} to program a logic “0” or “1” state, respectively. See examples below.

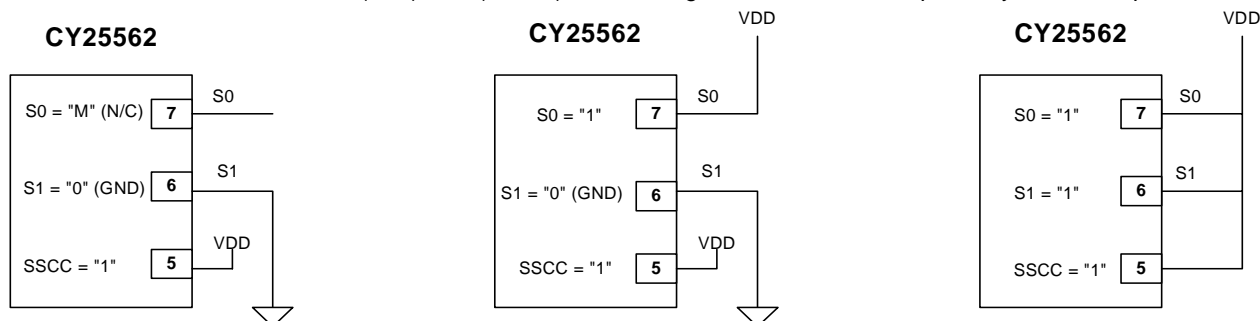


Figure 1. Tri-level Logic Examples

SSCG Theory of Operation

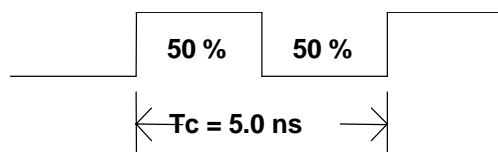
The CY25562 is a PLL-type clock generator using a proprietary Cypress design to modulate the reference clock. By precisely controlling the bandwidth of the output clock, the CY25562 becomes a low-EMI clock generator. The theory and detailed operation of the CY25562 will be discussed in the following sections.

EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of this 50/50-duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; third, fifth, seventh, etc. It is possible to reduce the amount of energy contained in the fundamental and odd harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI use shielding, filtering, multi-layer PCBs, etc. The CY25562 reduces the peak energy in the clock by increasing the clock bandwidth, thus lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The CY25562 takes a narrow band digital reference clock in the range of 50–200 MHz and produces a clock that sweeps between a controlled start (F1) and stop (F2) frequency at a precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 200 MHz clock with a 50 % duty cycle. From a 200-MHz clock we know the following:



Clock Frequency = $f_c = 200 \text{ MHz}$

Clock Period = $T_c = 1/200 \text{ MHz}$

If this clock is applied to the Xin/CLK pin of the CY25562, the output clock at pin 4 (SSCLK) will be sweeping back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate the total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition, sweep, from F1 to F2, the amount of time and sweep waveform become a very important factor in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. *Figure 2* shows the modulation profile of a 200-MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. *Figure 2* also shows a scan of the same SSCG clock using a spectrum analyzer. The spectrum analyzer scan shows a 10-dB reduction in the peak RF energy when using the CY25562 SSCG clock.

Modulation Rate

Spread Spectrum clock generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (F_{max}) and minimum frequency of the clock (F_{min}) determine this band of frequencies. The time required to transition from F_{min} to F_{max} and back to F_{min} is the period of the Modulation Rate, T_{mod} . Modulation Rates of SSCG clocks are generally referred to in terms of frequency or $F_{mod} = 1/T_{mod}$.

The input clock frequency, F_{in} , and the internal divider count, C_{div} , determine the Modulation Rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. The CY25562 has a fixed divider count of 2332.

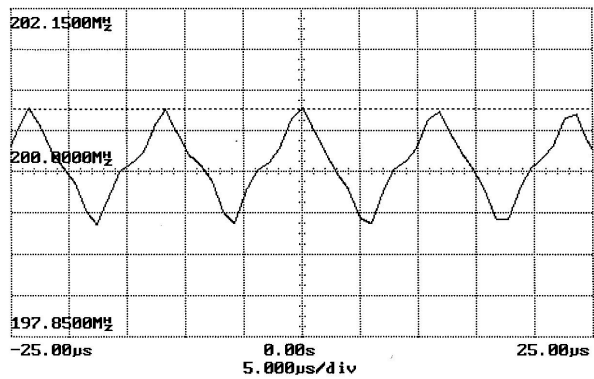
Device CY25562 **Cdiv** 2332 (All Ranges)

Example:

Device = CY25562
 Fin = 200 MHz
 Range = S1 = 1, S0 = 1

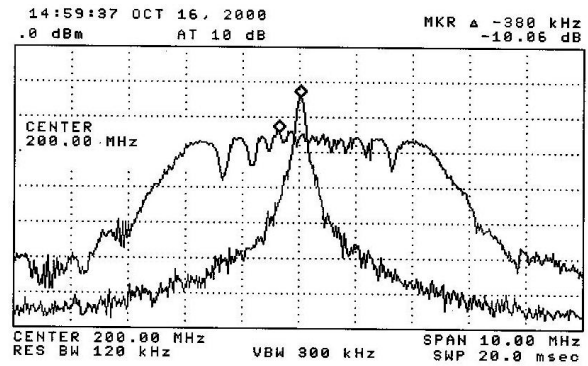
Then;

Modulation Rate = Fmod = 200 MHz/2332 = 85.7 kHz.



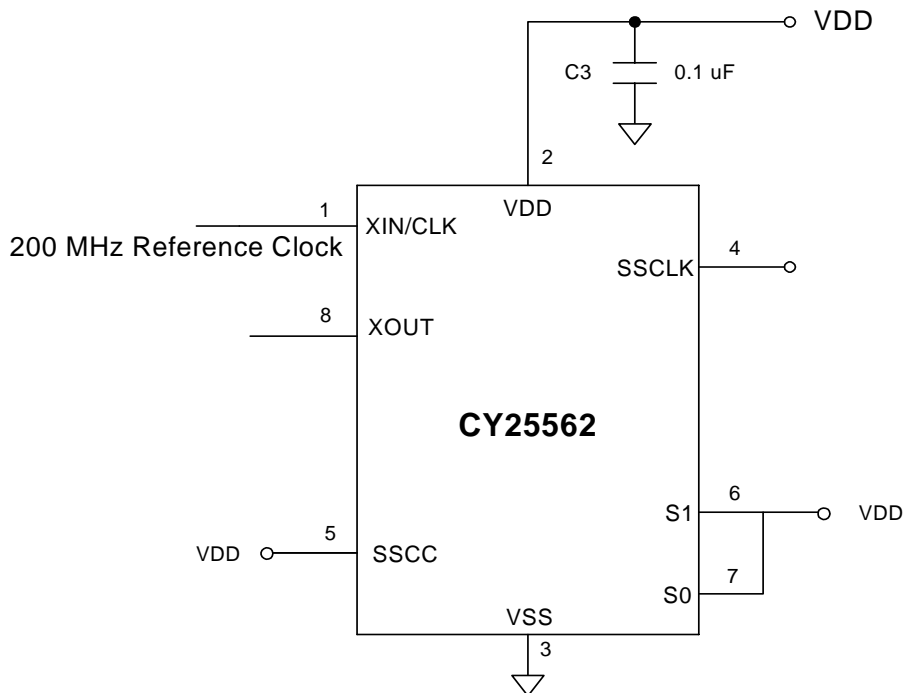
Min	199.311MHz	Max	200.840MHz
Rate	85.36kHz	Pk-Pk	1.529MHz

Modulation Profile



Spectrum Analyzer

Figure 2. SSCG Clock, CY25562, Fin = 200 MHz

CY25562 Application Schematic

Figure 3. Application Schematic

The schematic in *Figure 3* above demonstrates how the CY25562 is configured in a typical application. This application is using a 200-MHz reference clock connected to pin 1. Because an external reference clock is used, pin 8 (Xout) is left unconnected.

This configuration depicts the profile and spectrum scans shown in *Figure 2*. Note that $S0 = S1 = 1$, for a spread of approximately 1.1%.

Absolute Maximum Ratings^[1]

Supply Voltage (AV_{DD} or DV_{DD}):+6V Operating Temperature:..... 0°C to 70°C
 $AV_{DD} - DV_{DD}$:±300 mV Storage Temperature -65°C to +150°C
 $AG_{ND}-DG_{ND}$ ±300 mV

Table 2. DC Electrical Characteristics $V_{DD} = 3.3V$, Temp. = 25°C, and C_L (Pin 4) = 15 pF unless otherwise noted

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Range	±10%	2.97	3.3	3.63	V
V_{INH}	Input High Voltage	S0 and S1 only.	$0.85V_{DD}$	V_{DD}	V_{DD}	V
V_{INM}	Input Middle Voltage	S0 and S1 only.	$0.40V_{DD}$	$0.50V_{DD}$	$0.60V_{DD}$	V
V_{INL}	Input Low Voltage	S0 and S1 only.	0.0	0.0	$0.15V_{DD}$	V
V_{OH1}	Output High Voltage	$I_{OH} = 6$ ma	2.4			V
V_{OH2}	Output High Voltage	$I_{OH} = 20$ ma	2.0			V
V_{OL1}	Output Low Voltage	$I_{OH} = 6$ ma			0.4	V
V_{OL2}	Output Low Voltage	$I_{OH} = 20$ ma			1.2	V
C_{in1}	Input Capacitance	Xin/CLK (Pin 1)	3	4	5	pF
C_{in2}	Input Capacitance	Xout (Pin 8)	6	8	10	pF
C_{in2}	Input Capacitance	S0, S1, SSCC (Pins 7,6,5)	3	4	5	pF
I_{DD1}	Power Supply Current	FIN = 65 MHz, CL = 15 pF		23	30	mA
I_{DD2}	Power Supply Current	FIN = 200 MHz, CL = 15 pF		53	66	mA
I_{DD3}	Power Supply Current	FIN = 200 MHz, No Load		48	60	mA

Table 3. Electrical Timing Characteristics $V_{DD} = 3.3V$, T = 25°C, and $C_L = 15$ pF unless otherwise noted. Rise/Fall @ 0.4 – 2.4V, Duty @ 1.5V

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CLKFR}	Input Clock Frequency Range	Pk-pK = 3.3 Volts	50		200	MHz
t_{RISE}	Clock Rise Time (Pin 4)	SSCLK, CL = 15 pF, 200 MHz	0.8	0.9	1.0	ns
t_{FALL}	Clock Fall Time (Pin 4)	SSCLK, CL = 15 pF, 200 MHz	0.8	0.9	1.0	ns
t_{RISE}	Clock Rise Time (Pin 4)	SSCLK, CL = 33 pF, 200 MHz	1.1	1.45	1.8	ns
t_{FALL}	Clock Fall Time (Pin 4)	SSCLK, CL = 33 pF, 200 MHz	1.1	1.5	1.9	ns
D_{TYin}	Input Clock Duty Cycle	XIN/CLK (Pin 1)	30	50	70	%
D_{TYout}	Output Clock Duty Cycle	SSCLK1 (Pin 4)	45	50	55	%
FM1	Frequency Modulation	Fin = 70 MHz	29.5	30.0	30.5	kHz
FM2	Frequency Modulation	Fin = 200 MHz	85.0	85.4	86	kHz
C_{CJ1}	Cycle-to-Cycle Jitter	Fin = 50 MHz, Mod ON		150	175	ps
C_{CJ2}	Cycle-to-Cycle Jitter	Fin = 120 MHz, Mod ON		175	200	ps
C_{CJ3}	Cycle-to-Cycle Jitter	Fin = 200 MHz, Mod ON		250	300	ps

Ordering Information

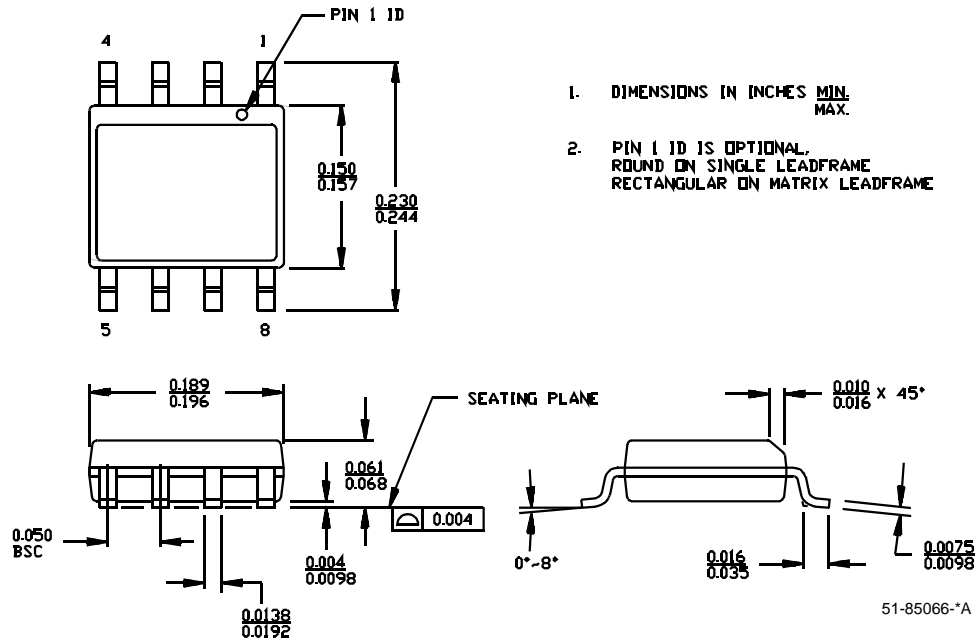
Part Number	Package Type	Product Flow
CY25562SC	8-pin SOIC	Commercial, 0° to 70°C
CY25562SCT	8-pin SOIC–Tape and Reel	Commercial, 0° to 70°C

Note:

1. Operation at any Absolute Maximum Rating is not implied.

Package Drawing and Dimensions

8-lead (150-mil) SOIC S8



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Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	115526	07/08/02	OXC	New Data Sheet