Spread Aware™, Two Output Zero Delay Buffer

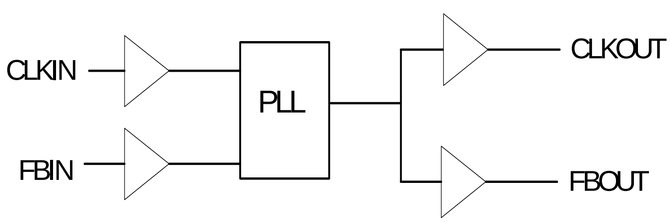
Features

- **Spread Aware™ - Designed to Work with SSFT Reference Signals**
- **Well Suited to Both 33 and 66 MHz Designs**
- **3.3V Power Supply**
- **On Chip 25Ω Damping Resistors**
- **Available in 8-pin SOIC Package**

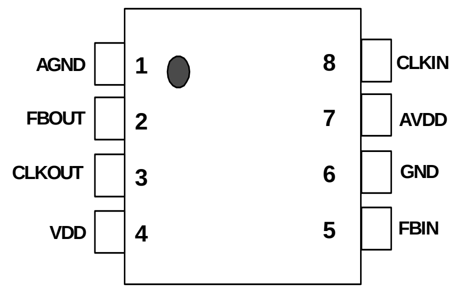
Key Specifications

Operating Voltage:..3.3V ±10%
Operating Range: ....25 MHz < f_{out} < 70 MHz
Cycle-to-cycle Jitter: ....<150 ps
Phase Error Jitter ....<150 ps

Block Diagram

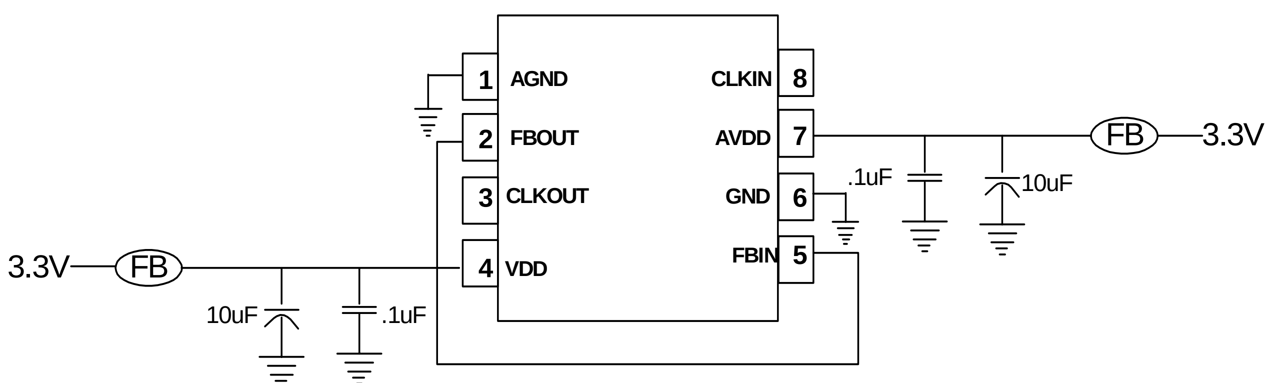


Pin Configuration



8 pin SOIC

Schematic



.

Pin Description

Pin	Name	I/O	Description
8	CLKIN	I	***Reference Input:*** Output signals will be synchronized to this signal.
5	FBIN	I	***Feedback Input:*** This input must be fed by one of the outputs (typically FBOUT) to ensure proper functionality. If the trace between FBIN and FBOUT is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the CLKIN signal input.
3	CLKOUT	O	***Integrated Series Resistor Outputs:*** The frequency and phase of the signals provided by this pin will be equal to the reference signal if properly laid out. This output has a 25Ω series damping resistor integrated.
2	FBOUT	O	***Feedback Output:*** This output has a 25Ω series resistor integrated on chip. Typically it is connected directly to the FBIN input with a trace equal length to the traces between output CLKOUT and the destination points of these output signal.
7	AVDD	P	***Analog Power Connection:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
1	AGND	G	***Analog Ground Connection:*** Connect to common system ground plane.
4	VDD	P	***Power Connections:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
6	GND	G	***Ground Connections:*** Connect to common system ground plane.

Overview

The integrated PLL of the CY2502 provides two low-jitter, low-skew clock outputs. One of these outputs, FBOUT, is used as feedback to the PLL, thus eliminating the propagation delay through the device. The PLL aligns the output edges to the input reference edge and produces a near-zero delay.

In applications requiring a higher number of outputs with zero propagation delay, using two or more devices may be impractical in as much as the device-to-device skew will reduce performance and add to the overall timing margin required. Instead the user can combine the CY2502 with the CY2318NZ fanout buffer to achieve 17 outputs at near zero delay (see *Figure 1*).

.

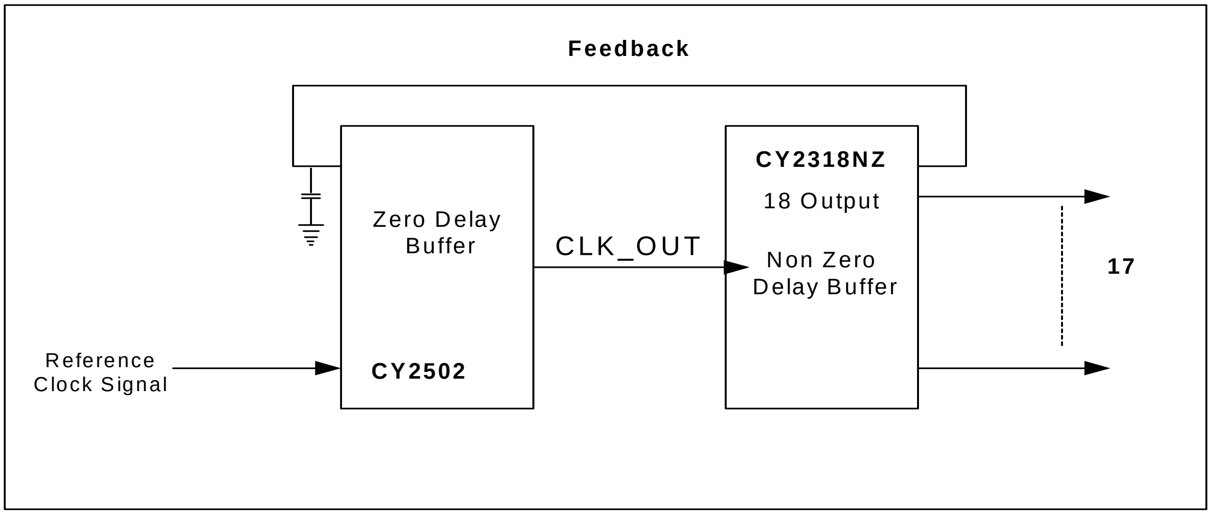


Figure 1. This Combination Provides Zero Delay Buffer Between the Reference Clocks Signal and 17 Outputs

Spread Aware

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew, which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum Timing Technology, please see the Cypress application note titled: "EMI Suppression Techniques with Spread Spectrum Frequency Timing Generators (SSFTG) ICs."

How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation, since the PLL on the ZDB will cause the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Absolute Maximum Ratings[1]

Parameter	Description	Rating	Unit
V_{DD} V_{IN}	Voltage on Any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to 70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: T_A = 0°C to 70 °C, V_{DD} = 3.3±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DDQ}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or GND; $I_0 = 0$			TBD	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 12mA			0.8	V
V_{OH}	Output High Voltage	I_{OH} = -12mA	2.1			V
I_{IL}	Input Low Current	V_{IN} = 0V			50	µA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$			50	µA

AC Electrical Characteristics: T_A = 0°C to 70 °C, V_{DD} = 3.3±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{OUT}	Output Frequency	30-pF load	25		70	MHz
t_R	Output Rise Time	0.8V to 2.0V, 30-pF load			2.1	ns
t_F	Output Fall Time	2.0V to 0.8V, 30-pF load			2.5	ns
t_{jCLKR}	Input Clock Rise[2]				4.5	ns
t_{jCLKF}	Input Clock Fall Time[2]				4.5	ns
t_{PEJ}	CLKIN to FBIN Skew Variation[3,4]	Measured at $V_{DD}/2$	–150	0	150	ps
t_{SK}	Output to Output Skew	Output loaded equally		0	450	ps
t_D	Duty Cycle	30-pF load	43	50	58	%
t_{LOCK}	PLL Lock Time	Power Supply Stable			1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle				150	ps

Notes:
1. Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. Longer input rise and fall time will degrade skew and jitter performance.
3. SKew is measured at $V_{DD}/2$ on rising edges.
4. Duty Cycle is measured at $V_{DD}/2$.

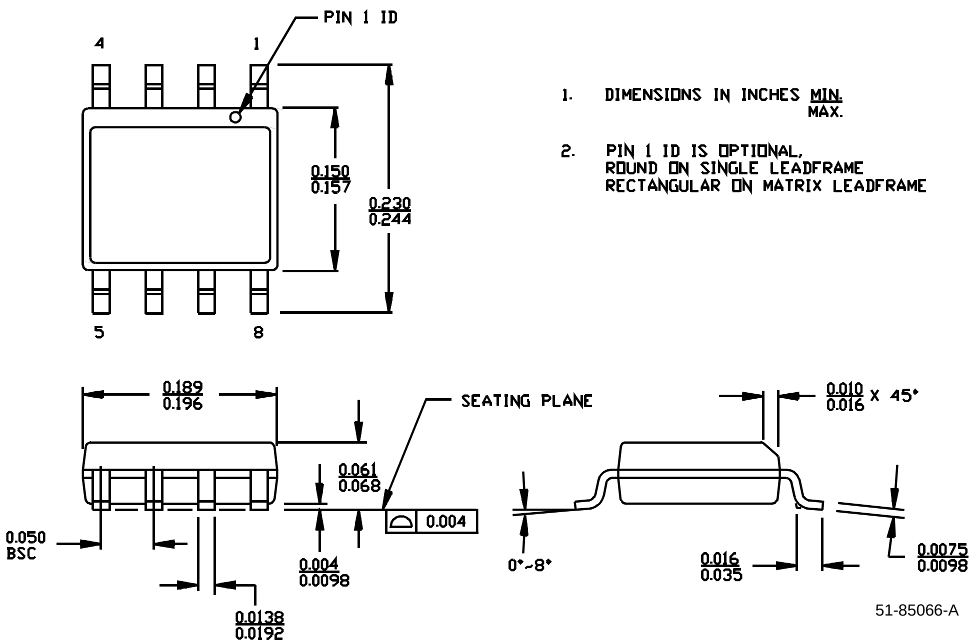
Ordering Information

Part Number	Package Name	Package Type	Product Flow
CY2502SC	S8	8 Pin SOIC (150 mil)	Commercial, 0° to 70°C
CY2502SCT	S8	8 Pin SOIC(150 mil) - Tape and Reel	Commercial, 0° to 70°C

Spread Aware is a trademark of Cypress Semiconductor Corporation. All products and company names mentioned in this document may be the trademarks of their respective holders.

Package Drawing and Dimensions

8-Lead (150-Mil) SOIC S8



Document Title: CY2502 Spread Aware™, Two Output Zero Delay Buffer Document Number: 38-07277				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110867	03/01/02	CTK	New Data Sheet