



CYPRESS

PRELIMINARY

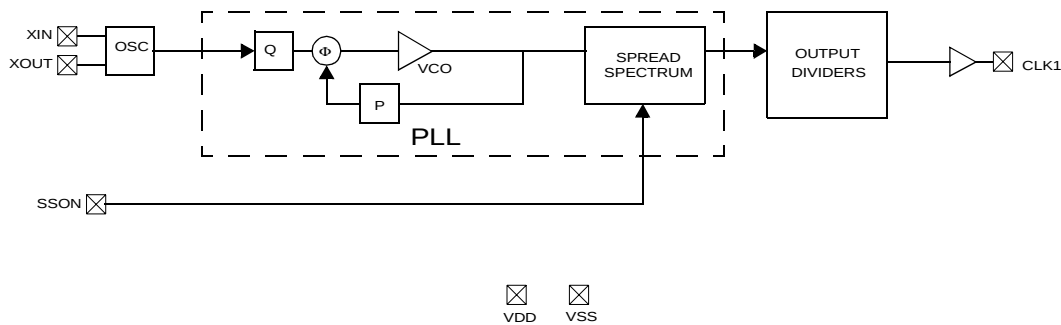
CY25001

16-MHz Spread Spectrum Clock Generator

Features	Benefits
• Integrated phase-locked loop (PLL)	High-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• Spread Spectrum	Spread Spectrum outputs for EMI reduction
• 3.3V operation	Enables application compatibility

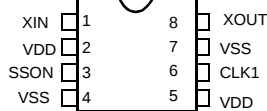
Part Number	Output	Input Frequency	Output Frequency
CY25001	1	16.00 MHz	16.00 MHz

Logic Block Diagram



Pin Configurations

CY25001
8-pin SOIC



Part #	Center Spread Percentage
CY25001SC-1	± 0.225%
CY25001SC-2	± 0.15%
CY25001SC-3	± 0.19%

Summary

Pin Name	Pin Number	Pin Description
XIN	1	Reference Crystal Input
VDD	2	Voltage Supply
SSON	3	Spread Spectrum Control for CLK1, 0 = SS off, 1 = SS on. Internal pull-up resistor.
VSS	4	Ground
VDD	5	Voltage Supply
CLK1	6	16-MHz Clock Output with Spread Spectrum
VSS	7	Ground
XOUT ^[1]	8	Reference Crystal Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Reference Frequency		16		MHz

DC Electrical Characteristics

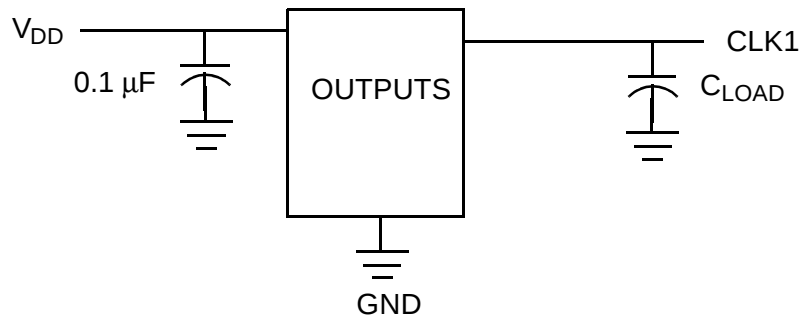
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} = 3.3 V	12	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3 V	12	24		mA
I _{IH}	Input High Current	V _{IH} = V _{DD}		5		μA
I _{IL}	Input Low Current	V _{IL} = 0V			50	μA
V _{IH}	Input High Voltage	CMOS levels, 70% of V _{DD}	0.7			V _{DD}
V _{IL}	Input Low Voltage	CMOS levels, 30% of V _{DD}			0.3	V _{DD}
C _{IN}	Input Capacitance				7	pF
I _{DD}	Supply Current	Sum of Core and Output Current			35	mA
R _{UP}	Pull-up resistor on input pin		80	100	150	kΩ

Note:

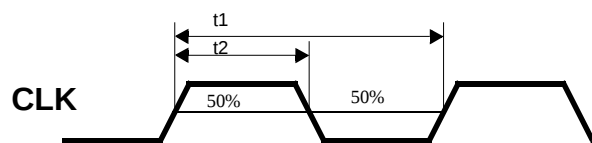
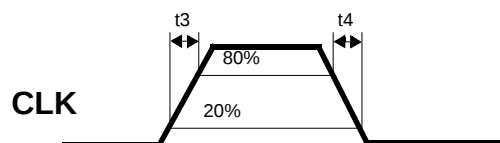
1. Float X_{OUT} if X_{IN} is externally driven.
2. Rated for 10 years.

AC Electrical Characteristics ($V_{DD} = 3.3V$)

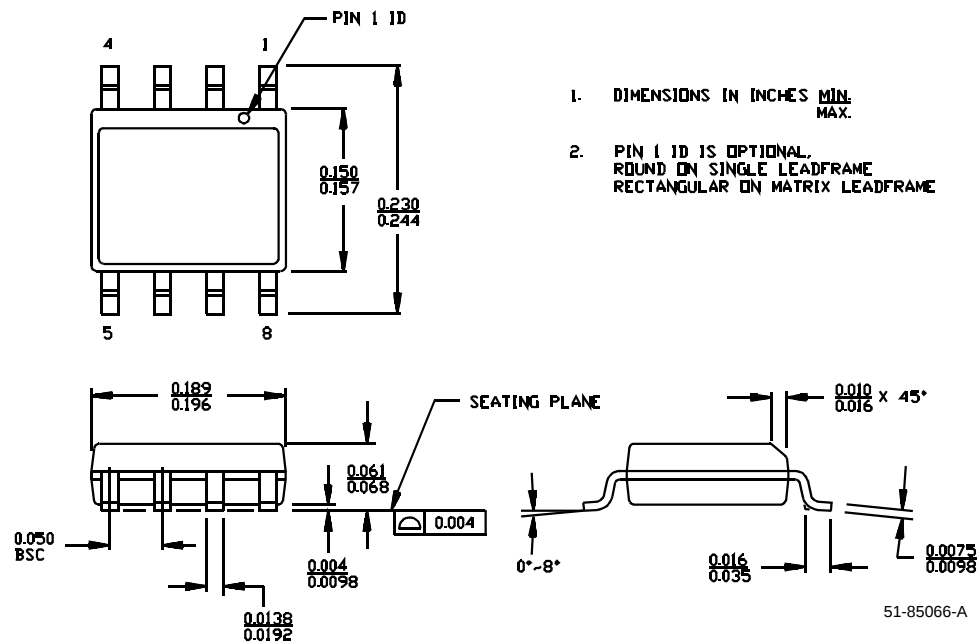
Parameter ^[3]	Description	Conditions	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 1, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20%–80% of V_{DD}	0.8	1.4	2	V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80%–20% of V_{DD}	0.8	1.4	2	V/ns
t_9	Clock Jitter	Peak to Peak Period Jitter with SSON = 0		50	100	ps
t_{10}	PLL Lock Time				3	ms

Test Circuit

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY25001SC-1	S8	8-Pin SOIC	Commercial	3.3V
CY25001SC-2	S8	8-Pin SOIC	Commercial	3.3V
CY25001SC-3	S8	8-Pin SOIC	Commercial	3.3V


Figure 1. Duty Cycle Definition; DC = t_2/t_1

Figure 2. Rise and Fall Time Definitions
Note:

3. Not 100% tested.

Package Diagram
8-lead (150-Mil) SOIC S8


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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113264	04/23/02	CKN	New Data Sheet