CY24260

Clock Generator for PDA/MP3/LCD

Features

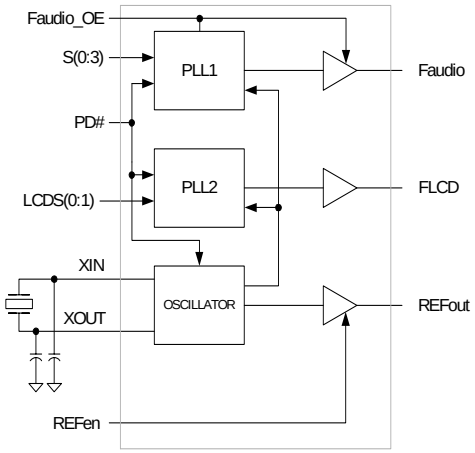
- **Supports PDA and Web-Pad clocking requirements**
- **Audio Clock for hardware codec or for AC 97 codec**
- **LCD controller programmable clock**
- **Advanced power management with synchronous clock throttling**
- **Power-down I_{PD} < 200µA**
- **Independent phase-locked loop (PLL)-disable capability**
- **Space-saving 20-lead TSSOP package**

Table 1. Frequency Table

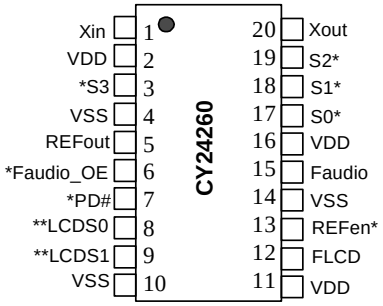
S(3:0)	Faudio (MHz)
0000	Clock Off, PLL Off
0001	24.576
0010	20
0011	N/A
0100	9.216
0101	16.25
0110	22.5792
0111	29.49
1000	2.048
1001	2.8224
1010	4.096
1011	5.6448
1100	6.144
1101	8.192
1110	11.2896
1111	12.288

LCDS1	LCDS0	FLCD (MHz)
0	0	Clock Off, PLL Off
0	1	48
1	0	24
1	1	40

Block Diagram



Pin Configuration[1]



20 pin TSSOP

Note:
1. * = Pull-up; ** = pull-down.

Pin Description

Pin	Name	PWR	I/O	Description
2,11,16	VDD			Connect to 3.3V or 5V
4,10,14	VSS			Power ground
17,18,19,3	S(0:3)		I PU	Faudio frequency select lines
8,9	LCDS(0:1)		I PD	FLCD Frequency select lines. Use a 10KW pull-up.
7	PD#		I PU	**Power-down Control**. 0 = device check down, 1= running. All outputs are turned off immediately upon PD# assertion.
5	REFout		O	Buffered output of X_{IN}
13	REFen		I PU	**REF Output Control**. 0 = Disable REFout, 1 = Enable REFout.
15	Faudio		O	Buffered output of PLL1
6	Faudio_OE		I PU	**Faudio Output Control**. 1= Faudio is running, 0 = Faudio is stopped. Faudio is stopped synchronously such that there are no glitches or short pulses.
12	FLCD		O	Buffered output of PLL2
20	Xout		O	**Oscillator Buffer Output**. Connect to crystal. Do not connect when an external clock is applied at X_{IN}. No internal capacitor.
1	Xin		I	**Oscillator Buffer Input**. Connect to a crystal or to an external clock. No internal capacitor.

Maximum Ratings

Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to + 150°C

Operating Temperature: .....0°C to +70°C

Maximum Power Supply: 3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters V_{DD} = 3.3V + 5%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{IN} = V_{DDQ}	–10		10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –8 mA	2.4			V
I_{DD}	Operating Supply Current	15 pF Load, FLCD PLL Off		7.7	10	mA
I_{DD}	Operating Supply Current	15 pF Load, FLCD PLL On		15	20	mA
I_{DDPD}	Power-down Supply Current	15 pF Load		50	100	µA
C_{IN}	Input Pin Capacitance			4		pF

AC Parameters V_{DD} = 3.3V + 5%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
X_{IN}	Input Crystal or Clock Frequency			3.6864		MHz
REF_{OUT}	REFout Frequency	1.5V		3.6864		MHz
T_R	Output Rise Time: Faudio, FLCD	0.2 V_{DD} to 0.8 V_{DD}	1.5	2	3	ns
T_F	Output Fall Time: Faudio, FLCD	0.8 V_{DD} to 0.2 V_{DD}	1.5	2	3	ns
T_{DC}	Output Duty Cycle	1.5V	45	50	55	%
T_{CCJ}	Cycle-to-Cycle Jitter			±100	±250	ps
T_{STABLE}	Stabilization Time				3	ms

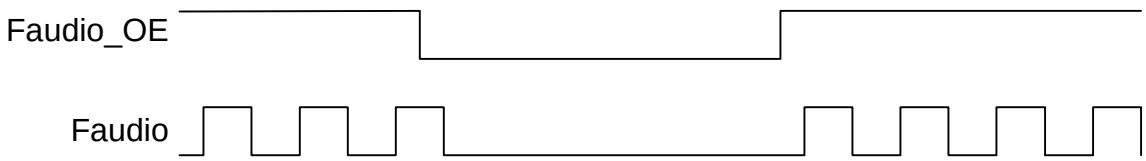


Figure 1. Faudio Enable/Disable Timing

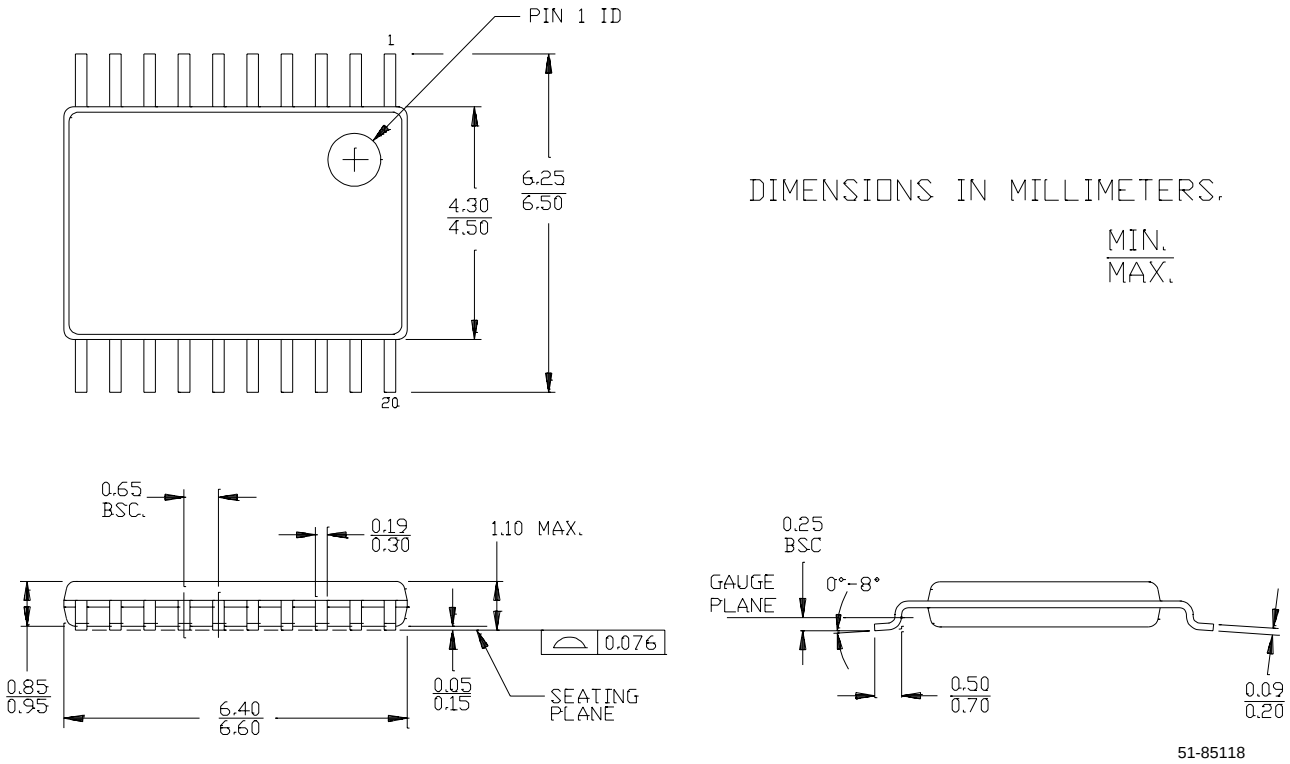
Clock	Max Load	Units
Faudio, REFout, FLCD	15	pF

Ordering Information

Part Number	Package Type	Product Flow
CY24260ZC	20-pin TSSOP	Commercial, 0°–70° C
CY24260ZCT	20-pin TSSOP – Tape and Reel	Commercial, 0°–70° C

Package Drawing and Dimensions

20-lead Thin Shrunk Small Outline Package (4.40-mm Body) Z20



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**	112832	03/04/02	DMG	New Data Sheet