CY24242

Laser Printer System Frequency Synthesizer

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Reduces measured EMI by as much as 10dB**
- **Four skew-controlled copies of CPU output**
- **Four skew-controlled copies of SDRAM output**
- **One copy of 14.31818 MHz Reference output**
- **One copy of 48 MHz USB clock (not spread)**
- **Selectable SSFTG modulation width**
- **Available in 28-pin SSOP (209 mil)**

Key Specifications

Supply Voltage:
VDDCORE: ..... 3.3V±10%
VDDC:.....3.3V±10% or 2.5V±5%
VDDS:.....3.3V±10% or 2.5V±5%
VDDU:.....3.3V±10% or 2.5V±5%
CPU Clock Cycle to Cycle Jitter: ..... 250 ps
USBCLK Long term Jitter:..... ± 500 ps
CPU0:3 Clock Skew: ..... 250 ps
CPU, SDRAM Output on Resistance:.....15Ω
Logic inputs have 250K ohm pull-up resistors

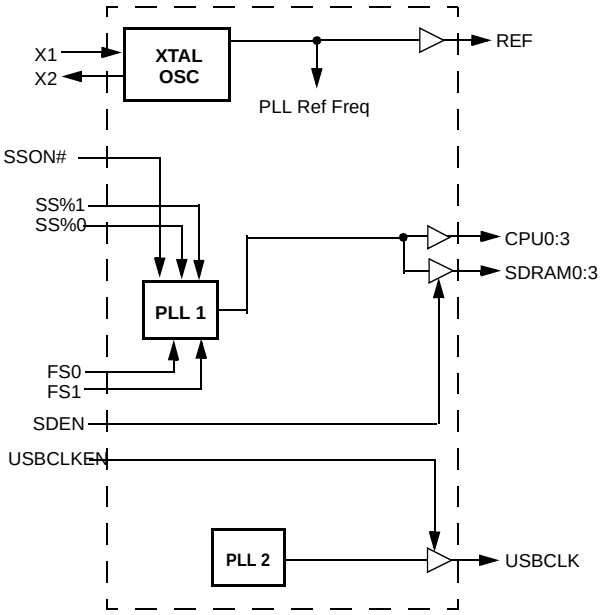
Table 1. Pin Selectable Frequency[1]

FS1	FS0	CPU(0:3), SDRAM(0:3)	USBCLK
0	0	133.3 MHz	48 MHz
0	1	100MHz	48 MHz
1	0	66.6MHz	48 MHz
1	1	50MHz	48 MHz

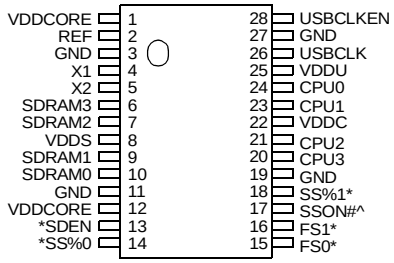
Table 2. Spread Characteristics

SSON#	SS%1	SS%0	CPU(0:3), SDRAM(0:3)
0	0	0	–0.5%
0	0	1	–1.0%
0	1	0	–2.5%
0	1	1	–3.75%
1	0	0	0 (off)\
1	0	1	0 (off)
1	1	0	0 (off)
1	1	1	0 (off)

Block Diagram



Pin Configuration[2, 3]



Notes:
1. All clock output loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. Signals marked with [*] has internal pull-up resistors
3. Signal marked with[^] has internal pull-down resistors.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	24, 23, 21, 20	O	***CPU Clock Outputs:*** These four outputs run at a frequency set by FS0:1. The width of the Spread Spectrum Modulation is enabled by pin SSON#, and selected by pins SS%0:1.
SDRAM0:3	10, 9, 7, 6	O	***SDRAM Outputs:*** These four SDRAM clock outputs run synchronously to the CPU clock. Modulation and frequency follow the CPU outputs.
FS0:1	15, 16	I	***Frequency Selection Inputs:*** Selects CPU clock frequency as shown in *Table 1*.
SS%0:1	14, 18	I	***Modulation Width Selection Inputs:*** These inputs select the width of the Spread Spectrum feature when it is enabled by SSON#.
USBCLK	26	O	***USB output:*** Timing signal running at 48.0080 MHz when a 14.31818 MHz frequency is provided as the reference. (167 ppm accuracy to 48 MHz, the output is equal to the reference times 57/17.)
SSON#	17	I	***CPU Spread Spectrum Enable Input:*** When this pin is pulled LOW, outputs CPU0:3 and SDRAM0:3 will have the Spread Spectrum Feature enabled.
USBCLKEN	28	I	***USB Disable Input:*** When this pin is pulled LOW, output USBCLK will be disabled to a LOW state.
REF	2	O	***Reference output:*** This output will be equal in frequency to the reference signal provided at X1/X2.
SDEN	13	I	***SDRAM Bank Disable Input:*** When this pin is pulled LOW, outputs SDRAM0:3 will be disabled to a low state.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** Connect to either a 14.318-MHz crystal or other reference signal.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDCORE	1, 12	P	***Power Connection:*** Core Power supply. Connect to 3.3V supply.
VDDU	25	P	***Power Connection:*** Power supply for the USB output. Connect to 3.3V or 2.5V supply.
VDDC	22	P	***Power Connection:*** Power supply for the CPU outputs. Connect to 3.3V or 2.5V supply.
VDDS	8	P	***Power Connection:*** Power supply for the SDRAM outputs. Connect to 3.3V or 2.5V supply.
GND	3,11, 19, 27	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As depicted in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ± 0.5% of the center frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the SMBus data stream.

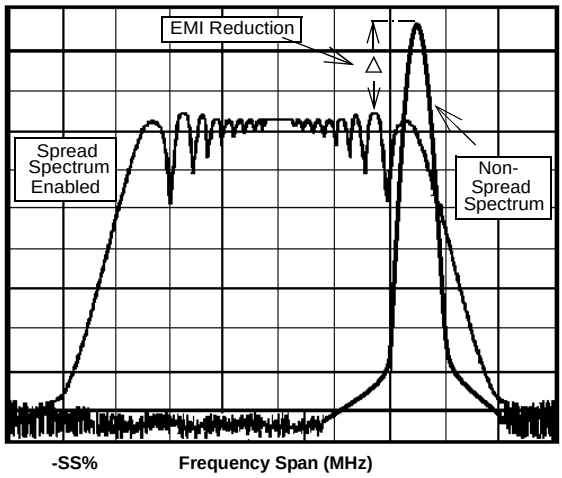


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

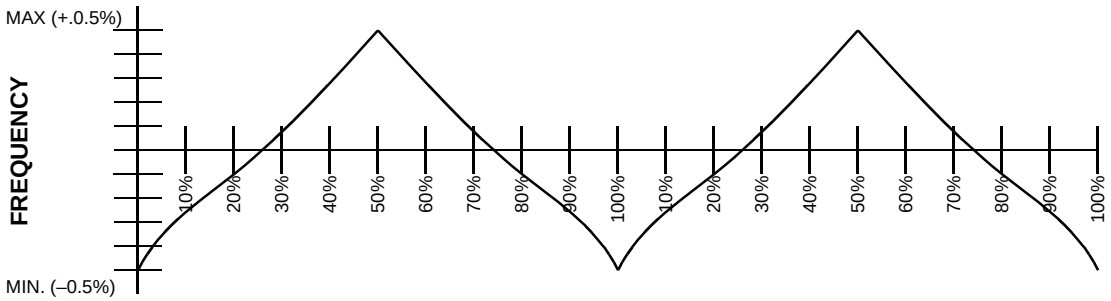


Figure 2. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–55 to +125	°C
T_B	Ambient Temperature under Bias	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics:

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V ± 10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Supply Current						
I_{DDQ3}	Supply Current (3.3V)	CPUCLK =100 MHz Outputs Loaded[4]			400	mA
I_{DDQ2}	Supply Current (2.5V)	CPUCLK =100 MHz Outputs Loaded[4]			400	mA
Logic Inputs						
V_{IL}	Input Low Voltage		GND-3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD} +.3	V
I_{IL}	Input Low Current[5]				–25	µA
I_{IH}	Input High Current[5]				10	µA
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[1]			1.5		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[6]			14		pF
$C_{IN,X1}$	X1 Input Capacitance[7]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:

4. CY24242 logic inputs have internal pull-up resistors.
5. X1 input threshold voltage (typical) is $V_{DDQ}/2$.
6. The CY24242 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
7. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = V_{DDQ3} = 3.3V±10%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF, V_{DDC} = 3.3V)

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.4V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	.4		3.2	.4		3.2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	.4		3.2	.4		3.2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

SDRAM Clock Outputs, SDRAM0:3 (Lump Capacitance Test Load = 30 pF, V_{DDC} = 3.3V)

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.4V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	.4		3.2	.4		3.2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	.4		3.2	.4		3.2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V		100	300		100	350	ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.			350			350	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

REF Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66/100MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency equal to the reference provided at pins X1, X2		14.318		MHz
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

USBCLK Clock Output (Lump Capacitance Test Load = 20 pF, V_{DDC} =3.3V)

Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min.	Typ.	Max.	
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JL}	Jitter, Long term	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			400	
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–55 to +125	°C
T_B	Ambient Temperature under Bias	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = V_{DDQ3} = 2.5V ± 5%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF, V_{DDC} = 2.5V)

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	.4		3.2	.4		3.2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	.4		3.2	.4		3.2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			250			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

SDRAM Clock Outputs, SDRAM0:3 (Lump Capacitance Test Load = 30 pF, V_{DDC} = 2.5V)

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	.4		3.2	.4		3.2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	.4		3.2	.4		3.2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V		250	300		250	350	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

REF Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency equal to the reference provided at pins X1, X2		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

USBCLK Clock Output (Lump Capacitance Test Load = 20 pF, V_{DDC} =2.5V)

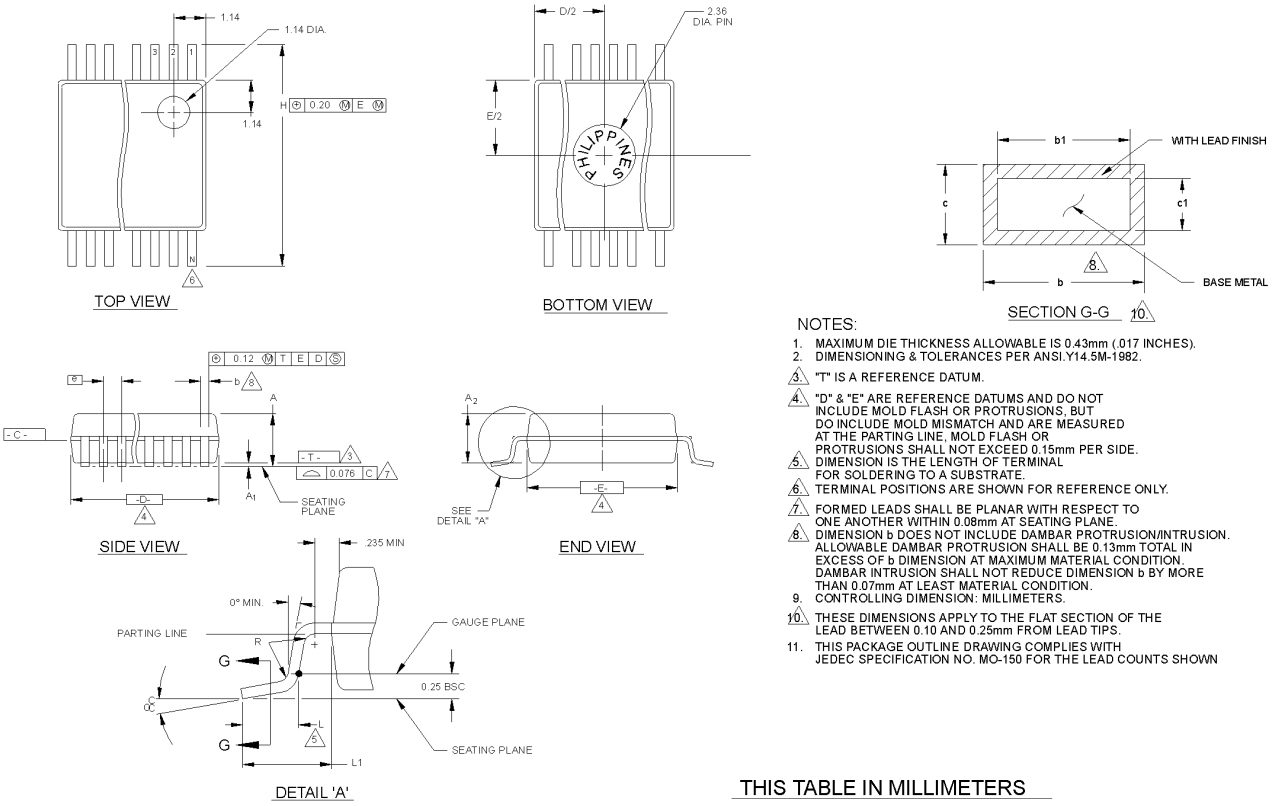
Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min.	Typ.	Max.	
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
t_{JL}	Jitter, Long term	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			500	
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			400	
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

Ordering Information

Ordering Code	Package Name	Package Type	Temperature Grade
CY24242	PVC	28-pin SSOP (300 mils)	C (Commercial 0 - 70^0)

Package Diagrams

28-Pin Small Shrink Outline Package (SSOP,209 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLEI

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	.004	.006							

Document Title: CY24242 Laser Printer Frequency Synthesizer Document Number: 38-07268				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110533	10/08/01	SZV	Change from Spec number: 38-01133 to 38-07268