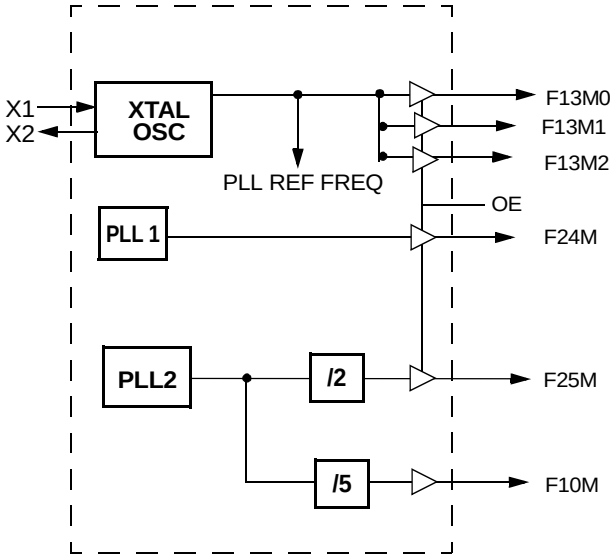
CY24240

Custom FTG for XBOX

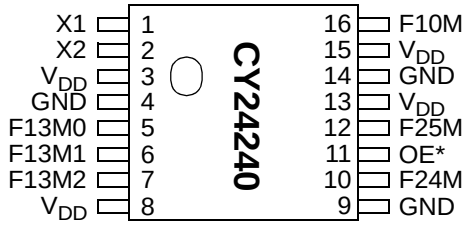
Features

- **Three copies of 13.5-MHz clock**
- **One copy of 25-MHz clock**
- **One copy of 24.576-MHz clock**
- **One copy of 10-MHz clock**
- **27-MHz reference frequency (Including crystal)**
- **Output Enable function**
- **Available in a 150-mil SOIC package**

Block Diagram



Pin Configuration[1]



Note:

1. Internal pull-up resistors present on input marked with *. Design should not solely rely on internal resistors.
2. No internal capacitors are provided at pins X1 and X2

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
X1	1	I/O	***Crystal connection:*** This pin has dual functions. It can be used as an external 27-MHz crystal connection or as an external reference frequency input.
X2	2	I/O	***Crystal connection:*** A connection for an external 27-MHz crystal. If using an external reference, this pin must be left unconnected.
F25M	12	O	***25 MHz Clock Output:*** When the reference frequency is 27 MHz, this pin provides a fixed 25-MHz clock output.
F24M	10	O	***24 MHz Clock Output:*** When the reference frequency is 27 MHz, this pin provides a fixed 24.576-MHz clock output.
F13M0:2	5, 6, 7	O	***13.5 MHz Clock Outputs:*** When the reference frequency is 27 MHz, these pins provide fixed 13.5-MHz clock outputs.
F10M	16	O	***10 MHz Clock Output:*** When the reference frequency is 27 MHz, this pin provides a fixed 10-MHz clock output. This output is not affected by the OE logic input.
OE	11	I	***Output Enable Input:*** Hold HIGH for normal operation. When held to ground, the outputs (excluding 10-MHz output) are held LOW. An internal pull up is present on this input.
VDD	3, 8, 13, 15	P	***Power Connection:*** Power supply. Connect to 3.3V.
GND	4, 9, 14	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Overview

The CY24240 is a highly integrated frequency timing generator, supplying all the required clock sources for the Microsoft XBox design.

DC Electrical Characteristics

Absolute Maximum DC Power Supply

Parameter	Description	Min.	Max.	Unit
T_O	Operating Temperature		0–70	°C

DC Operating Requirements

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.3V±5%	3.13	3.30	3.47	V
I_{DD}	Supply Current	$0<V_{in}<V_{DD3}$			TBD	mA
V_{IL}	Input Low Voltage	I_{oh}=(–1 mA)			0.8	V
V_{OH}	Input High Voltage	I_{oh}=(–1 mA)	2.0			V
V_{OH}	Output High Voltage	I_{oh}=(–1 mA)	3.0			V
V_{OL}	Output Low Voltage	I_{ol}=(1 mA)			0.3	V

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, f_{XTL} = 27 MHz
AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[3]

AC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
F_{REF}	X1 clock Synthesizer Reference Frequency		27.000		MHz
F_{TOL}	Reference Frequency Tolerance			25	ppm
FOUT1A/B/C Reference Clock Output specifications					
F_{OUTR}	Frequency		13.5		MHz
DC_R	Duty Cycle[3]	45	50	55	%
t_{RH}	Clock High Time[4]	33		41	ns
t_{RL}	Clock Low Time[5]	33		41	ns
t_{RJ}	Clock to Clock Jitter[6]			200	pF
C_{LR}	Load Capacitance		2	7	pF
t_{RF}/t_{RR}	Rise/Fall Time[8,9] C_L = 2 pF C_L = 4 pF	500		 3000	ps
FOUT2 Audio Clock Output Specifications					
F_{OUTA}	Frequency		24.576		MHz
DC_A	Duty Cycle[3]	45	50	55	%
t_{AH}	Clock High Time[4]	18.3		22.4	ns
t_{AL}	Clock Low Time[5]	18.3		22.4	ns
t_{AJ}	Clock to Clock Jitter[6]			300	pF
C_{LA}	Load Capacitance		10		pF
t_{AF}/t_{AR}	Rise/Fall Time (C_L = 10 pF)[8,9]	1		4	ns
FOUT3 Ethernet Clock Output Specifications					
F_{OUTE}	Frequency		25		MHz
DC_E	Duty Cycle[3]	35	50	65	%
t_{EH}	Clock High Time[4]	14		26	ns
t_{EL}	Clock Low Time[5]	14		26	ns
t_{EJ}	Clock to Clock Jitter[6]			300	pF
C_{LE}	Load Capacitance		10		pF

AC Electrical Characteristics (continued)

Parameter	Description	Min.	Typ.	Max.	Unit
t_{EF}/t_{ER}	Rise/Fall Time (C_L = 3 pF)[8,9]	1		4	ns
FOUT4 SMC Clock Output Specifications					
F_{OUTS}	Frequency		10		MHz
DC_S	Duty Cycle[3]	25	50	75	%
t_{SH}	Clock High Time[4]	25		75	ns
t_{SL}	Clock Low Time[5]	25		75	ns
C_{LS}	Load Capacitance		15		pF
t_{SF}/t_{SR}	Rise/Fall Time (C_L = 15 pF) [8,9]			15	ns
Reference Oscillator and Crystal Parameters					
F_O	Frequency[9]		27.00		MHz
C_{XTAL}	Load Capacitance[10]		6		pF
R_{ESR}	Effective Series Resistance		40	150	Ohm

Notes:

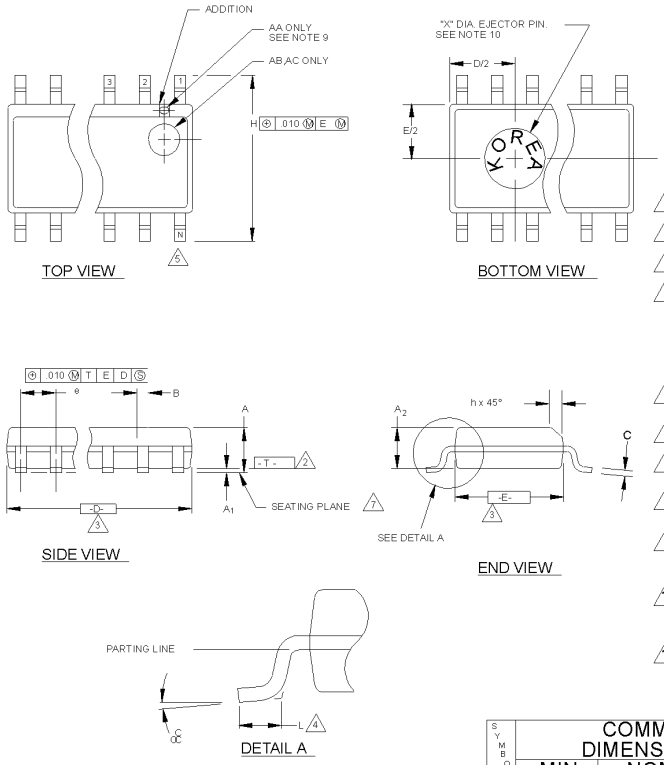
3. This specification is provided for reference only. The controlling specifications are the clock high and low times.
4. Time measured from the rising edge crossing V_{OH} to the falling edge crossing V_{OL}.
5. Time measured from the rising edge crossing V_{OL} to the falling edge crossing V_{OH}.
6. The absolute difference in period between any two consecutive clock cycles.
7. Time measured from 10% to 90% points on the rising or falling edge of the waveform.
8. Rise and fall time is measured at the clock input being driven, and may be achieved with suitable series resistance introduced between the clock output driver and the clock input.
9. For best performance and accurate frequencies from this device, it is recommenced but not mandatory that the chosen crystal meets or exceeds these specifications.
10. Larger values may cause this device to exhibit oscillator startup problems.

Ordering Information

Ordering Code	Package Name	Package Type
CY24240	PVC	16-pin SSOP (150 mils)

Package Diagram

16-Pin Shrink Small Outline Package (SOIC, 150 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

Document Title: CY24240 Custom FTG for XBOX Document Number: 38-07267				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110532	12/15/01	SZV	Change from Spec number: 38-01114 to 38-07267