



# CYPRESS

## CY24239

### Spread Spectrum Frequency Timing Generator

#### Features

- Maximized EMI Suppression using Cypress's Spread Spectrum Technology
- -1.2% and -2.4% Spread Spectrum support
- Three copies of CPU output
- Seven copies of PCI output
- One 48-MHz output for USB / One 24-MHz for SIO
- Two buffered reference outputs
- Two IOAPIC outputs
- Seventeen SDRAM outputs provide support for 4 DIMMs
- SMBus interface for programming
- Power management control inputs

#### Key Specifications

CPU Cycle-to-Cycle Jitter: ..... 250 ps  
 CPU to CPU Output Skew: ..... 350 ps  
 PCI to PCI Output Skew: ..... 500 ps  
 SDRAMIN to SDRAM0:16 Delay: ..... 3.7 ns typ.  
 V<sub>DDQ3</sub>: ..... 3.3V±5%

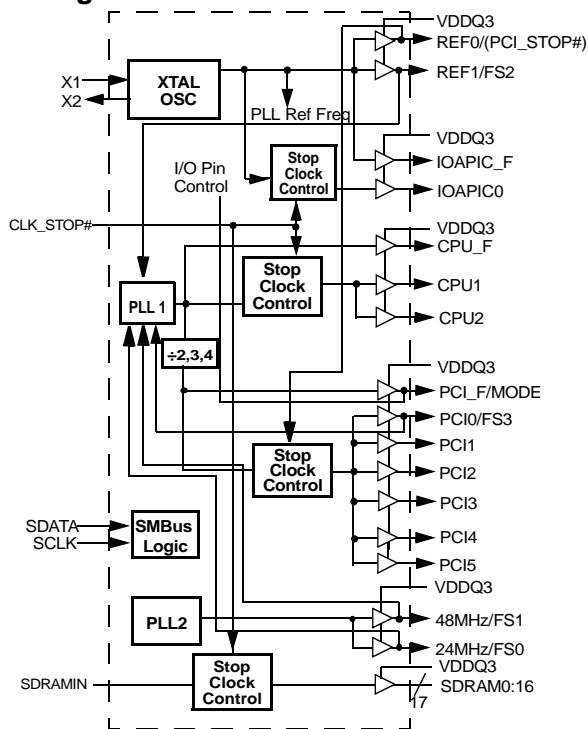
**Table 1. Mode Input Table**

Mode	Pin 3
0	PCI_STOP#
1	REF0

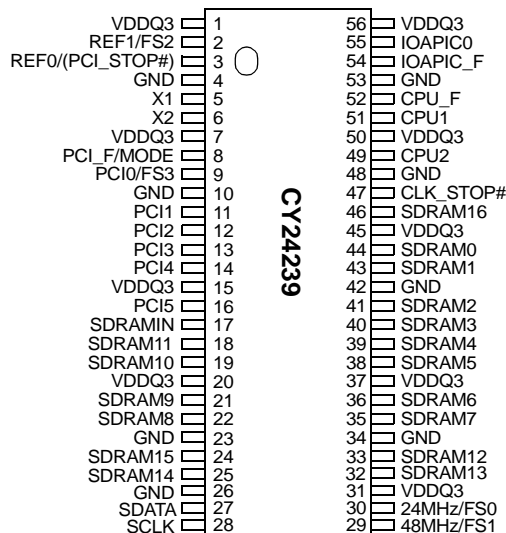
**Table 2. Pin Selectable Frequency**

Input Address				CPU_F, CPU1:2 (MHz)	PCI_F, PCI0:5 (MHz)	Spread Spec- trum
FS3	FS2	FS1	FS0			
1	1	1	1	91.66	30.5	OFF
1	1	1	0	75.0	25.0	OFF
1	1	0	1	100.0	33.3	OFF
1	1	0	0	83.3	27.76	OFF
1	0	1	1	66.6	33.3	OFF
1	0	1	0	105.0	26.3	OFF
1	0	0	1	110.0	27.5	OFF
1	0	0	0	133.3	33.3	OFF
0	1	1	1	91.66	30.5	-1.2%
0	1	1	0	75.0	25.0	-1.2%
0	1	0	1	100.0	33.3	-1.2%
0	1	0	0	83.3	27.76	-1.2%
0	0	1	1	91.66	30.5	-2.4%
0	0	1	0	75.0	25.0	-2.4%
0	0	0	1	100.0	33.3	-2.4%
0	0	0	0	83.3	27.76	-2.4%

#### Block Diagram



#### Pin Configuration<sup>[1]</sup>



#### Note:

1. Internal pull-up resistors should not be relied upon for setting I/O pins HIGH. Pin function with parentheses determined by MODE pin resistor strapping. Unlike other I/O pins, input FS3 has an internal pull-down resistor.

Intel is a registered trademark of Intel Corporation.

## Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU1:2	51, 49	O	<b>CPU Outputs 1 and 2:</b> Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . These outputs are affected by the CLK_STOP# input.
CPU_F	52	O	<b>Free-Running CPU Output:</b> Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . This output is not affected by the CLK_STOP# input.
PCI1:5	11, 12, 13, 14, 16	O	<b>PCI Outputs 1 through 5:</b> Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . These outputs are affected by the PCI_STOP# input.
PCI0/FS3	9	I/O	<b>PCI Output/Frequency Select Input:</b> As an output, frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . This output is affected by the PCI_STOP# input. When an input, latches data selecting the frequency of the CPU and PCI outputs.
PCI_F/MODE	8	I/O	<b>Free Running PCI Output:</b> Frequency is set by the FS0:3 inputs or through serial input interface, see <i>Table 2</i> and <i>Table 6</i> . This output is not affected by the PCI_STOP# input. When an input, selects function of pin 3 as described in <i>Table 1</i> .
CLK_STOP#	47	I	<b>CLK_STOP# Input:</b> When brought LOW, affected outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, affected outputs start beginning with a full clock cycle (2–3 CPU clock latency).
IOAPIC_F	54	O	<b>Free-running IOAPIC Output:</b> This output is a buffered version of the reference input which is not affected by the CPU_STOP# logic input. Its swing is set by voltage applied to VDDQ3.
IOAPIC0	55	I/O	<b>IOAPIC Output:</b> Provides 14.318-MHz fixed frequency. The output voltage swing is set by voltage applied to VDDQ3. This output is disabled when CLK_STOP# is set LOW.
48MHz/FS1	29	I/O	<b>48-MHz Output:</b> 48 MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power-up, FS1 input will be latched, setting output frequencies as described in <i>Table 2</i> .
24MHz/FS0	30	I/O	<b>24-MHz Output:</b> 24 MHz is provided in normal operation. In standard systems, this output can be used as the clock input for a Super I/O chip. Upon power up, FS0 input will be latched, setting output frequencies as described in <i>Table 2</i> .
REF1/FS2	2	I/O	<b>Reference Output:</b> 14.318 MHz is provided in normal operation. Upon power-up, FS2 input will be latched, setting output frequencies as described in <i>Table 2</i> .
REF0 (PCI_STOP#)	3	I/O	<b>Fixed 14.318-MHz Output 0 or PCI_STOP# Pin:</b> Function determined by MODE pin. The PCI_STOP# input enables the PCI 0:5 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effects take place on the next PCI_F clock cycle. As an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins (14.318 MHz).
SDRAMIN	17	I	<b>Buffered Input Pin:</b> The signal provided to this input pin is buffered to 17 outputs (SDRAM0:16).
SDRAM0:16	44, 43, 41, 40, 39, 38, 36, 35, 22, 21, 19, 18, 33, 32, 25, 24, 46	O	<b>Buffered Outputs:</b> These seventeen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3, and they are deactivated when CLK_STOP# input is set LOW.
SCLK	28	I	Clock pin for SMBus circuitry.
SDATA	27	I/O	Data pin for SMBus circuitry.
X1	5	I	<b>Crystal Connection or External Reference Frequency Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	6	I	<b>Crystal Connection:</b> An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	1, 7, 15, 20, 31, 37, 45, 50, 56	P	<b>Power Connection:</b> Power supply for core logic, PLL circuitry, SDRAM output buffers, PCI output buffers, reference output buffers and 48-MHz/24-MHz output buffers. Connect to 3.3V.
GND	4, 10, 23, 26, 34, 42, 48, 53	G	<b>Ground Connections:</b> Connect all ground pins to the common system ground plane.

## Functional Description

### I/O Pin Operation

Pins 2, 8, 9, 29, and 30 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and the pins become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

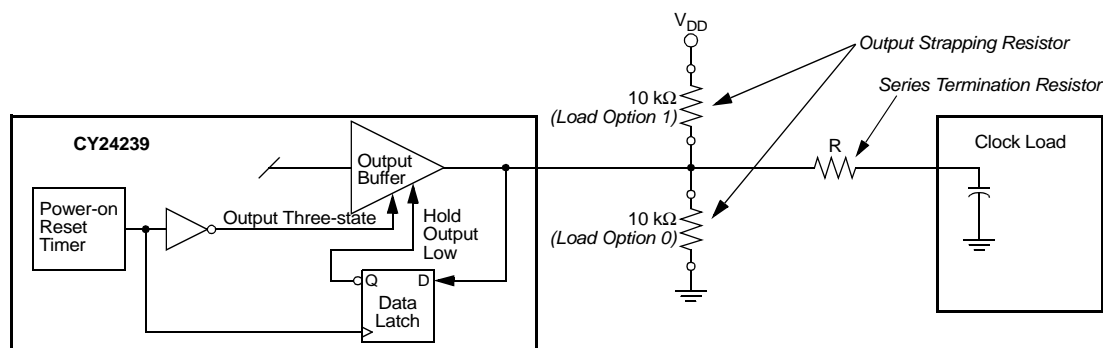
An external 10-k $\Omega$  “strapping” resistor is connected between the I/O pin and ground or  $V_{DD}$ . Connection to ground sets a latch to “0,” connection to  $V_{DD}$  sets a latch to “1.” *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connections.

Upon CY24239 power-up, the first 2 ms of operation is used for input logic selection. During this period, the five I/O pins (2, 8, 9, 29, 30) are three-stated, allowing the output strapping resistor on the I/O pins to pull the pins and their associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic “0” or “1”

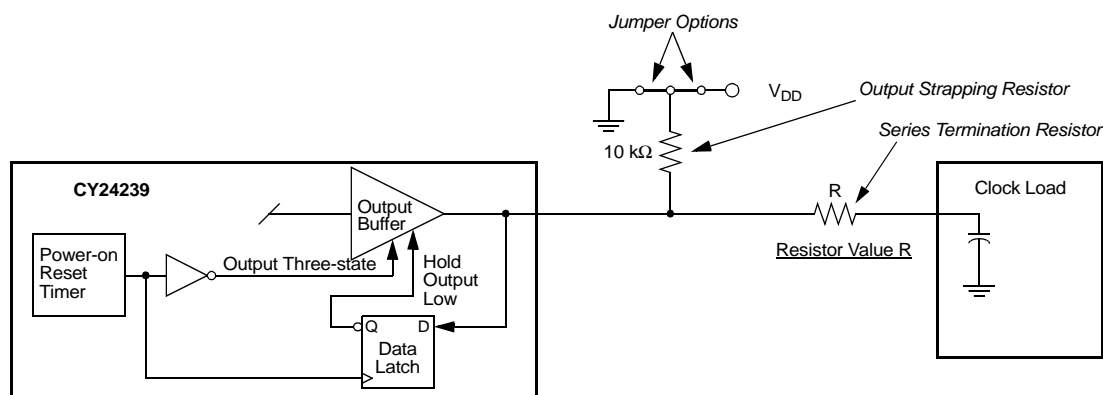
condition of the I/O pin is latched. Next the output buffer is enabled, converting the I/O pins into operating clock outputs. The 2-ms timer starts when  $V_{DD}$  reaches 2.0V. The input bits can only be reset by turning  $V_{DD}$  off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output (<40 $\Omega$ , nominal), which is minimally affected by the 10-k $\Omega$  strap to ground or  $V_{DD}$ . As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or  $V_{DD}$  should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, the specified output frequency is delivered on the pin, assuming that  $V_{DD}$  has stabilized. If  $V_{DD}$  has not yet reached full value, output frequency initially may be below target but will increase to target once  $V_{DD}$  voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.



**Figure 1. Input Logic Selection Through Resistor Load Option**



**Figure 2. Input Logic Selection Through Jumper Option**

## Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

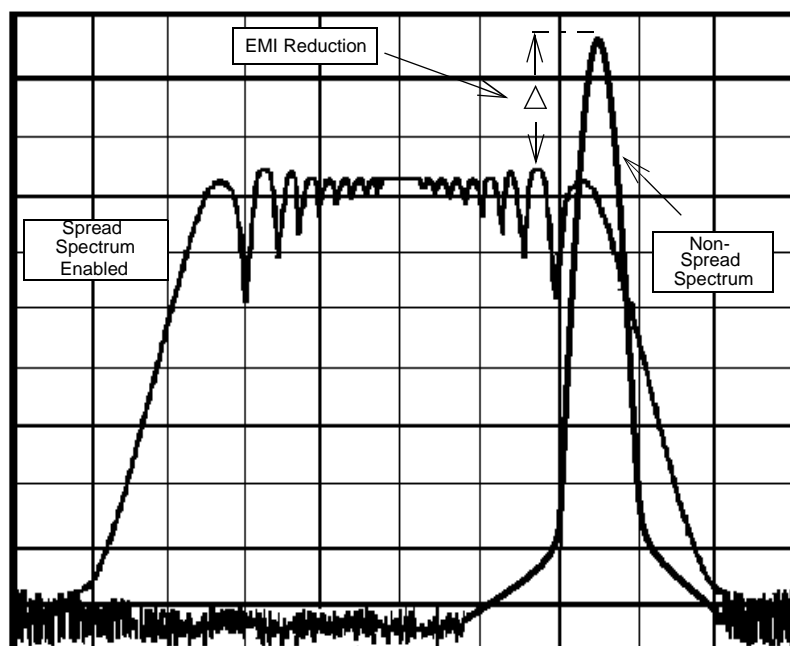
As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

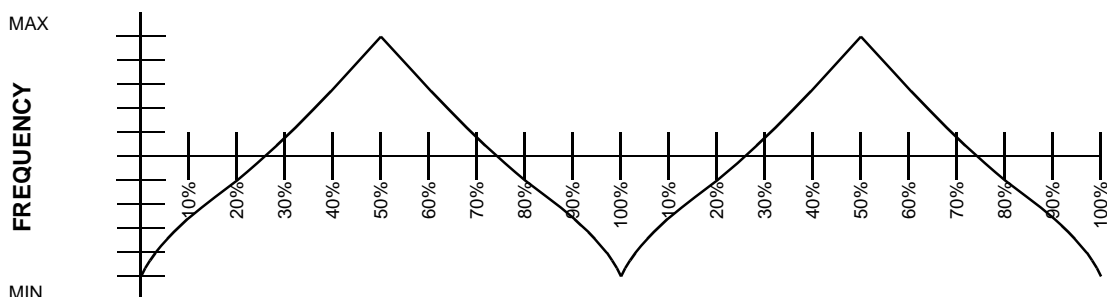
Where  $P$  is the percentage of deviation and  $F$  is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is specified in *Table 6*. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the SMBus data stream. Refer to *Table 7* for more details.



**Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation**



**Figure 4. Typical Modulation Profile**

## Serial Data Interface

The CY24239 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the CY24239 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the

chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 3* summarizes the control functions of the serial data interface.

### Operation

Data is written to the CY24239 in eleven bytes of eight bits each. Bytes are written in the order shown in *Table 4*.

**Table 3. Serial Data Interface Control Functions Summary**

Control Function	Description	Common Application
Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections alternate to the selections that are provided by the FS0:3 pins. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
Output Three-state	Puts all clock outputs into a high-impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to <i>Table 5</i> .	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

**Table 4. Byte Writing Sequence**

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the CY24239 to accept the bits in Data Bytes 0–7 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the CY24239 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the CY24239, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the CY24239, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to <i>Table 5</i>	The data bits in Data Bytes 0–7 set internal CY24239 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to <i>Table 5</i> , Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6	Don't Care	Unused by the CY24239, therefore bit values are ignored ("don't care").
11	Data Byte 7		

### Writing Data Bytes

Each bit in Data Bytes 0–7 controls a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 5* gives the bit formats for registers located in Data Bytes 0–7.

*Table 6* details additional frequency selections that are available through the serial data interface.

*Table 7* details the select functions for Byte 0, bits 1 and 0.

**Table 5. Data Bytes 0–7 Serial Configuration Map**

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL2	Refer to <i>Table 6</i>		0
5	--	--	SEL1	Refer to <i>Table 6</i>		0
4	--	--	SEL0	Refer to <i>Table 6</i>		0
3	--	--	Frequency Table Selection	Frequency Controlled by FS(3:0) <i>Table 2</i>	Frequency Controlled by SEL(3:0) <i>Table 6</i>	0
2	--	--	SEL3	Refer to <i>Table 6</i>		0
1	--	--	(Reserved)	--	--	0
0	--	Test Mode	--	Normal	Three-stated	0
Data Byte 1						
7	--	--	--	--	--	0
6	--	--	--	--	--	0
5	--	--	--	--	--	0
4	--	--	--	--	--	0
3	46	SDRAM16	Clock Output Disable	LOW	Active	1
2	49	CPU2	Clock Output Disable	LOW	Active	1
1	51	CPU1	Clock Output Disable	LOW	Active	1
0	52	CPU_F	Clock Output Disable	LOW	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	8	PCI_F	Clock Output Disable	LOW	Active	1
5	16	PCI5	Clock Output Disable	LOW	Active	1
4	14	PCI4	Clock Output Disable	LOW	Active	1
3	13	PCI3	Clock Output Disable	LOW	Active	1
2	12	PCI2	Clock Output Disable	LOW	Active	1
1	11	PCI1	Clock Output Disable	LOW	Active	1
0	9	PCI0	Clock Output Disable	LOW	Active	1
Data Byte 3						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	29	48MHz	Clock Output Disable	LOW	Active	1
4	30	24MHz	Clock Output Disable	LOW	Active	1
3	33, 32, 25, 24	SDRAM12:15	Clock Output Disable	LOW	Active	1

**Table 5. Data Bytes 0–7 Serial Configuration Map** (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
2	22, 21, 19, 18	SDRAM8:11	Clock Output Disable	LOW	Active	1
1	39, 38, 36, 35	SDRAM4:7	Clock Output Disable	LOW	Active	1
0	44, 43, 41, 40	SDRAM0:3	Clock Output Disable	LOW	Active	1
<b>Data Byte 4</b>						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
<b>Data Byte 5</b>						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	54	IOAPIC_F	Disabled	LOW	Active	1
4	55	IOAPICO	Disabled	LOW	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	2	REF1	Clock Output Disable	LOW	Active	1
0	3	REF0	Clock Output Disable	LOW	Active	1

**Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes**

Input Conditions				Output Frequency		Spread Spectrum
Data Byte 0, Bit 3 = 1				CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)	Percentage
Bit 2 SEL_3	Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0			
1	1	1	1	91.66	30.5	OFF
1	1	1	0	75.0	25.0	OFF
1	1	0	1	100.0	33.3	OFF
1	1	0	0	83.3	27.76	OFF
1	0	1	1	66.6	33.3	OFF
1	0	1	0	105.0	26.3	OFF
1	0	0	1	110.0	27.5	OFF
1	0	0	0	133.3	33.3	OFF
0	1	1	1	91.66	30.5	-1.2%
0	1	1	0	75.0	25.0	-1.2%
0	1	0	1	100.0	33.3	-1.2%
0	1	0	0	83.3	27.76	-1.2%
0	0	1	1	91.66	30.5	-2.4%
0	0	1	0	75.0	25.0	-2.4%
0	0	0	1	100.0	33.3	-2.4%
0	0	0	0	83.3	27.76	-2.4%

**Table 7. Select Function for Data Byte 0, Bits 0**

Function	Input Conditions	Output Conditions				
	Data Byte 0	CPU_F, 1:2	PCI_F, PCI0:5	REF0:1, IOAPIC0,_F	48MHZ	24MHZ
	Bit 0					
Normal Operation	0	Note 2	Note 2	14.318 MHz	48 MHz	24 MHz
Three-state	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

**Note:**

2. CPU and PCI frequency selections are listed in *Table 2* and *Table 6*.



## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C
$T_A$	Operating Temperature	0 to +70	°C
$ESD_{PROT}$	Input ESD Protection	2 (min.)	kV

## DC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{DDQ3} = 3.3\text{V} \pm 5\%$

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
<b>Supply Current</b>						
$I_{DD}$	3.3V Supply Current	CPU_F, 1:2 = 100 MHz Outputs Loaded <sup>[3]</sup>		370		mA
<b>Logic Inputs</b>						
$V_{IL}$	Input Low Voltage		GND - 0.3		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD} + 0.3$	V
$I_{IL}$	Input Low Current <sup>[4]</sup>				-25	μA
$I_{IH}$	Input High Current <sup>[4]</sup>				10	μA
$I_{IL}$	Input Low Current (SEL100/66#)				-5	μA
$I_{IH}$	Input High Current (SEL100/66#)				+5	μA
<b>Clock Outputs</b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 1\text{ mA}$			50	mV
$V_{OH}$	Output High Voltage	$I_{OH} = -1\text{ mA}$	3.1			V
$V_{OH}$	Output High Voltage	CPU_F, 1:2 IOAPIC $I_{OH} = -1\text{ mA}$	2.2			V
$I_{OL}$	Output Low Current	CPU_F, 1:2 $V_{OL} = 1.25\text{V}$	60	73	85	mA
		PCI_F, PCI0:5 $V_{OL} = 1.5\text{V}$	96	110	130	mA
		IOAPIC0, IOAPIC_F $V_{OL} = 1.25\text{V}$	72	92	110	mA
		REF0:1 $V_{OL} = 1.5\text{V}$	61	71	80	mA
		48-MHz $V_{OL} = 1.5\text{V}$	60	70	80	mA
		24-MHz $V_{OL} = 1.5\text{V}$	60	70	80	mA
		SDRAM0:16 $V_{OL} = 1.5\text{V}$	95	110	130	mA
$I_{OH}$	Output High Current	CPU_F, 1:2 $V_{OL} = 1.25\text{V}$	43	60	80	mA
		PCI_F, PCI0:5 $V_{OL} = 1.5\text{V}$	76	96	120	mA
		IOAPIC0, IOAPIC_F $V_{OL} = 1.25\text{V}$	60	90	130	mA
		REF0:1 $V_{OL} = 1.5\text{V}$	50	60	72	mA
		48-MHz $V_{OL} = 1.5\text{V}$	50	60	72	mA
		24-MHz $V_{OL} = 1.5\text{V}$	50	60	72	mA
		SDRAM0:16 $V_{OL} = 1.5\text{V}$	75	95	120	mA

### Notes:

- All clock outputs loaded with 6" 60Ω transmission lines with 22-pF capacitors.
- CY24239 logic inputs (except FS3) have internal pull-up devices (pull-ups not full CMOS level). Logic input FS3 has an internal pull-down device.

**DC Electrical Characteristics:**  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$  (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
<b>Crystal Oscillator</b>						
$V_{TH}$	X1 Input Threshold Voltage <sup>[5]</sup>	$V_{DDQ3} = 3.3\text{V}$		1.65		V
$C_{LOAD}$	Load Capacitance, Imposed on External Crystal <sup>[6]</sup>			14		pF
$C_{IN,X1}$	X1 Input Capacitance <sup>[7]</sup>	Pin X2 unconnected		28		pF
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance	Except X1 and X2			5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

**AC Electrical Characteristics**
 $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$ 

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum is disabled.

**CPU Clock Outputs, CPU\_F, 1:2 (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/ Comments	CPU = 100 MHz			Unit
			Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.25	10		10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.0V	3.0			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	2.8			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.25V			350	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		$\Omega$

**Notes:**

- X1 input threshold voltage (typical) is  $V_{DDQ3}/2$ .
- The CY24239 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 20 pF; this includes typical stray capacitance of short PCB traces to crystal.
- X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

**PCI Clock Outputs, PCI0:5 (Lump Capacitance Test Load = 30 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$t_P$	Period	Measured on rising edge at 1.5V	30			ns
$t_H$	High Time	Duration of clock cycle above 2.4V	12			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	12			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V			500	ps
$t_O$	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		$\Omega$

**IOAPIC0 and IOAPIC\_F Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$f$	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		$\Omega$

**REF0:1 Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$f$	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		$\Omega$

**SDRAM 0:16 Clock Outputs (Lump Capacitance Test Load = 22 pF)**

Parameter	Description	Test Condition/ Comments	SDRAMIN = 100 MHz			Unit
			Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.5V	10		10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.4V	3.0			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	2.0			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$t_{SK}$	Output Skew	Measured on rising and falling edge at 1.5V			250	ps
$t_{PD}$	Propagation Delay	Measured from SDRAMIN		3.7		ns
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		$\Omega$

**48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$f$	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	48.008			MHz
$f_D$	Deviation from 48 MHz	$(48.008 - 48)/48$	+167			ppm
m/n	PLL Ratio	$(14.31818 \text{ MHz} \times 57/17 = 48.008 \text{ MHz})$	57/17			
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		$\Omega$

**24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

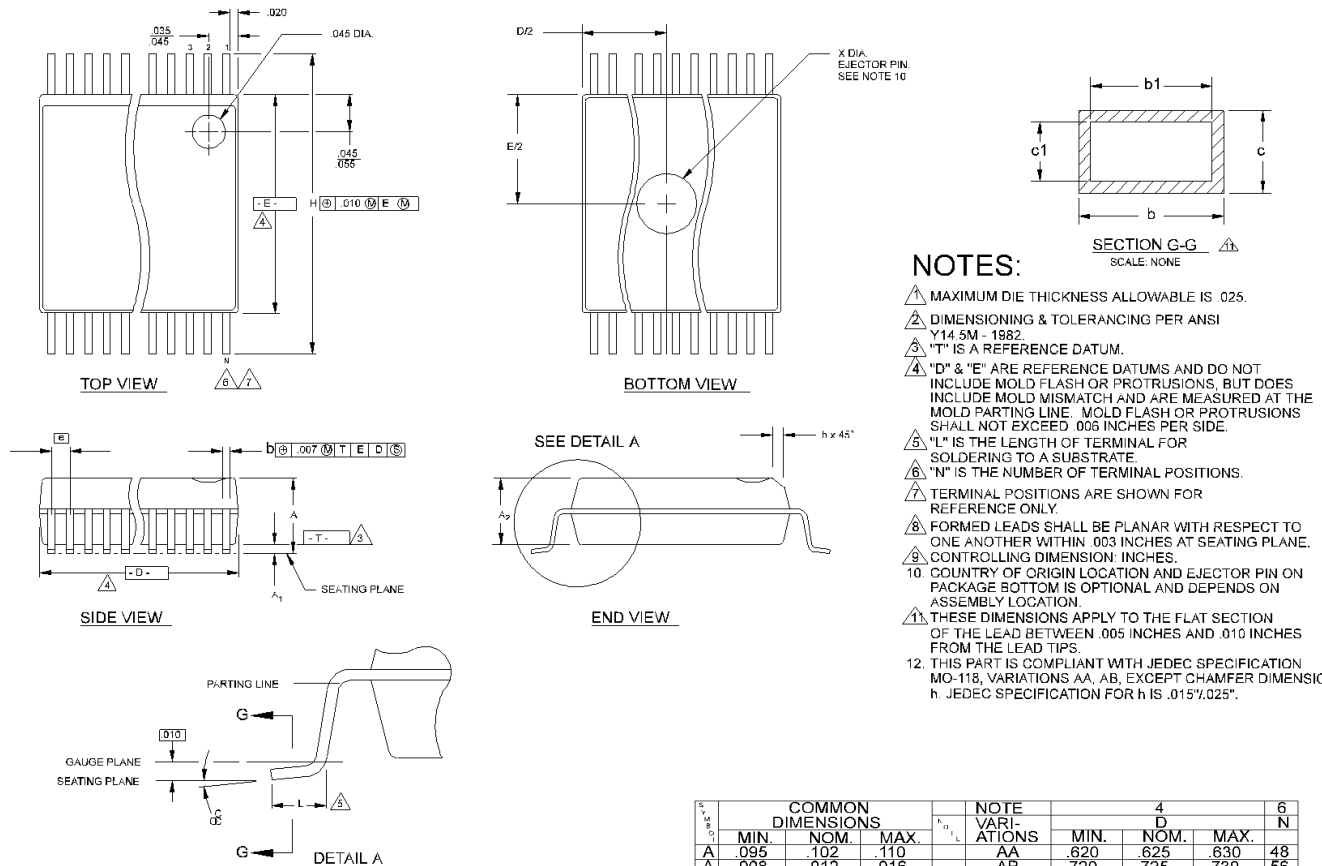
Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	24.004			MHz
f <sub>D</sub>	Deviation from 24 MHz	(24.004 – 24)/24	+167			ppm
m/n	PLL Ratio	(14.31818 MHz x 57/34 = 24.004 MHz)	57/34			
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>O</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

**Ordering Information**

Ordering Code	Package Type
CY24239PVC	56-pin SSOP (300 mils)

## Package Diagram

### 56-Pin Small Shrink Outline Package (SSOP, 300 mils)



#### Summary of nominal dimensions in inches:

**Body Width: 0.296**  
**Lead Pitch: 0.025**  
**Body Length: 0.625**  
**Body Height: 0.102**

S VARIATIONS	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AA	.620	.625	.630	48
A <sub>1</sub>	.008	.012	.016	AB	.720	.725	.730	56
A <sub>2</sub>	.008	.090	.092					
b	.008	.010	.015					
c	.005	.010	.012					
D	.005	.006	.0085					
E	.292	.296	.299					
e		.025 BSC						
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N								
X	.085	.093	.100					
α	0°	5°	8°					

THIS TABLE IN INCHES

S VARIATIONS	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A <sub>1</sub>	0.20	0.31	0.41	AB	18.29	18.42	18.54	56
A <sub>2</sub>	2.24	2.29	2.34					
b	0.203	0.254	0.343					
c	0.203	0.254	0.305					
D	0.127	0.152	0.216					
E	7.42	7.52	7.59					
e		0.635 BSC						
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N								
X	2.16	2.36	2.54					
α	0°	5°	8°					

THIS TABLE IN MILLIMETERS

Document Title: CY24239 Spread Spectrum Frequency Timing Generator  
Document Number: 38-07038

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106975	05/24/01	IKA	New Data Sheet