PRELIMINARY

CY24233

Clock Generator for DVD Players

Product Features

- **Two Reference outputs (27.00 MHz)**
- **Two 33.8688-MHz outputs**
- **Two 512fs outputs (22.5792 MHz or 24.576 MHz)**
- **27.00-MHz Clock or crystal input**
- **3.3V operation (2.5V functional)**
- **High-drive outputs**
- **0 PPM application frequency synthesis error**
- **16-pin TSSOP package**

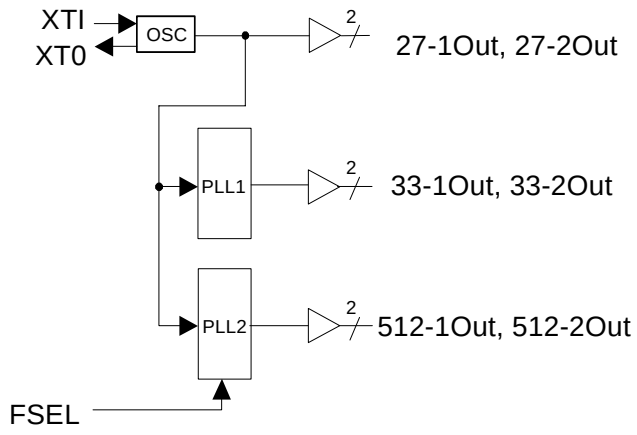
Product Description

The CY24233 is a clock generator solution that supports DVD digital disk players. It produces a complete set of clocks needed to support the entire system. All output clocks are synthesized from a single 27.00MHz fundamental cut crystal or input reference clock. The output clocks are precisely synthesized to meet the systems low PPM error requirements.

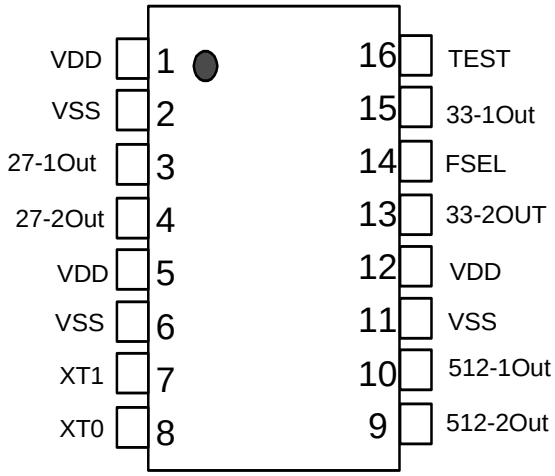
Table 1.

Test	FSEL	27-1Out 27-2Out	33-1Out 33-2Out	512-1Out 512-2Out
0	0	27.00 MHz	2.700 MHz	1.800 MHz
0	1	27.00 MHz	2.700 MHz	3.000 MHz
1	0	27.00 MHz	33.8688 MHz	22.5792 MHz
1	1	27.00 MHz	33.8688 MHz	24.576 MHz

Block Diagram



Pin Configuration



Pin Description[1]

Pin #	Name	I/O	Description
3,4	27-1Out 27-2Out	O	3.3V fixed-frequency 27.00-MHz clock outputs. See *Table 1* on page 1 for frequency selection for test mode functionality.
9,10	512-1Out 512-2Out	O	3.3V fixed frequency clock outputs. See *Table 1* on page 1 for frequency selection.
13,15	33-1Out 33-2Out	O	3.3V fixed frequency 33.8688-MHz clock outputs. See *Table 1* on page 1 for frequency selection for test mode functionality.
14*	FSEL	I	Frequency selection input. This pin controls the frequency that is present on two 512 output clock pins.
8	XTO	O	On-chip reference oscillator pin. Drives an external crystal. When an externally generated reference signal is used at XTI, this pin remains unconnected. Bypass with a proper capacitance to ground to match the external crystal's load capacitance.
7	XTI	I	On-chip reference oscillator input pin. Requires either an external crystal (nominally 27 MHz) or externally generated reference signal. Bypass with a proper capacitance to ground to match the external crystal's load capacitance.
1, 5, 12	VDD	PWR	3.3V Power supply.
2,6,11	VSS	PWR	Device ground for all circuitry
16	TEST	I	Internal pull up. If this input pin is asserted low, it will set this device into a test mode. See *Table 1* on page 1.

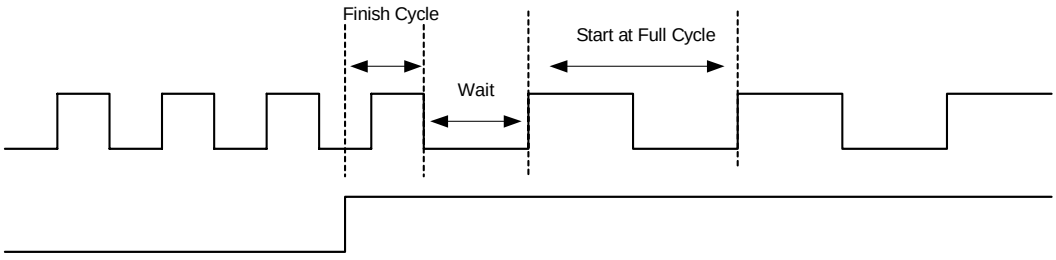
Note:
1. **Table Nomenclature:** All pin numbers with an asterisks (*) immediately after them indicates that they have an internal pull-up resistor to ensure that they will be sensed as a logic HIGH even if no external circuitry is attached to them. I = Input pins, O = Output pins and PWR = Power connection pins.

Table 2. Maximum Lumped Capacitative Output Loads

Clock	Max Load	Units
27-1Out	40	pF
27-2Out	25	pF
33-1Out,33-2Out, 512-1Out,512-2Out	15	pF

FSEL Switching Synchronization

The FSEL input is used to select the frequency of the clocks on the 512-1Out and 512-2Out pins. The device contains internal clock edge synchronization to insure that when the state of this pin is changed while the clocks are running no short (runt) or long (stretched) clocks will occur in the output streams. This is to say that the transitions will be made at a naturally occurring clock edge of the former clocks period and the cycle immediately after the change will be of a full newly selected clocks period and duty cycle.



Maximum Ratings

Maximum Input Voltage Relative to V_{SS}: .....V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}:..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to +150°C

Operating Temperature: .....–10°C to +75°C

Maximum ESD protection 2KV

Maximum Power Supply: 5.5V

Operating Voltage: 2.5–3.6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters (V_{DD} = 3.3V ± 10%, T_A = –10°C to +75°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	Note 2	-	-	0.8	Vdc
V_{IH}	Input High Voltage		2.0	-	-	Vdc
I_{IL}	Input Low Current	For internal Pull-up resistors, Notes 2 & 3 I_{IL} measured at V_{IN} = GND, I_{IH} measured at V_{IN} = V_{DD}	–18	–8	–3.5	µA
I_{IH}	Input High Current		-	-	5	µA
V_{HYS}	Input Hysteriss	Note 2	250	410	750	mV
$I_{dd3.3V}$	Dynamic Supply Current	Test = 1, FSEL=1, Note 4	-	48	60	mA
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = 4.0 mA	2.4	-	-	V
C_{in}	Input Pin Capacitance		-	-	5	pF
C_{out}	Output Pin Capacitance		-	-	6	pF
L_{pin}	Pin Inductance		-	-	7	nH
C_{xtal}	Crystal Pin Capacitance		-	5	-	pF

AC Parameters [5]

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{ERR}	Frequency Error, all outputs	XTI = 27.00 MHz	-	-	0	ppm
T_R	Rise Time	All clocks at rated load, Note 6	-	2	5	ns
T_F	Fall Time	All clocks at rated load, Note 6	-	2	5	ns
T_{PU}	Power up to Stable Output	All Output Clocks, Note 7	-	-	3	ms
T_{DC1}	Clock Duty Cycle (all output clocks)	All clocks at rated load, Note 7	45	50	55	%
T_{j2}	Clock Jitter (33-1Out,33-2Out)	Cycle to cycle jitter (Peak -maximum) All clocks at rated load Note 7	-	150	200	ps
T_{j2}	Clock Jitter (512-1Out,512-2Out)		-	150	200	ps
T_{j3}	Clock Jitter (27-1Out,27-2Out)		-	-	350	ps
T_{XS}	Crystal Oscillator Start-up Time		-	-	40	µs

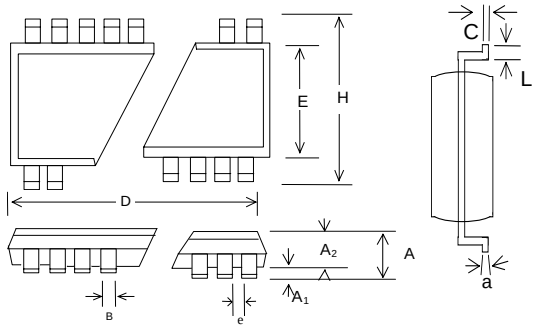
Notes:

2. Applicable to input signal: FSEL and Test pins.
3. Although internal pull-up resistors have a typical value of 400K, this value may vary between 200K and 800K.
4. All outputs loaded as per*Table 2* on page 2.
5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.
6. Measured between 0.2* V_{DD} and 0.8*Volts.
7. Trigerring is done at 1.5V.

Ordering Information

Part Number	Package Type	Product Flow
CY24233ZC	16-Pin TSSOP	Commercial, -10° to 75°C

Package Drawing and Dimensions



16 Pin TSSOP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.193	0.197	0.201	4.90	5.00	5.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	-	8°	0°	-	8°

Revision History

Document Title: CY24233 Clock Generator for DVD Players Document Number: 38-07132				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110596	11/29/01	DMG	New data sheet