



CYPRESS

PRELIMINARY

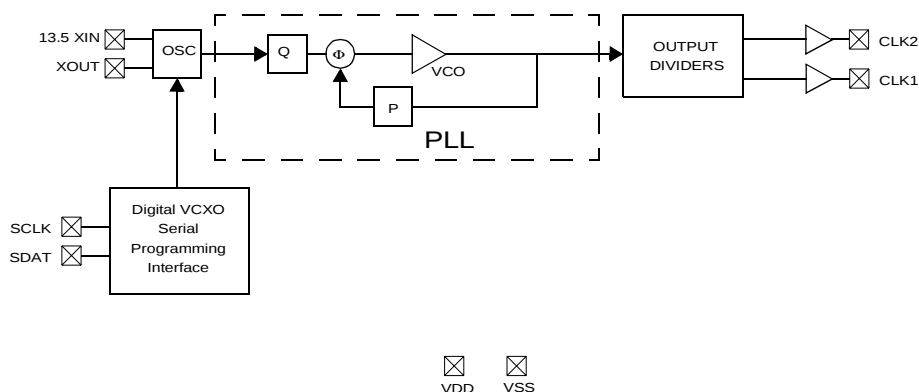
CY24202

27-MHz Clock Generator with Serial Programming Interface

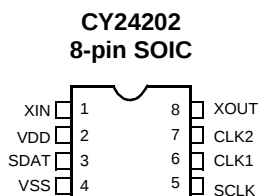
Features	Benefits
• Integrated phase-locked loop	High-performance PLL tailored for multimedia applications
• Low jitter, high accuracy outputs	Meets critical timing requirements in complex system designs
• Serial Programming Interface (SPI)	Dynamic Digital VCXO control
• 3.3V Operation	Enables application compatibility in low power systems

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24202	2	13.5-MHz pullable crystal input per Cypress Specification	2 copies of 27 MHz

Logic Block Diagram



Pin Configuration



Summary

Name	Pin Number	Description
XIN	1	Reference Crystal Input
VDD	2	Voltage Supply
SDAT	3	Digital VCXO Serial Data Input
VSS	4	Ground
SCLK	5	Digital VCXO Serial Clock Input
CLK1	6	Clock Output 1 @ 27 MHz
CLK2	7	Clock Output 2 @ 27 MHz
XOUT ^[1]	8	Reference Crystal Output

Pullable Crystal Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
CR _{load}	Crystal Load Capacitance		14		pF
C0/C1			240		
ESR	Equivalent Series Resistance		35		Ω
T ₀	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			±20	ppm
TT _s	Stability over temperature and aging			±50	ppm

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Reference Frequency		13.5		MHz

Notes:

1. Float XOUT if XIN is externally driven.
2. Rated for 10 years.

DC Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		μA
I_{VDD}	Supply Current			20	30	mA

AC Electrical Characteristics ($V_{DD} = 3.3V$)

Parameter ^[3]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 4, 50% of VDD	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of VDD	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% - 20% of VDD	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter			175	ps
t_{10}	PLL Lock Time				3	ms

Note:

3. Not 100% tested.

Serial Programmable Interface Protocol

The CY24202 utilizes a 2-wire interface SDAT and SCLK that operates up to 400 kbits/sec in Read or Write mode. The basic Write serial format is as follows: Start Bit; 7-bit Device Address (DA); R/w Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit, as illustrated in Figure 1.

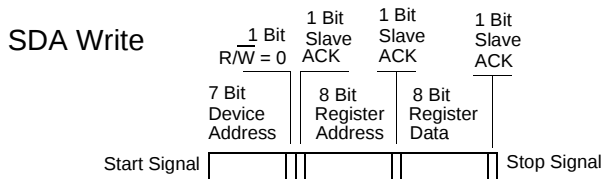


Figure 1. Data Frame Architecture

Data Valid

Data is valid when the Clock is HIGH, and may only be transitioned when the clock is LOW as illustrated in Figure 2.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 3.

Start Sequence

Start Frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given the next 8-bit data must be the device address (7 bits) and a R/w bit (0 for write), followed by register address (8 bits) and register data (8 bits). See Figure 3.

Stop Sequence

Stop Frame is indicated by SDAT going high when SCLK is high. A Stop Frame frees the bus for writing to another part on the same bus or writing to another random register address. See Figure 3.

Acknowledge Pulse

During Write Mode the CY24202 will respond with an Acknowledge pulse after every 8 bits. This is accomplished by pulling the SDAT line low during the next clock cycle after the 8th bit is shifted in.

Device Address

The 7 bit device address is 1101001.

Register Address

The 8 bit address for the VCXO register is 00010011.

Register Data

The register data can be any value between 00H - FFH. As you increase the value, the capacitance on the XIN and XOUT pins will increase, thereby decreasing the xtal frequency.

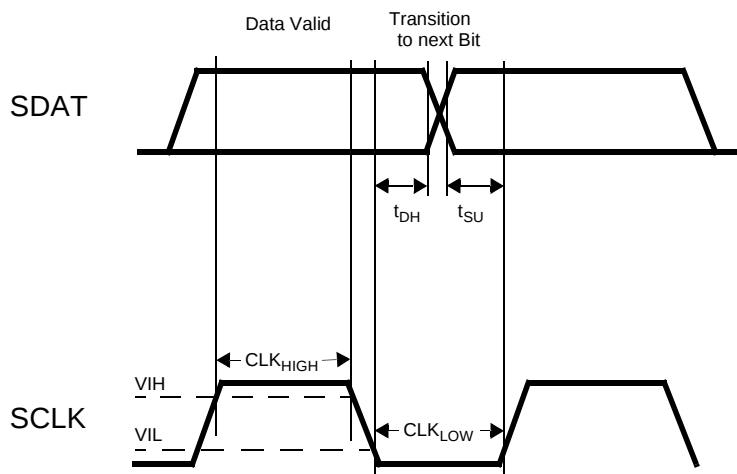


Figure 2. Data Valid and Data Transition Periods

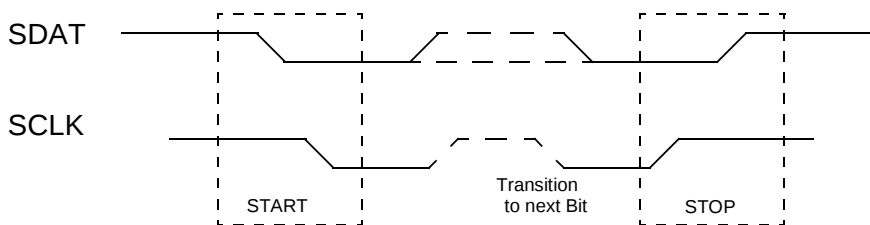


Figure 3. Start and Stop Frame

Serial Programming Interface Timing Specifications

Parameter	Description	Min.	Max.	Unit
f_{SCL}	Frequency of SCLK		400	kHz
	Start Mode Time from SDAT LOW to SCLK LOW	0.6		μ s
CLK_{LOW}	SCLK LOW Period	1.3		μ s
CLK_{HIGH}	SCLK HIGH Period	0.6		μ s
t_{SU}	Data Transition to SCLK HIGH	100		ns
t_{DH}	Data Hold (SCLK LOW to Data Transition)	0		ns
	Rise Time of SCLK and SDAT		300	ns
	Fall Time of SCLK and SDAT		300	ns
	Stop Mode Time from SCLK HIGH to SDA HIGH	0.6		μ s
	Stop Mode to Start Mode	1.3		μ s

Test Circuit

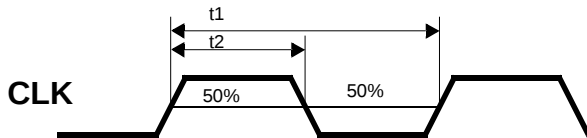
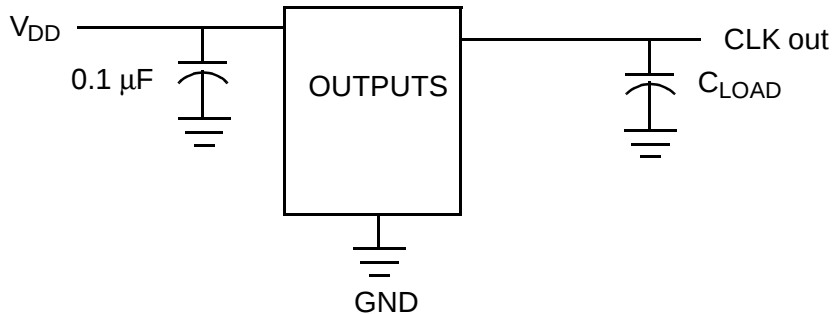


Figure 4. Duty Cycle Definition; DC = t₂/t₁

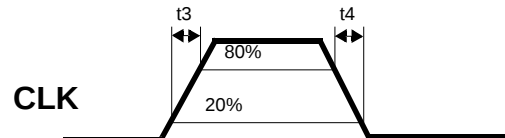


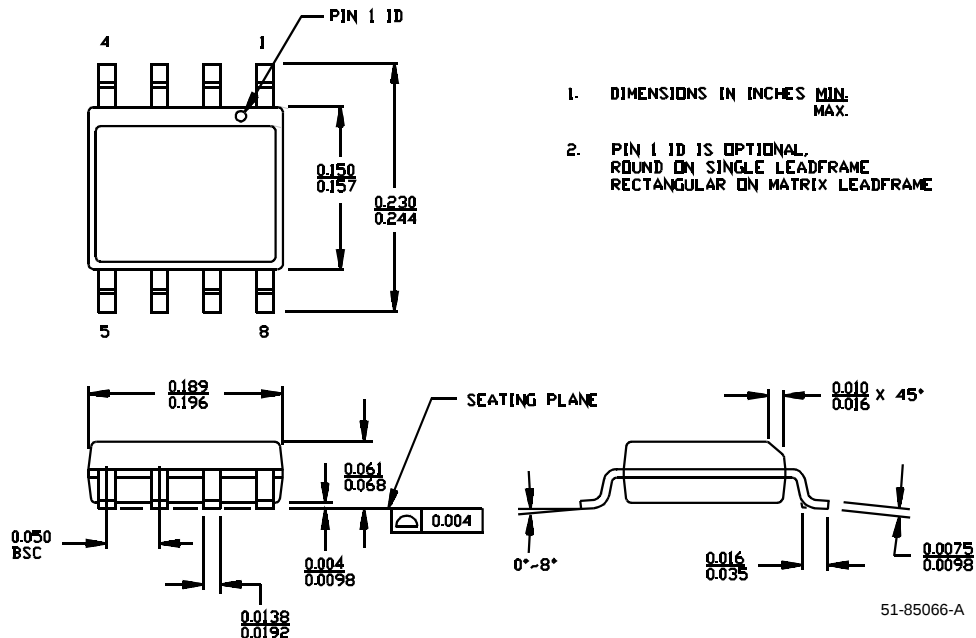
Figure 5. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24202SC	S8	8-Pin SOIC	Commercial	3.3V

Package Diagram

8-Lead (150-Mil) SOIC S8





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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111424	02/27/02	CKN	New data sheet