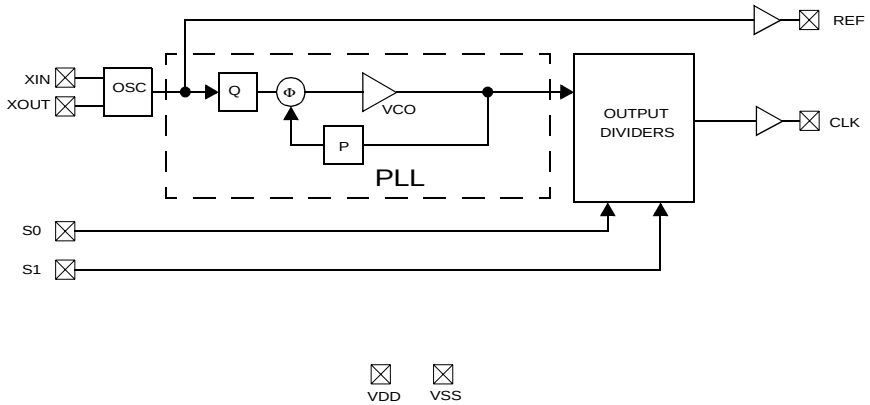
MediaClock™ for LCD Projectors

Features	Benefits
• **Integrated phase-locked loop**	High-performance PLL tailored for projector applications
• **Low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **3.3V operation**	Enables application compatibility
• **8-pin SOIC package**	Industry standard package saves on board space

Part Number	Outputs	Input Frequency	Output Frequencies
CY24126	2	24 MHz	24 MHz, 48.00 MHz/120.00 MHz (selectable)

Logic Block Diagram



Pin Configurations

CY24126
8-pin SOIC

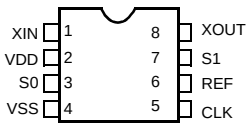


Table 1.

XIN (MHz)	S1[1]	S0	CLK (MHz)	Note
24.00	L	L	120.00	x5
24.00	H	L	48.00	x2
24.00	X	H	disable	-

Note:
1. X = don't care.

Pin Summary

Name	Pin Number	Description
XIN	1	Reference Input (24-MHz crystal or external input)
VDD	2	3.3V Voltage Supply
S0	3	CLK Select Line, see *Table 1*
VSS	4	Ground
CLK	5	48.00 MHz/120.00 MHz (frequency selectable). See *Table 1*
REF	6	Reference output
S1	7	Clock select line, see *Table 1*
XOUT[2]	8	Drives an external crystal

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[3]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
f_{REF}	Reference Frequency	–	24	–	MHz

DC Electrical Characteristics

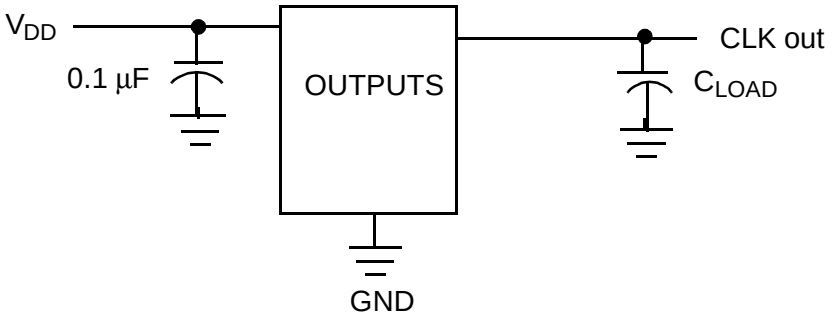
Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24	–	mA
C_{IN}	Input Capacitance		–	–	7	pF
I_{IZ}	Input Leakage Current		–	5	–	µA
I_{DD}	Supply Current	No output load	–	–	35	mA

AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter[4]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of V_{DD}	0.8	1.4	–	V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% - 20% of V_{DD}	0.8	1.4	–	V/ns
t_9	Clock Jitter	Peak to Peak period jitter	–	–	350	ps
t_{10}	PLL Lock Time		–	–	3	ms

Notes:
2. Float XOUT if XIN is externally driven.
3. Rated for 10 years.
4. Not 100% tested.

Test Circuit



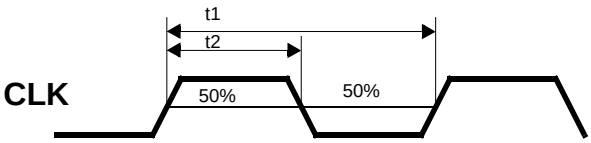


Figure 1. Duty Cycle Definition; DC = t2/t1

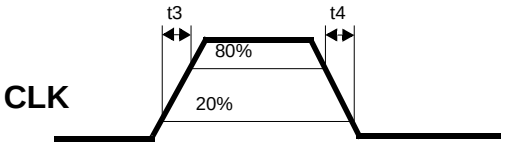


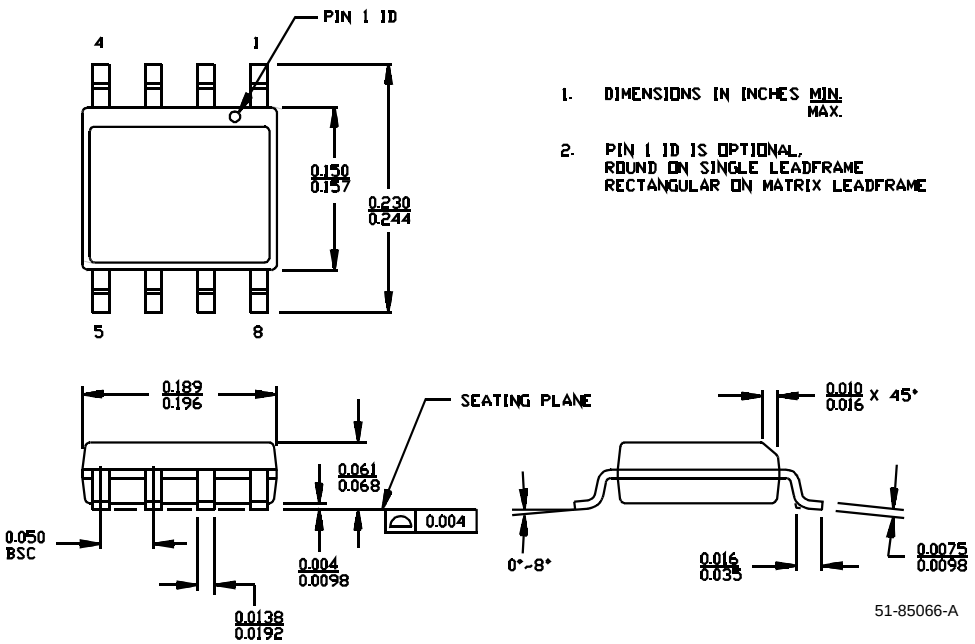
Figure 2. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24126SC	S8	8-Pin SOIC	Commercial	3.3V

Package Diagram

8-Lead (150-Mil) SOIC S8



Document Title: CY24126 MediaClock™ for LCD Projectors Document Number: 38-07326				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111595	03/01/02	CKN	New data sheet