



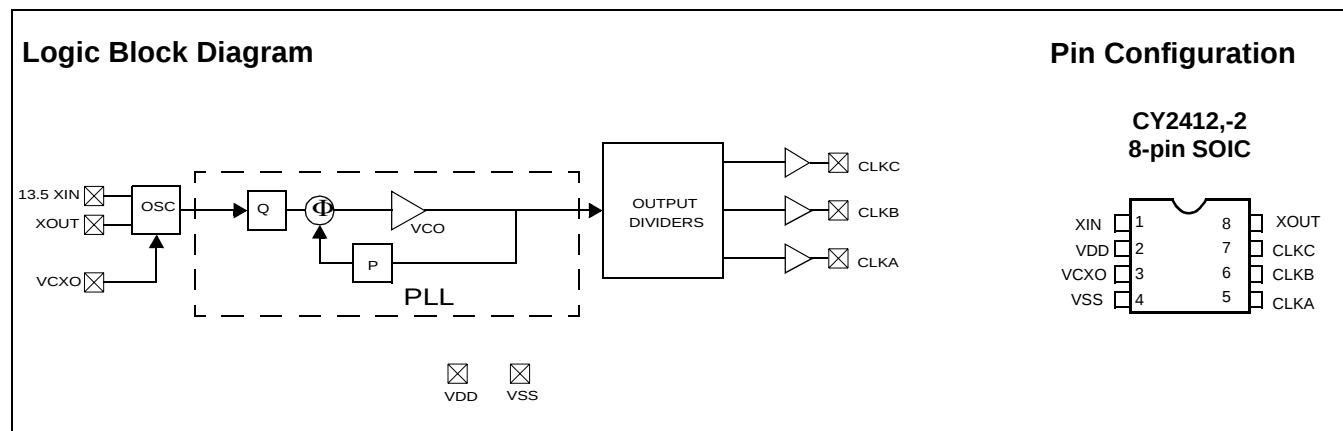
CYPRESS

CY2412

MPEG Clock Generator with VCXO

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• VCXO with analog adjust	Large ± 150 -ppm range, better linearity
• 3.3V operation	Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY2412	3	13.5-MHz pullable crystal input per Cypress specification	Two 27-MHz outputs, one 54-MHz output (3.3V)
CY2412-2	3	13.5-MHz pullable crystal input per Cypress specification	27 MHz, 13.5 MHz, 54 MHz (3.3V)



Pin Summary

Name	Pin Number	Description
X _{IN}	1	Reference Crystal Input
V _{DD}	2	Voltage Supply
VCXO	3	Input Analog Control for VCXO
V _{SS}	4	Ground
CLKA	5	54-MHz clock output
CLKB	6	27-MHz clock output (-1)
CLKB	6	13.5-MHz clock output (-2)
CLKC	7	27-MHz clock output
X _{OUT} ^[1]	8	Reference Crystal Output

Pullable Crystal Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
CR _{load}	Crystal Load Capacitance		14		pF
C0/C1			240		
ESR	Equivalent Series Resistance		35		Ω
T ₀	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT _s	Stability over Temperature and Aging			± 50	ppm

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	3.14	3.3	3.47	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Reference Frequency		13.5		MHz

Notes:

1. Float X_{OUT} if X_{IN} is externally driven.
2. Rated for ten years.

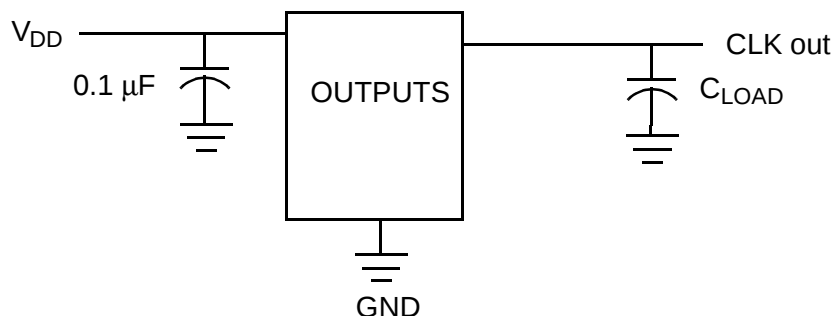
DC Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		μA
$f_{\Delta XO}$	VCXO pullability range		-150		+150	ppm
V_{VCXO}	VCXO input range		0		V_{DD}	V
f_{VBW}	VCXO input bandwidth			DC to 200		kHz
I_{DD}	Supply Current	Sum of Core and Output Current			35	mA

AC Electrical Characteristics

Parameter ^[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of V_{DD}	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter		100	200	ps
t_{10}	PLL Lock Time				3	ms

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2412SC	S8	8-pin SOIC	Commercial	3.3V
CY2412SC-2	S8	8-pin SOIC	Commercial	3.3V

Note:

3. Not 100% tested.

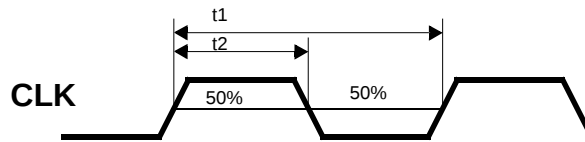


Figure 1. Duty Cycle Definition; $DC = t2/t1$

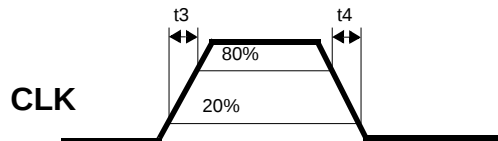
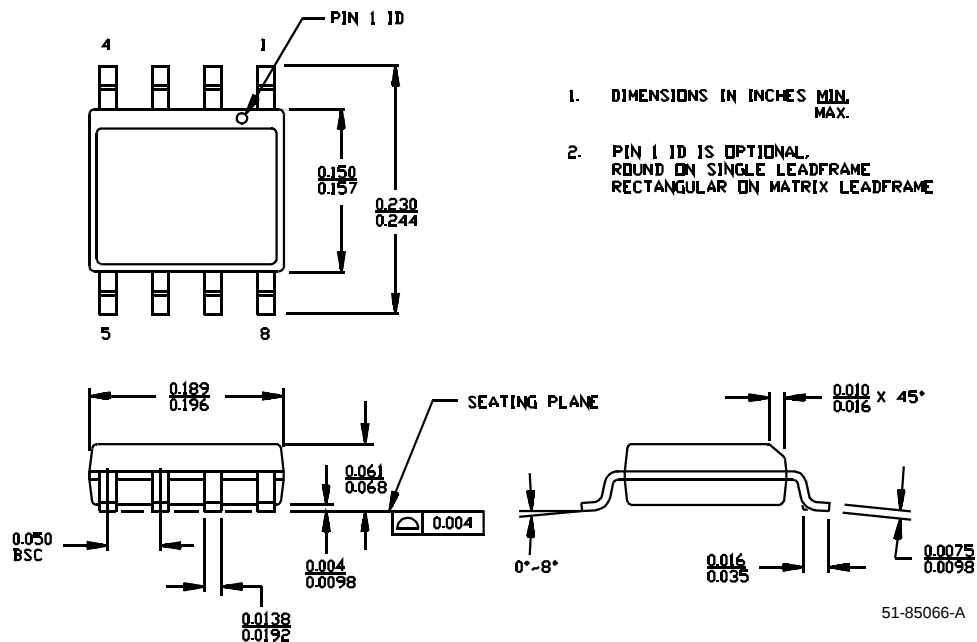


Figure 2. Rise and Fall Time Definitions

Package Diagram

8-lead (150-mil) SOIC S8



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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110492	10/28/01	SZV	Change from Spec number: 38-00898 to 38-07227
*A	112457	03/14/02	CKN	Added CY2412-2 to data sheet