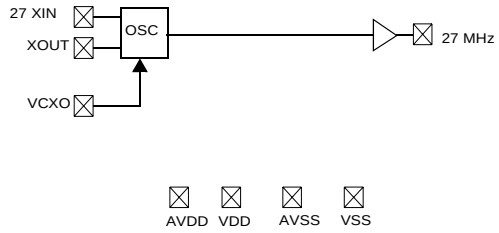
MediaClock™ 27-MHz VCXO Clock Generator

Features	Benefits
• Low-jitter, high-accuracy output	Meets critical timing requirements in complex system designs
• VCXO with analog adjust	Large ± 150 ppm range, better linearity
• 3.3V operation	

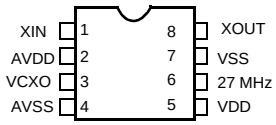
Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24119	1	27-MHz pullable crystal per Cypress Specification	One copy of 27 MHz (3.3V)

Logic Block Diagram



Pin Configuration

CY24119
8-pin SOIC



Pin Summary

Name	Pin Number	Description
A_{VDD}	2	Analog Voltage Supply
V_{DD}	5	Output Voltage Supply
AV_{SS}	4	Analog Ground
V_{SS}	7	Output Ground
X_{IN}	1	Reference Crystal Input
V_{CXO}	3	Analog Control for V_{CXO}
X_{OUT}	8	Reference Crystal Output
27 MHz	6	27-MHz Clock Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[1]	–65	125	°C
T_J	Junction Temperature		125	°C
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}, AV_{DD}	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0		70	° C
C_{LOAD}	Max Load Capacitance			15	pF
f_{REF}	Reference Frequency	10	27	30	MHz

DC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output HIGH Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$ (source)	12	24		mA
I_{OL}	Output LOW Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$ (sink)	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		µA
$f_{\Delta xo}$	V_{CXO} Pullability Range		–150		+150	ppm
V_{VCXO}	V_{CXO} Input Range		0		AV_{DD}	V
f_{VBW}	V_{CXO} Input Bandwidth			DC to 200		kHz
I_{DD}	Supply Current	Sum of Core and Output Current			13	mA

Pullable Crystal Specifications

Parameter	Name	Min.	Typ.	Max.	Unit
CR_{load}	Crystal Load Capacitance		13		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T_o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			±20	ppm
TT_s	Stability over Temperature and Aging		±20	±50	ppm

Notes:
1. Rated for 10 years.

AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter[2]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of V_{DD}	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak-to-Peak Period Jitter			100	ps

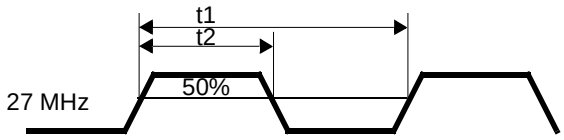


Figure 1. Duty Cycle Definition; DC = t_2/t_1

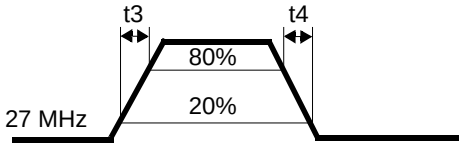
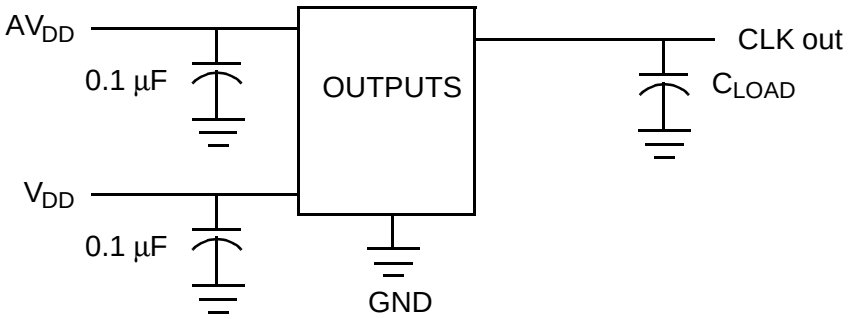


Figure 2. Rise and Fall Time Definitions



Test Circuit

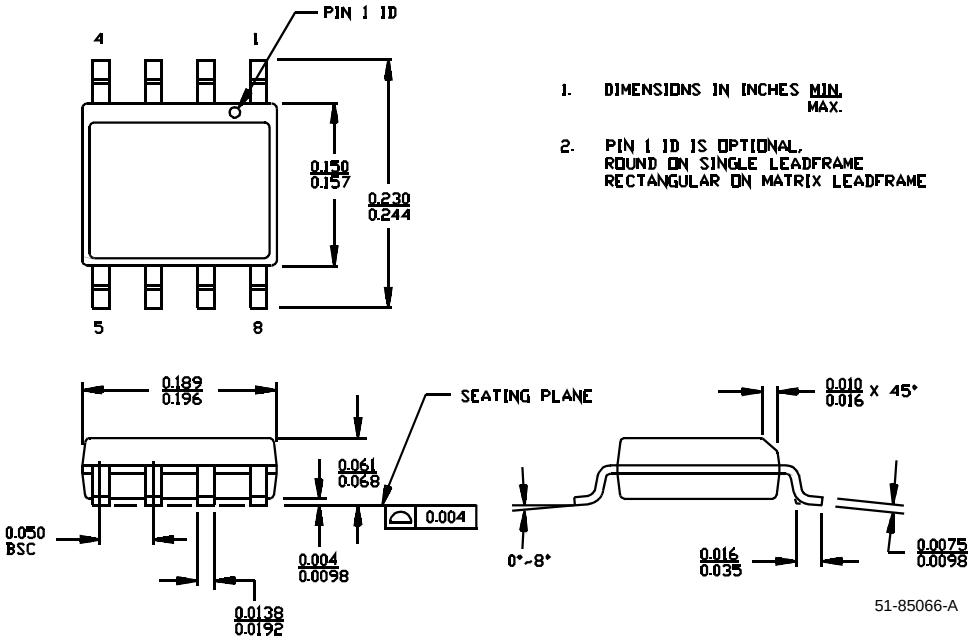
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24119-SC	S8	8-pin SOIC	Commercial	3.3V
CY24119-SCT	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V

Note:
2. Not 100% tested.

Package Diagram

8-lead (150-mil) SOIC S8



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111551	03/22/02	CKN	New Data Sheet