



14 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMs

Features

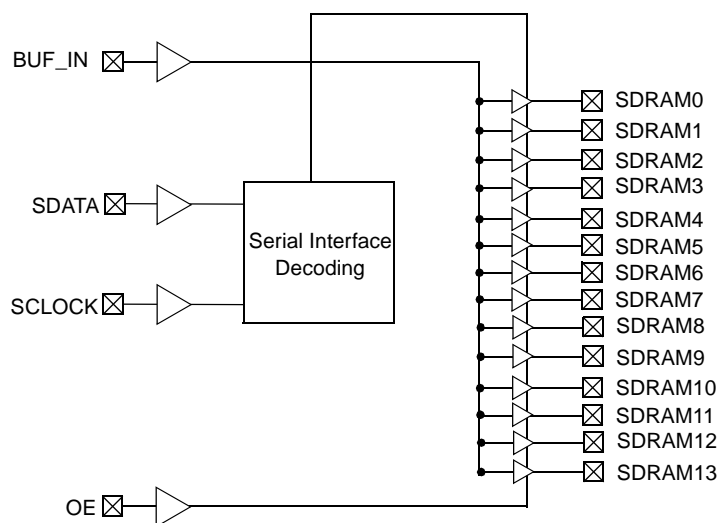
- One input to 14 output buffer/driver
- Supports up to three SDRAM DIMMs
- Two additional outputs for feedback
- Serial interface for output control
- Low skew outputs
- Up to 100-MHz operation
- Multiple V_{DD} and V_{SS} pins for noise reduction
- Dedicated OE pin for testing
- Low EMI outputs
- 28-pin SOIC (300-mil) package
- 3.3V operation

Functional Description

The CY2314ANZ is a 3.3V buffer designed to distribute high-speed clocks in desktop PC applications. The part has 14 outputs, 12 of which can be used to drive up to three SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium® II processors. The CY2314ANZ can be used in conjunction with the CY2280, CY2281, CY2282 or similar clock synthesizer for a complete Pentium II motherboard solution.

The CY2314ANZ also includes a serial interface which can enable or disable each output clock. On power-up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

Block Diagram



Pin Configuration

| 28-pin SOIC Top View | | | |
|-------------------------|----|----|-------------|
| V_{DD} | 1 | 28 | V_{DD} |
| SDRAM0 | 2 | 27 | SDRAM11 |
| SDRAM1 | 3 | 26 | SDRAM10 |
| V_{SS} | 4 | 25 | V_{SS} |
| V_{DD} | 5 | 24 | V_{DD} |
| SDRAM2 | 6 | 23 | SDRAM9 |
| SDRAM3 | 7 | 22 | SDRAM8 |
| V_{SS} | 8 | 21 | V_{SS} |
| BUF_IN | 9 | 20 | OE |
| SDRAM4 | 10 | 19 | SDRAM7 |
| SDRAM5 | 11 | 18 | SDRAM6 |
| SDRAM12 | 12 | 17 | SDRAM13 |
| V_{DDIIC} | 13 | 16 | V_{SSIIC} |
| SDATA | 14 | 15 | SCLK |

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Pin Summary

| Name | Pins | Description |
|--------------------|--|---|
| V _{DD} | 1, 5, 24, 28 | 3.3V Digital voltage supply |
| V _{SS} | 4, 8, 21, 25 | Ground |
| V _{DDIIC} | 13 | Serial interface voltage supply |
| V _{SSIIC} | 16 | Ground for serial interface |
| BUF_IN | 9 | Input clock |
| OE | 20 | Output Enable, three-states outputs when LOW. Internal pull-up to V _{DD} |
| SDATA | 14 | Serial data input, internal pull-up to V _{DD} |
| SCLK | 15 | Serial clock input, internal pull-up to V _{DD} |
| SDRAM [0-13] | 2, 3, 6, 7, 10, 11, 18, 19, 22, 23, 26, 27, 12, 17 | SDRAM clock outputs |

Device Functionality

| OE | SDRAM [0-13] |
|----|--------------|
| 0 | High-Z |
| 1 | 1 x BUF_IN |

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

.

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0"
- Serial interface address for the CY2314ANZ is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|------|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | ---- |

Byte 0:SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enabled

| Bit | Pin # | Description |
|-------|-------|--------------------------|
| Bit 7 | 11 | SDRAM5 (Active/Inactive) |
| Bit 6 | 10 | SDRAM4 (Active/Inactive) |
| Bit 5 | -- | Reserved, drive to 0 |
| Bit 4 | -- | Reserved, drive to 0 |
| Bit 3 | 7 | SDRAM3 (Active/Inactive) |
| Bit 2 | 6 | SDRAM2 (Active/Inactive) |
| Bit 1 | 3 | SDRAM1 (Active/Inactive) |
| Bit 0 | 2 | SDRAM0 (Active/Inactive) |

Byte 1: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

| Bit | Pin # | Description |
|-------|-------|---------------------------|
| Bit 7 | 27 | SDRAM11 (Active/Inactive) |
| Bit 6 | 26 | SDRAM10 (Active/Inactive) |
| Bit 5 | 23 | SDRAM9 (Active/Inactive) |
| Bit 4 | 22 | SDRAM8 (Active/Inactive) |
| Bit 3 | -- | Reserved, drive to 0 |
| Bit 2 | -- | Reserved, drive to 0 |
| Bit 1 | 19 | SDRAM7 (Active/Inactive) |
| Bit 0 | 18 | SDRAM6 (Active/Inactive) |

Byte 2: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

| Bit | Pin # | Description |
|-------|-------|---------------------------|
| Bit 7 | 17 | SDRAM13 (Active/Inactive) |
| Bit 6 | 12 | SDRAM12 (Active/Inactive) |
| Bit 5 | -- | Reserved, drive to 0 |
| Bit 4 | -- | Reserved, drive to 0 |
| Bit 3 | -- | Reserved, drive to 0 |
| Bit 2 | -- | Reserved, drive to 0 |
| Bit 1 | -- | Reserved, drive to 0 |
| Bit 0 | -- | Reserved, drive to 0 |

Maximum Ratings

Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage (Except BUF_IN)..... -0.5V to $V_{DD} + 0.5V$
 DC Input Voltage (BUF_IN)..... -0.5V to +7.0V

Storage Temperature -65°C to +150°C
 Junction Temperature 150°C
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) >2000V

Operating Conditions ^[1]

| Parameter | Description | Min. | Max. | Unit |
|-----------|---|-------|-------|------|
| V_{DD} | Supply Voltage | 3.135 | 3.465 | V |
| T_A | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| C_L | Load Capacitance | | 30 | pF |
| C_{IN} | Input Capacitance | | 7 | pF |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-------------|--|--|------|------|------|
| V_{IL} | Input LOW Voltage ^[2] | Except serial interface pins | | 0.8 | V |
| V_{ILiic} | Input LOW Voltage | For serial interface pins only | | 0.7 | V |
| V_{IH} | Input HIGH Voltage ^[2] | | 2.0 | | V |
| I_{IL} | Input LOW Current (BUF_IN input) | $V_{IN} = 0V$ | -10 | 10 | μA |
| I_{IL} | Input LOW Current (Except BUF_IN Pin) | $V_{IN} = 0V$ | | 100 | μA |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | -10 | 10 | μA |
| V_{OL} | Output LOW Voltage ^[3] | $I_{OL} = 25\text{ mA}$ | | 0.4 | V |
| V_{OH} | Output HIGH Voltage ^[3] | $I_{OH} = -36\text{ mA}$ | 2.4 | | V |
| I_{DD} | Supply Current ^[3] | Unloaded outputs, 100 MHz | | 200 | mA |
| I_{DD} | Supply Current ^[3] | Loaded outputs, 100 MHz | | 290 | mA |
| I_{DD} | Supply Current ^[3] | Unloaded outputs, 66.67 MHz | | 150 | mA |
| I_{DD} | Supply Current ^[3] | Loaded outputs, 66.67 MHz | | 185 | mA |
| I_{DDS} | Supply Current | BUF_IN= V_{DD} or V_{SS} All other inputs at V_{DD} | | 500 | μA |

Notes:

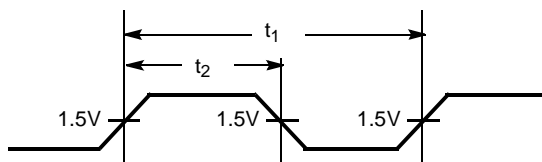
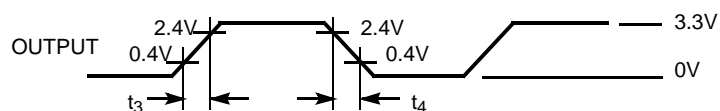
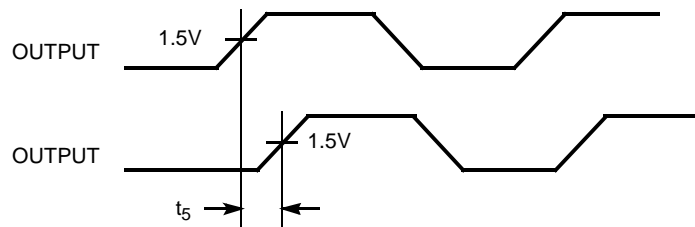
1. Electrical parameters are guaranteed under the operating conditions specified.
2. BUF_IN input has a threshold voltage of $V_{DD}/2$.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics^[4] Over the Operating Range

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------|---|--------------------------------|------|------|------|------|
| | Maximum Operating Frequency | | | | 100 | MHz |
| | Duty Cycle ^[3, 5] = $t_2 \div t_1$ | Measured at 1.5V | 45.0 | 50.0 | 55.0 | % |
| t_3 | Rising Edge Rate ^[3] | Measured between 0.4V and 2.4V | 0.9 | 1.5 | 4.0 | V/ns |
| t_4 | Falling Edge Rate ^[3] | Measured between 2.4V and 0.4V | 0.9 | 1.5 | 4.0 | V/ns |
| t_5 | Output to Output Skew ^[3] | All outputs equally loaded | -250 | | +250 | ps |
| t_6 | SDRAM Buffer LH Prop. Delay ^[3] | Input edge greater than 1 V/ns | 1.0 | 3.5 | 5.0 | ns |
| t_7 | SDRAM Buffer HL Prop. Delay ^[3] | Input edge greater than 1 V/ns | 1.0 | 3.5 | 5.0 | ns |
| t_8 | SDRAM Buffer Enable Delay ^[3] | Input edge greater than 1 V/ns | 1.0 | 5 | 12 | ns |
| t_9 | SDRAM Buffer Disable Delay ^[3] | Input edge greater than 1 V/ns | 1.0 | 20 | 30 | ns |

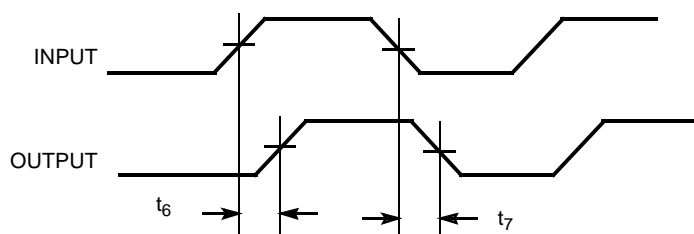
Notes:

4. All parameters specified with loaded outputs.
5. Duty cycle of input clock is 50%. Rising and falling edge rate of the input clock is greater than 1 V/ns.

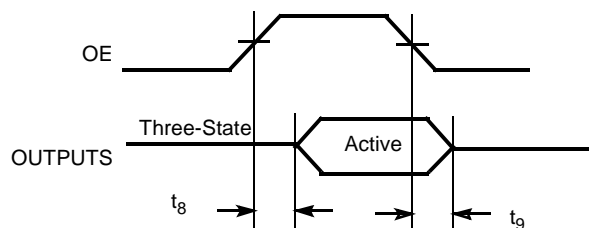
Switching Waveforms
Duty Cycle Timing

All Outputs Rise/Fall Time

Output-Output Skew


Switching Waveforms (continued)

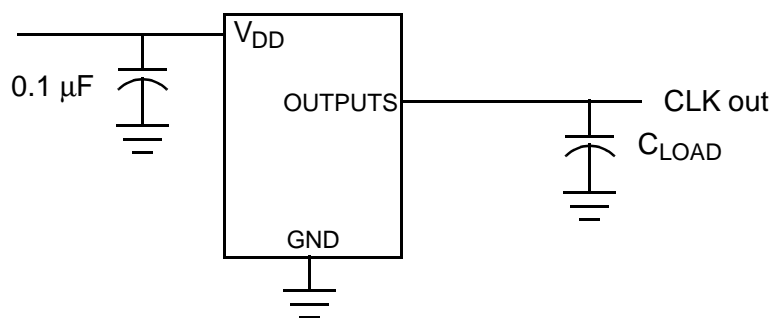
SDRAM Buffer LH and HL Propagation Delay



SDRAM Buffer Enable and Disable Times



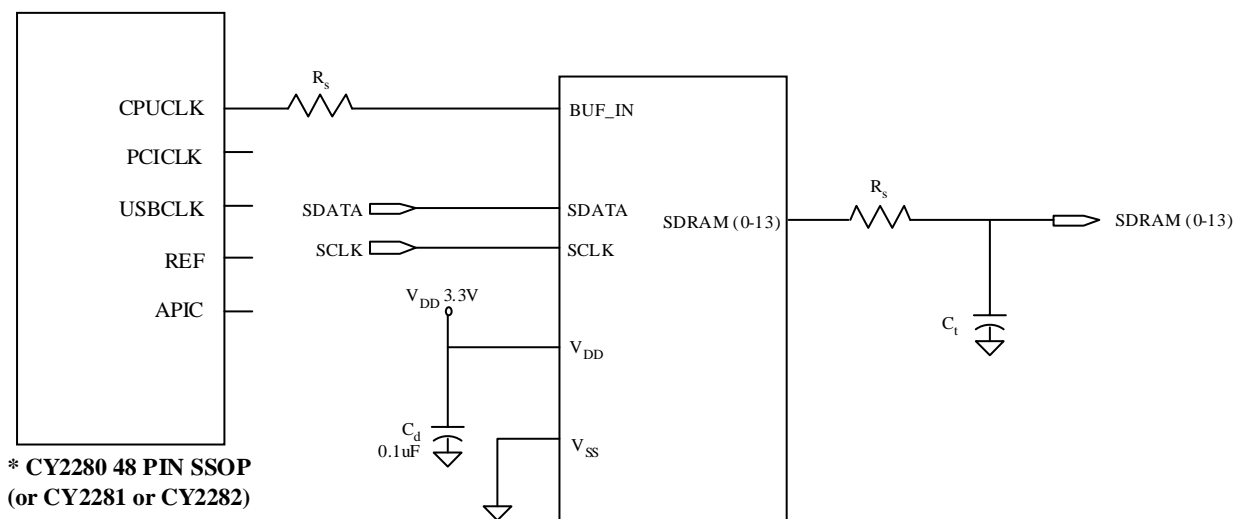
Test Circuit



Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.

Application Circuit



* CY2280 48 PIN SSOP
(or CY2281 or CY2282)

CY2314ANZ: 28-PIN SOIC

* THIS FREQUENCY SYNTHESIZER IS USED TO
GENERATE CPU, PCI, USB, REF, AND APIC CLOCKS.

C_d = DECOUPLING CAPACITORS
 C_t = OPTIONAL EMI-REDUCING CAPACITORS
 R_s = SERIES TERMINATING RESISTORS

Summary

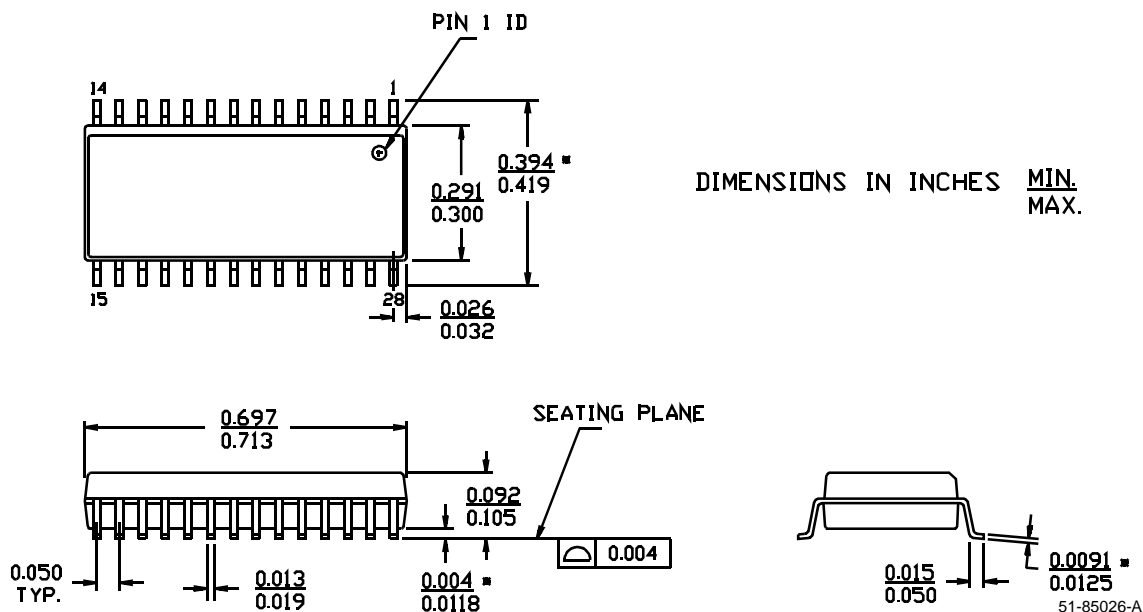
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the buffer (typically 25 Ω), and R_{series} is the series terminating resistor.
 $R_{series} > R_{trace} - R_{out}$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50 Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 μ F–22 μ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---------------|--------------|--------------|-----------------|
| CY2314ANZSC-1 | S28 | 28-Pin SOIC | Commercial |

Package Diagram

28-Lead (300-Mil) Molded SOIC S21



| Document Title: CY2314ANZ 14 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMs Document Number: 38-07143 | | | | |
|--|---------|------------|-----------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 110252 | 11/18/01 | DSG | Change from Spec number: 38-00687 to 38-07143 |