13 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMs

Features

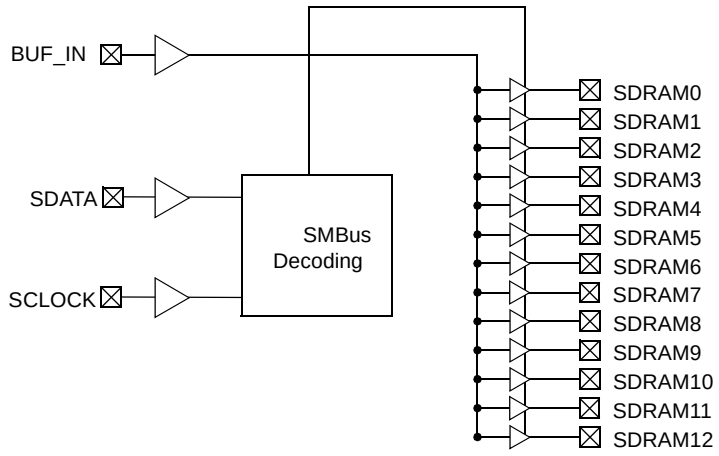
- **One input to 13 output buffer/driver**
- **Supports up to three SDRAM DIMMs**
- **One additional outputs for feedback**
- **SMBus interface for output control**
- **Low skew outputs**
- **Up to 100 MHz operation**
- **Multiple V_{DD} and V_{SS} pins for noise reduction**
- **Low EMI outputs**
- **28-pin SOIC (300-mil) package**
- **3.3V operation**

Functional Description

The CY2313BNZ is a 3.3V buffer designed to distribute high-speed clocks in desktop PC applications. The part has 13 outputs, 12 of which can be used to drive up to three SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium® II processors. The CY2313BNZ can be used in conjunction with the CY2280, CY2281, CY2282 or similar clock synthesizer for a complete Pentium II motherboard solution.

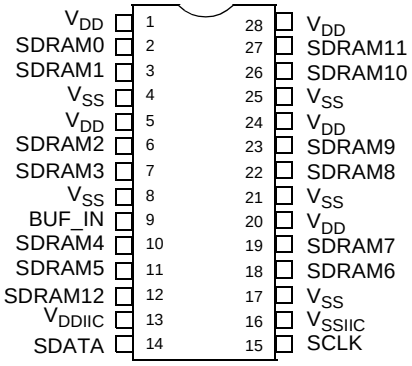
The CY2313BNZ also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled.

Block Diagram



Pin Configuration

28 SOIC
Top View



Pentium is a registered trademark of Intel Corporation.

Pin Summary

Name	Pins	Description
V_{DD}	1, 5, 20, 24, 28	3.3V Digital voltage supply
V_{SS}	4, 8, 17, 21, 25	Ground
V_{DDIIC}	13	SMBus Voltage supply
V_{SSIIC}	16	Ground for SMBus
BUF_IN	9	Input clock
SDATA	14	SMBus data input, internal pull-up to V_{DD}
SCLK	15	SMBus clock input, internal pull-up to V_{DD}
SDRAM [0-12]	2, 3, 6, 7, 10, 11, 12, 18, 19, 22, 23, 26, 27	SDRAM clock outputs

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to “0”
- SMBus Address for the CY2313BNZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 0: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enabled

Bit	Pin #	Description
Bit 7	11	SDRAM5 (Active/Inactive)
Bit 6	10	SDRAM4 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

Byte 1: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	27	SDRAM11 (Active/Inactive)
Bit 6	26	SDRAM10 (Active/Inactive)
Bit 5	23	SDRAM9 (Active/Inactive)
Bit 4	22	SDRAM8 (Active/Inactive)
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	19	SDRAM7 (Active/Inactive)
Bit 0	18	SDRAM6 (Active/Inactive)

Byte 2: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	--	Reserved, drive to 0
Bit 6	12	SDRAM12 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	--	Reserved, drive to 0
Bit 0	--	Reserved, drive to 0

Maximum Ratings

Supply Voltage to Ground Potential..... –0.5V to +7.0V
DC Input Voltage (Except BUF_IN).....–0.5V to V_{DD} + 0.5V
DC Input Voltage (BUF_IN)..... –0.5V to +7.0V

Storage Temperature ..... –65°C to +150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2000V
Ambient Temperature under BIAS..... –55°C to +125°C

Operating Conditions[1]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance		30	pF

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C

DC Electrical Characteristics: T_A = -40°C to +85°C, V_{DD} = 3.3V±5%

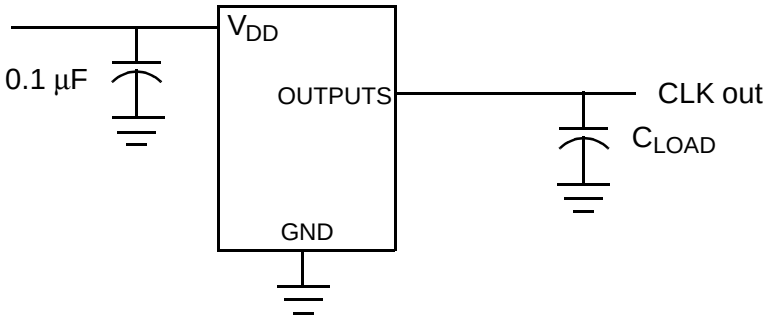
Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
I_{DD}	3.3V Supply Current	BUF_IN = 100 MHz			250	mA
Logic Inputs						
V_{IL}	Input Low Voltage		GND–0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}+0.5	V
I_{ILEAK}	Input Leakage Current, BUF_IN		–5		+5	µA
I_{ILEAK}	Input Leakage Current[1]		–20		+5	µA
Logic Outputs (SDRAM0:12)						
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	65	100	160	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	70	110	185	mA
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Note:
1. SDATA and SCLOCK logic pins have 250-kΩ internal pull-up resistors.

AC Electrical Characteristics: T_A = -40°C to +85°C, V_{DD} = 3.3V±5% (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency		0		133	MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
t_{SR}	Output Skew, Rising Edges				250	ps
t_{SF}	Output Skew, Falling Edges				250	ps
t_{EN}	Output Enable Time		1.0		8.0	ns
t_{DIS}	Output Disable Time		1.0		8.0	ns
t_{PR}	Rising Edge Propagation Delay		1.0		5.0	ns
t_{PF}	Falling Edge Propagation Delay		1.0		5.0	ns
t_D	Duty Cycle	Measured at 1.5V	45		55	%
Z_o	AC Output Impedance			15		Ω
t_{PR}	Rising Edge Propagation Delay		1.0		5.0	ns

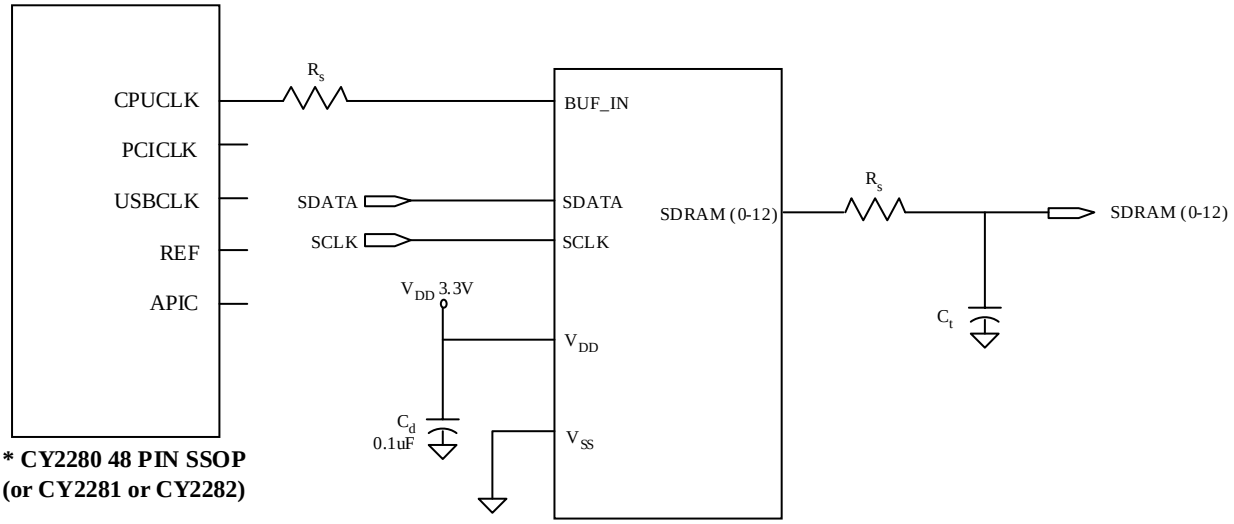
Test Circuit



Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



* THIS FREQUENCY SYNTHESIZER IS USED TO GENERATE CPU, PCI, USB, REF, AND APIC CLOCKS.

C_d = DECOUPLING CAPACITORS
C_t = OPTIONAL EMI-REDUCING CAPACITORS
R_s = SERIES TERMINATING RESISTORS

Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 mF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically 25W), and Rseries is the series terminating resistor.

  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50W impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 mF–22 mF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

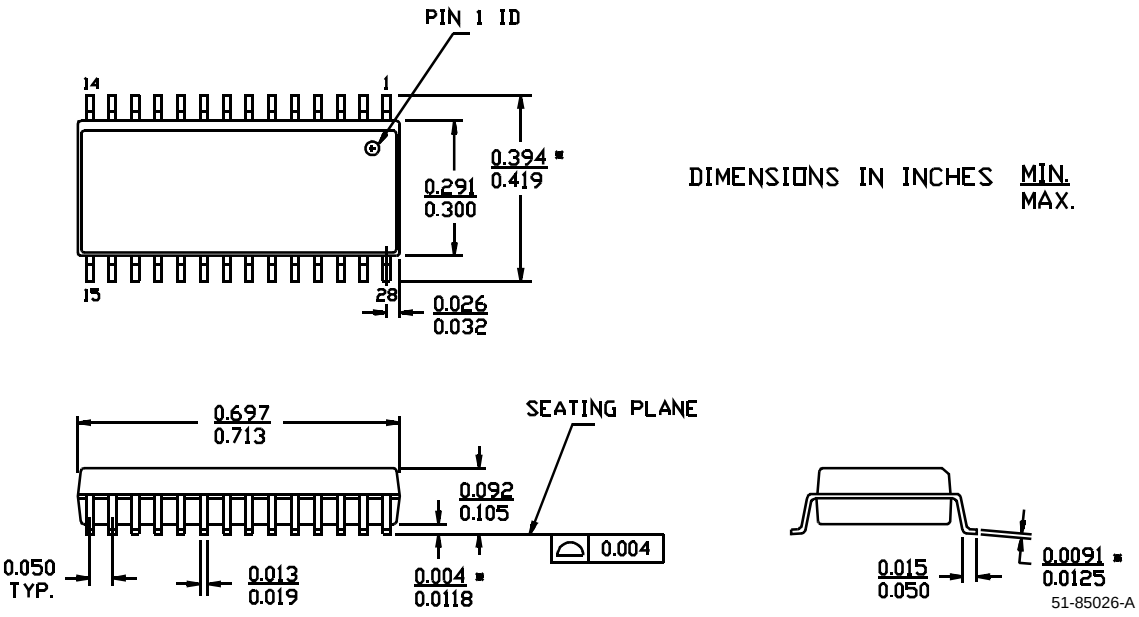
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2313BNZSI	S21	28-Pin SOIC	Industrial
CY2313BNZPVI*		28-Pin SSOP	Industrial
CY2313BNZZI*		28-Pin TSSOP	Industrial

*Call factory for availability

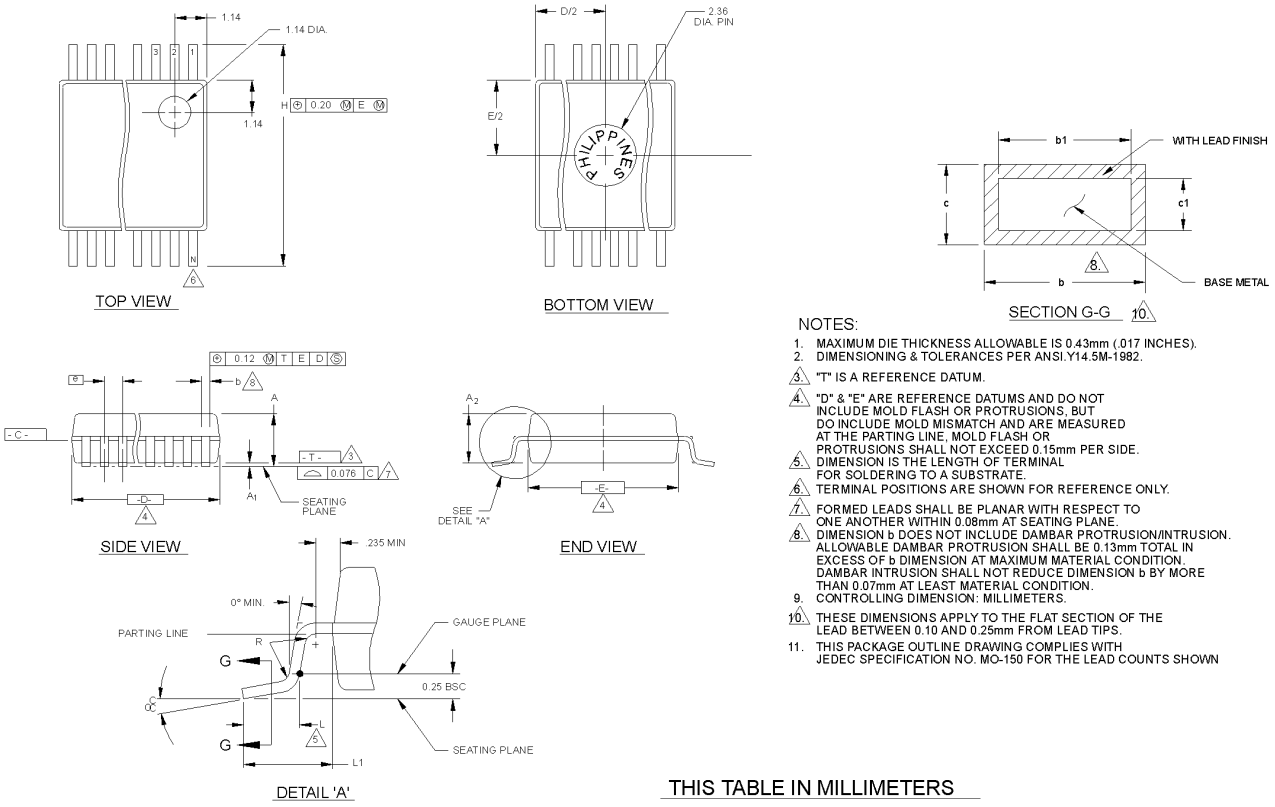
Package Diagram

28-Lead (300-Mil) Molded SOIC S21



Package Diagram

28-Pin Shrunk Small Outline Package (SSOP, 209-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	0.09	0.15							

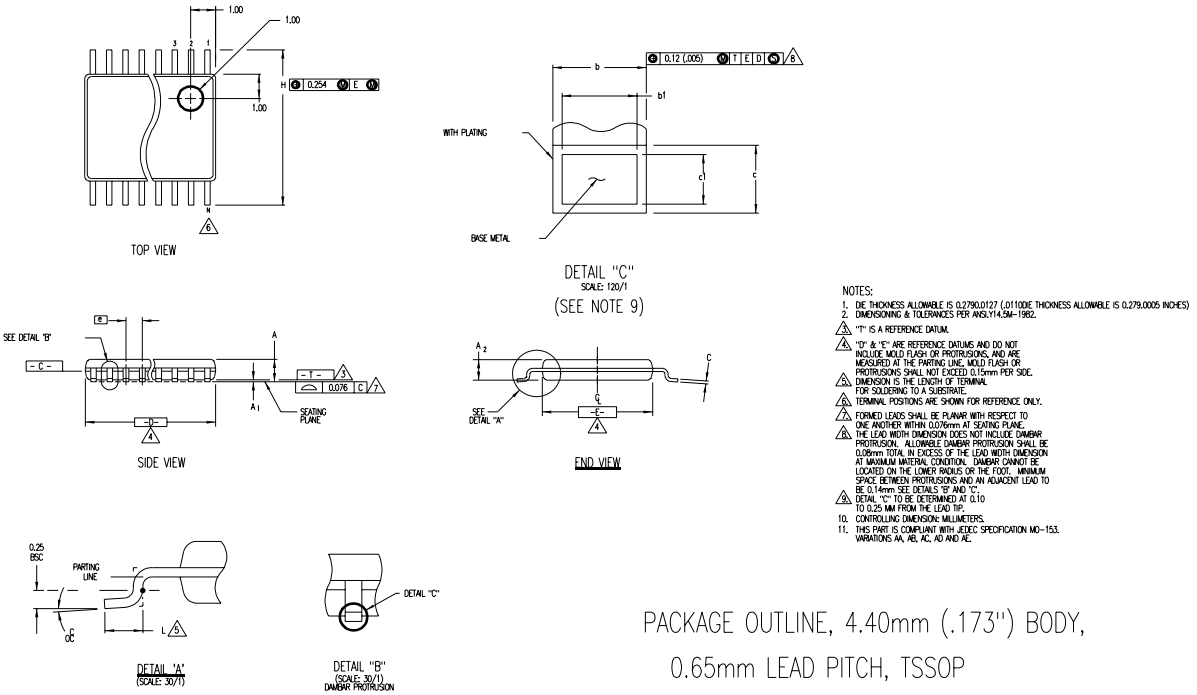
VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	.004	.006							

Package Diagram

28-Pin Thin Shrunk Small outline Package (TSSOP 173 mi)



NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.2790.0127 (.0110DIE THICKNESS ALLOWABLE IS 0.279.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M–1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm. SEE DETAILS "B" AND "C".
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO–153. VARIATIONS AA, AB, AC, AD AND AE.

PACKAGE OUTLINE, 4.40mm (.173") BODY,
0.65mm LEAD PITCH, TSSOP

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	———	———	1.10		AA	2.90	3.00	3.10	8
A_1	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A_2	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	–	0.30	8	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	–	0.20		AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
α	0	4	8						

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	———	———	.0433		AA	.114	.118	.122	8
A_1	.002	.004	.006		AB	.193	.197	.201	14
A_2	.0335	.0354	.0374		AC	.193	.197	.201	16
b	.0075	–	.0118	8	AD	.252	.256	.260	20
b1	.0075	.0087	.0098		AE	.303	.307	.311	24
c	.0035	–	.0079		AF	.378	.382	.386	28
c1	.0035	.0050	.0053						
D	SEE VARIATIONS			4					
E	.169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	.020	.024	.028	5					
N	SEE VARIATIONS			6					
α	0	4	8						

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Document Title: CY2313BNZ 13 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMS Document Number: 38-07261				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110526	02/20/02	SZV	Change from Spec number: 38-01090 to 38-07261