ADVANCE INFORMATION

CY2308A

3.3V 200-MHz Zero Delay Buffer

Features

- **10-MHz to 200-MHz operating range**
- **Multiple configurations (see "Available CY2308A Configurations" table on page 2 of this data sheet)**
- **Total Timing Budget Impact (TTBI) @ 200 MHz < 650 ps**
- **Eight low-skew outputs**
  - **Output-output skew < 200 ps**
  - **Device-device skew < 500 ps**
- **Input-output skew < 250 ps**
- **Cycle-cycle jitter < 100 ps**
- **Three-stateable outputs**
- **< 50µA shutdown current**
- **Phase-locked loop (PLL) bypass mode (see page 2)**
- **Spread Aware™**
- **16-pin TSSOP**
- **3.3V operation**
- **Industrial temperature available**

Functional Description

The CY2308A is a high-performance 200-MHz zero delay buffer designed for high-speed clock distribution. The integrated PLL is designed for low jitter and optimized for noise rejection. These parameters are critical for reference clock distribution in systems using high-performance ASICs and microprocessors. The CY2308A PLL feedback is external and is obtained at FBK.

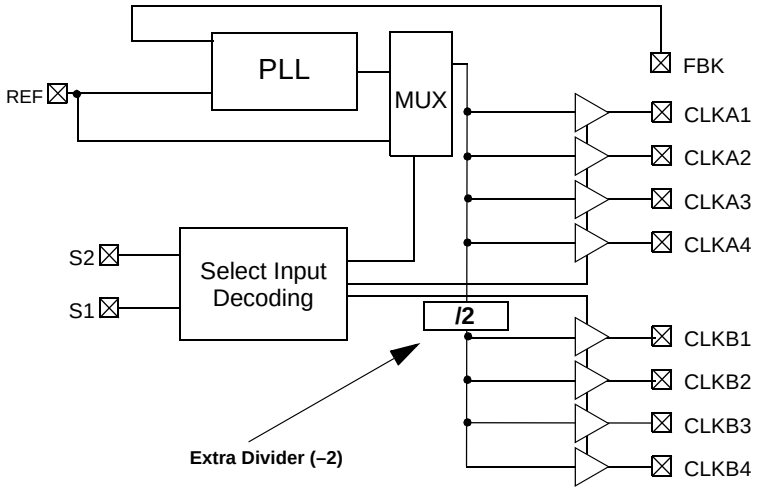
The CY2308A has two banks of four outputs each that can be controlled by the Select inputs as shown in the table "Selected Input Decoding." If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes.

The CY2308A PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 µA of current draw. The PLL shuts down in two additional cases, as shown in the "Select Input Decoding" table.

The CY2308A is available in five different configurations, as shown in the "Available CY2308A Configurations" table on page 2. CY2308A–1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The CY2308A–1H is the high-drive version of the –1, and rise and fall times on this device are much faster.

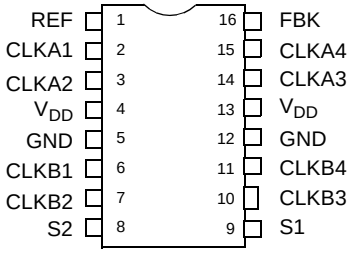
The CY2308A–2 allows the user to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives FBK.

Block Diagram



Pin Configuration

TSSOP
Top View



Select Input Decoding

S2	S1	CLOCK A1–A4	CLOCK B1–B4	Output Source	PLL Shutdown
0	0	Three-state	Three-state	PLL	Y
0	1	Driven	Three-state	PLL	N
1	0	Driven	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

Available CY2308A Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
CY2308A–1	Bank A or Bank B	Reference	Reference
CY2308A–1H	Bank A or Bank B	Reference	Reference
CY2308A–2	Bank A	Reference	Reference/2
CY2308A–2	Bank B	2 X Reference	Reference

Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V-tolerant input
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[2]	Clock output, Bank B
7	CLKB2[2]	Clock output, Bank B
8	S2[1]	Select input, bit 2, 5V-tolerant input
9	S1[1]	Select input, bit 1, 5V-tolerant input
10	CLKB3[2]	Clock output, Bank B
11	CLKB4[2]	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[2]	Clock output, Bank A
15	CLKA4[2]	Clock output, Bank A
16	FBK[1]	PLL feedback input

Notes:
1. Weak pull-ups.
2. Weak pull-downs.

Maximum Ratings

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Input Voltage (Except Ref, S1, S2)...–0.5V to V_{DD} + 0.5V

DC Input Voltage (REF, S1, S2).....–0.5 to 7V

Storage Temperature.....–65°C to +150°C

Junction Temperature .....150°C

Junction-to-Ambient Thermal Resistance

16-pin TSSOP ....113.4°C/W

Static Discharge Voltage
(per MIL-STD-883, Method 3015)..... >2000V

Operating Conditions for CY2308AZC-XX Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance (F_{OUT} < 133 MHz)		30	pF
	Load Capacitance (F_{OUT} > 133 MHz)		15	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2308AZC–XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	CMOS Levels, 30% of V_{DD}		0.3	V_{DD}
V_{IH}	Input HIGH Voltage	CMOS Levels, 70% of V_{DD}	0.7		V_{DD}
I_{IL}	Input LOW Current	V_{IN} = 0V (100k pull-up only)		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} (100k pull-up only)		10.0	µA
I_{OL}	Output LOW Current[3] (–1, –2)	V_{OL} = 0.5V	12		mA
	(–1H)		18		
I_{OH}	Output HIGH Current[3] (–1, –2)	V_{OH} = V_{DD} – 0.5V		–12	mA
	(–1H)			–18	
I_{DDS}	Power Down Supply Current	All inputs are @ 0V, excludes current through pull-downs		50	µA
I_{DD}	Supply Current	Unloaded outputs @ 200 MHz		75.0	mA
		Loaded outputs @ 200 MHz, C_L = 15 pF		140.0	

Notes:

3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY2308AZC–XX Commercial Temperature Devices[4]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
	Reference Frequency		10		200	MHz
	Reference Edge Rate	30% to 70% of V_{DD}	0.5		4	V/ns
	Reference Duty Cycle		25		75	%
t_1	Output Frequency	C_L = 30 pF	10		133	MHz
		C_L = 15 pF	10		200	
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	45.0	50.0	55.0	%
t_3	Rising Edge Rate[3] (–1, –2)	20% to 80% of V_{DD}, C_L = 30 pF	0.5		3	V/ns
		C_L= 15 pF	0.8		4	
t_3	Rising Edge Rate[3] (–1H)	20% to 80% of V_{DD}, C_L = 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
t_4	Falling Edge Rate[3] (–1, –2)	80% to 20% of V_{DD}, C_L = 30 pF	0.5		3	V/ns
		CL = 15 pF	0.8		4	
t_4	Falling Edge Rate[3] (–1H)	80% to 20% of V_{DD}, C_L = 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
TTBI	Total Timing Budget Impact, Bank A and B Same Frequency	Outputs @ 200 MHz, Tracking Skew Not Included			650	ps
	Total Timing Budget Impact, Bank A and B Different Frequency				850	
t_5	Output to Output Skew[3]	All Outputs Equally Loaded			200	ps
t_6	Input to Output Skew (Static Phase Offset)[3]	Measured at $V_{DD}/2$, REF to FBK			250	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$			500	ps
t_J	Cycle to Cycle Jitter,[3] Bank A and B Same Frequency	Loaded Outputs			200	ps
					35	ps_{RMS}
t_J	Cycle to Cycle Jitter,[3] Bank A and B Different Frequency	Loaded Outputs			400	ps
					67	ps_{RMS}
t_{tsk}	Tracking Skew	Input Reference Clock @ < 50-KHz Modulation with ±3.75% Spread			200	ps
t_{LOCK}	PLL Lock Time[3]	Stable Power Supply, Valid Clock at REF			1.0	ms

Notes:
4. All parameters are specified with loaded outputs.

Operating Conditions for CY2308AZI–XX Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance (F_{OUT} < 100 MHz)		30	pF
	Load Capacitance (F_{OUT} > 100 MHz)		15	pF
C_{IN}	Input Capacitance		7	pF

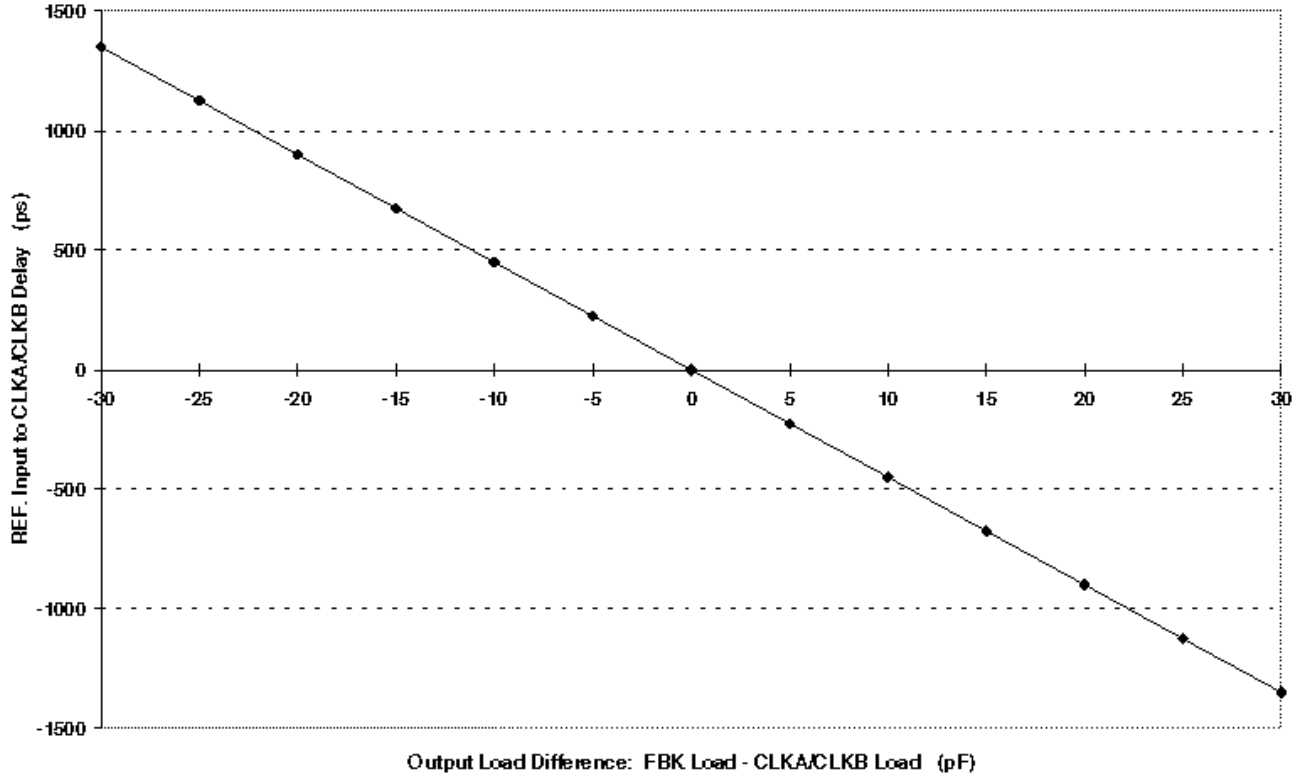
Electrical Characteristics for CY2308AZI-XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	CMOS Levels, 30% of V_{DD}		0.3	V_{DD}
V_{IH}	Input HIGH Voltage	CMOS Levels, 70% of V_{DD}	0.7		V_{DD}
I_{IL}	Input LOW Current	V_{IN} = 0V (100k pull-ups only)		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} (100k pull-ups only)		10.0	µA
I_{OL}	Output LOW Current[3] (–1, –2)	V_{OL} = 0.5V	12		mA
	(–1H)		18		
I_{OH}	Output HIGH Current[3] (–1, –2)	V_{OH} = V_{DD} – 0.5V		–12	mA
	(–1H)			–18	
I_{DDS}	Power Down Supply Current	All inputs are @ 0V, excludes current through pull-downs		50	µA
I_{DD}	Supply Current	Unloaded outputs @ 166 MHz		60.0	mA
		Loaded outputs @ 166 MHz, C_L = 15 pF		120.0	

Switching Characteristics for CY2308AZI–XX Industrial Temperature Devices [4]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
	Reference Frequency		10		170	MHz
	Reference Edge Rate	30% to 70% of V_{DD}	0.5		4	V/ns
	Reference Duty Cycle		25		75	%
t_1	Output Frequency	C_L = 30 pF	10		100	MHz
		C_L = 15 pF	10		170	
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40.0	50.0	60.0	%
t_3	Rising Edge Rate[3] (–1, –2)	20% to 80% of V_{DD}, C_L = 30 pF	0.5		3	V/ns
		C_L= 15 pF	0.8		4	
t_3	Rising Edge Rate[3] (–1H)	20% to 80% of V_{DD}, C_L = 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
t_4	Falling Edge Rate[3] (–1, –2)	80% to 20% of V_{DD}, C_L = 30 pF	0.5		3	V/ns
		CL = 15 pF	0.8		4	
t_4	Falling Edge Rate[3] (–1H)	80% to 20% of V_{DD}, C_L = 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
TTBI	Total Timing Budget Impact, Bank A and B Same Frequency	Outputs @ 166 MHz, Tracking Skew Not Included			650	ps
	Total Timing Budget Impact, Bank A and B Different Frequency				850	
t_5	Output to Output Skew[3]	All Outputs Equally Loaded			200	ps
t_6	Input to Output Skew (static phase offset)[3]	Measured at $V_{DD}/2$, REF to FBK			250	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$			500	ps
t_J	Cycle to Cycle Jitter[3], Bank A and B Same Frequency	Loaded Outputs			200	ps
					35	ps_{RMS}
t_J	Cycle to Cycle Jitter[3], Bank A and B Different Frequency	Loaded Outputs			400	ps
					67	ps_{RMS}
t_{tsk}	Tracking Skew	Input Reference Clock @ < 50-KHz Modulation with ±3.75% Spread			200	ps
t_{LOCK}	PLL Lock Time[3]	Stable Power Supply, Valid Clock at REF			1.0	ms

REF. Input to CLKA/CLKB Delay vs. Difference in Loading Between FBK Pin and CLKA/CLKB Pins

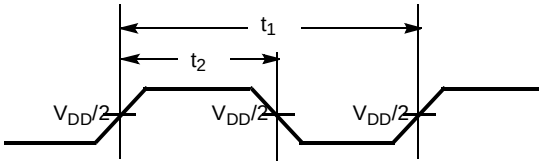


Zero Delay and Skew Control

To close the feedback loop of the CY2308A, FBK can be driven from any of the eight available output pins. The output driving FBK will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. See *REF Input to CLK Delay vs. Loading Difference*. For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally. For further information on using CY2308A, refer to the application note “CY2308: Zero Delay Buffer.”

Duty Cycle Timing

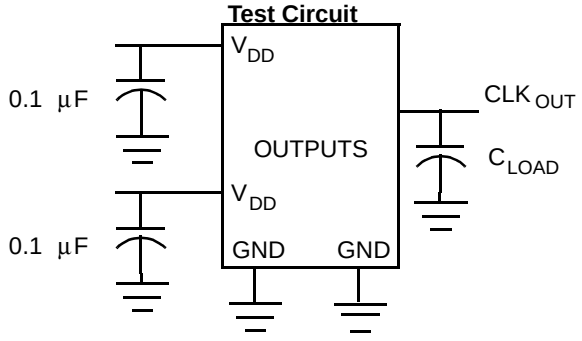


Typical Duty Cycle and I_{DD} Trends

<Add the following graphs later...>

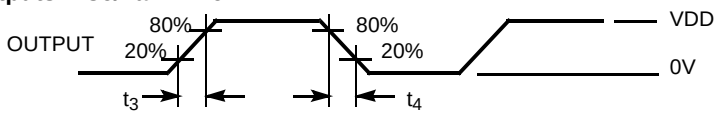
- Duty cycle vs. V_{DD} (conditions: 30 pF or 15 pF load, 25°, Freq = 33 MHz, 66 MHz, 133 MHz, 166 MHz, 200 MHz)
- Duty cycle vs. Freq. (conditions: 30 pF or 15 pF load, V_{DD} = 3.3V, –40 to 85°, Freq = 33 MHz, 66 MHz, 133 MHz, 166 MHz, 200 MHz)
- I_{DD} vs. number of outputs loaded (conditions: 30 pF or 15 pF load, 3.3V, 25°, Freq = 33 MHz, 66 MHz, 133 MHz, 166 MHz, 200 MHz)

Test Circuits

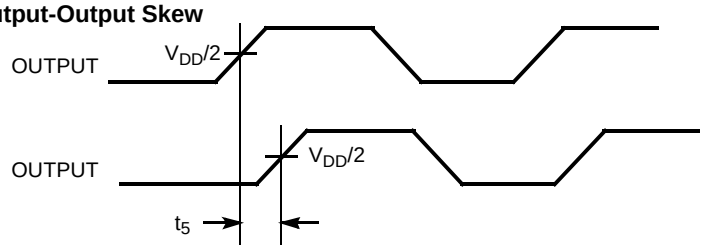


Switching Waveforms

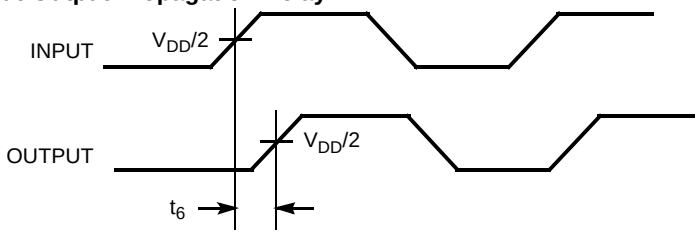
All Outputs Rise/Fall Time



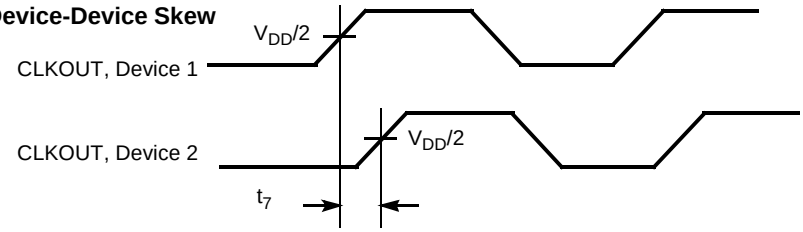
Output-Output Skew



Input-Output Propagation Delay



Device-Device Skew

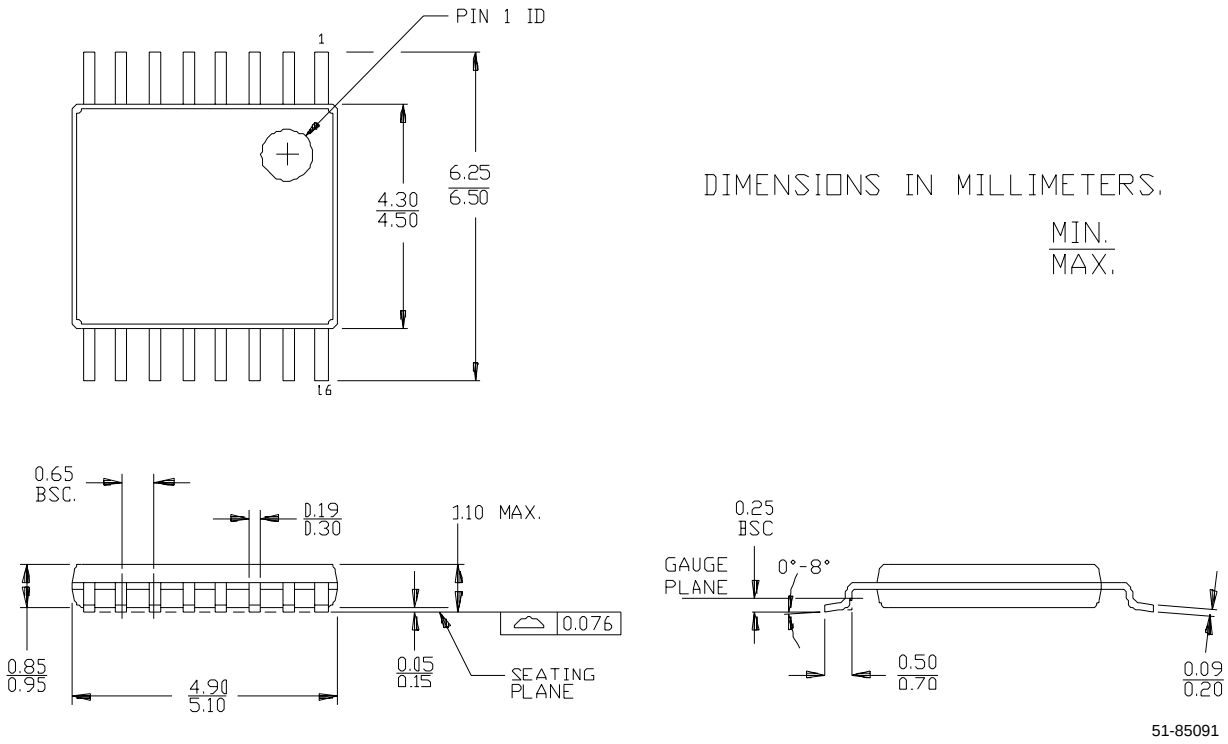


Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2308AZC-1	Z16	16-pin 4.4-mm TSSOP	Commercial
CY2308AZI-1	Z16	16-pin 4.4-mm TSSOP	Industrial
CY2308AZC–1H	Z16	16-pin 4.4-mm TSSOP	Commercial
CY2308AZI–1H	Z16	16-pin 4.4-mm TSSOP	Industrial
CY2308AZC–2	Z16	16-pin 4.4-mm TSSOP	Commercial
CY2308AZI–2	Z16	16-pin 4.4-mm TSSOP	Industrial

Package Diagram

16-pin Thin Shrunk Small Outline Package (4.40-mm Body) Z16



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