ADVANCE INFORMATION

CY2305A

3.3V 200-MHz Zero Delay Buffer

Features

- **10-MHz to 200-MHz operating range**
- **Total Timing Budget Impact (TTBI) @ 200 MHz < 650 ps**
- **Five low-skew outputs**
  - **Output-output skew < 200 ps**
  - **Device-device skew < 500 ps**
- **Input-output skew < 250 ps**
- **Cycle-cycle jitter < 100 ps**
- **< 50μA shutdown current**
- **Spread Aware™**
- **8-pin SOIC**
- **3.3V operation**
- **Industrial temperature available**

Functional Description

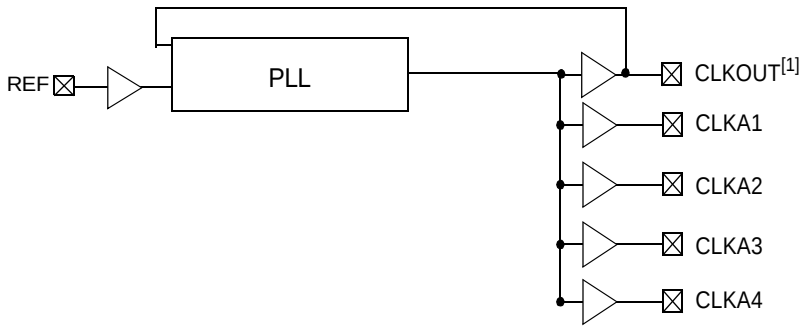
The CY2305A is a high-performance 200MHz zero delay buffer designed for high-speed clock distribution. The integrated PLL is designed for low jitter and optimized for noise rejection. These parameters are critical for reference clock distribution in systems using high-performance ASIC's and microprocessors. The phase-locked loop (PLL) feedback is internal and is obtained from CLKOUT.

The CY2305A accepts a reference clock input, and drives out five low-skew clocks.

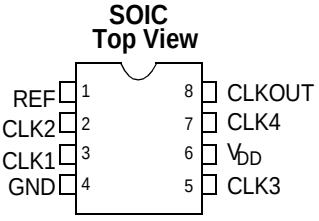
The CY2305A PLL enters power-down when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 50μA of supply current.

The CY2305A is available in standard (-1) or high-drive (-1H) output versions. The high-drive features faster rise and fall times.

Block Diagram



Pin Configuration



Note:

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Pin Description

Pin	Signal	Description
1	REF[2]	Input reference frequency, 5V-tolerant input
2	CLK2[3]	Buffered clock output
3	CLK1[3]	Buffered clock output
4	GND	Ground
5	CLK3[3]	Buffered clock output
6	V_{DD}	3.3V supply
7	CLK4[3]	Buffered clock output
8	CLKOUT[3]	Buffered clock output, internal feedback on this pin

Notes:
2. Weak pull-ups.
3. Weak pull-downs.

Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage (Except REF) .....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF ..... –0.5V to 7V

Storage Temperature .....–65°C to +150°C

Junction Temperature ..... 150°C

Junction-to-Ambient Thermal Resistance

8-pin SOIC..... 138.66°C/W

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .....> 2,000V

Operating Conditions for CY2305ASC–XX Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance (F_{OUT} < 133 MHz)		30	pF
	Load Capacitance (F_{OUT} > 133 MHz)		15	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2305ASC–XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	CMOS Levels, 30% of V_{DD}		0.3	V_{DD}
V_{IH}	Input HIGH Voltage	CMOS Levels, 70% of V_{DD}	0.7		V_{DD}
I_{IL}	Input LOW Current	V_{IN} = 0V (100k pull-up only)		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} (100k pull-up only)		10.0	µA
I_{OL}	Output LOW Current,[4] (–1)	V_{OL} = 0.5V	12		mA
	(–1H)		18		
I_{OH}	Output HIGH Current,[4] (–1)	V_{OH} = V_{DD} – 0.5V		–12	mA
	(–1H)			–18	
I_{DDS}	Power Down Supply Current	All inputs are @ 0V, excludes current through pull-downs		50	µA
I_{DD}	Supply Current	Unloaded outputs @ 200 MHz		45	mA
		Loaded outputs @ 200 MHz C_L = 15 pF		85	

Switching Characteristics for CY2305ASC–XX Commercial Temperature Devices [5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
	Reference Frequency		10		200	MHz
	Reference Edge Rate	30% to 70% of V_{DD}	0.5		4	V/ns
	Reference Duty Cycle		25		75	%
t_1	Output Frequency	30 pF Load	10		133	MHz
		15 pF Load	10		200	
	Duty Cycle[4] = $t_2 \div t_1$	Measured at V_{DD}/2	45.0	50.0	55.0	%
t_3	Rising Edge Rate,[4] (–1)	20% to 80% of V_{DD}, C_L= 30 pF	0.5		3	V/ns
		C_L= 15 pF	0.8		4	
t_3	Rising Edge Rate,[4] (–1H)	20% to 80% of V_{DD}, C_L= 30 pF	TBD		TBD	V/ns
		C_L= 15 pF	TBD		TBD	
t_4	Falling Edge Rate,[4] (–1)	80% to 20% of V_{DD}, C_L= 30 pF	0.5		3	V/ns
		C_L= 15 pF	0.8		4	

Notes:

4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. All parameters specified with loaded outputs.

Switching Characteristics for CY2305ASC–XX Commercial Temperature Devices (continued)[5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_4	Falling Edge Rate,[4] (–1H)	80% to 20% of V_{DD}, C_L= 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
TTBI	Total Timing Budget Impact	Outputs @ 200 MHz, Tracking Skew Not Included			650	ps
t_5	Output to Output Skew[4]	All Outputs Equally Loaded			200	ps
t_6	Input to Output Skew (Static phase offset)[4]	Measured at V_{DD}/2, REF to CLKOUT			250	ps
t_7	Device to Device Skew[4]	Measured at V_{DD}/2			500	ps
t_J	Cycle to Cycle Jitter[4]	Loaded Outputs			200	ps
					35	ps_{RMS}
t_{tsk}	Tracking Skew	Input Reference Clock @ < 50-KHz Modulation with ±3.75% Spread			200	ps
t_{LOCK}	PLL Lock Time[4]	Stable Power Supply, Valid Clock at REF			1.0	ms

Operating Conditions for CY2305ASI–XX Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance (F_{OUT} < 100 MHz)		30	pF
	Load Capacitance (F_{OUT} > 100 MHz)		15	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2305ASI–XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	CMOS Levels, 30% of V_{DD}		0.3	V_{DD}
V_{IH}	Input HIGH Voltage	CMOS Levels, 70% of V_{DD}	0.7		V_{DD}
I_{IL}	Input LOW Current	V_{IN} = 0V (100K Pull-up Only)		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} (100K Pull-up Only)		10.0	µA
I_{OL}	Output LOW Current,[4] (–1)	V_{OL} = 0.5V	12		mA
	(–1H)		18		
I_{OH}	Output HIGH Current,[4] (–1)	V_{OH} = V_{DD} – 0.5V		–12	mA
	(–1H)			–18	
I_{DDS}	Power Down Supply Current	All inputs are @ 0V, excludes current through pull-downs		50	µA
I_{DD}	Supply Current	Unloaded outputs @ 166 MHz		40	mA
		Loaded outputs @ 166 MHz, C_L = 15 pF		70	

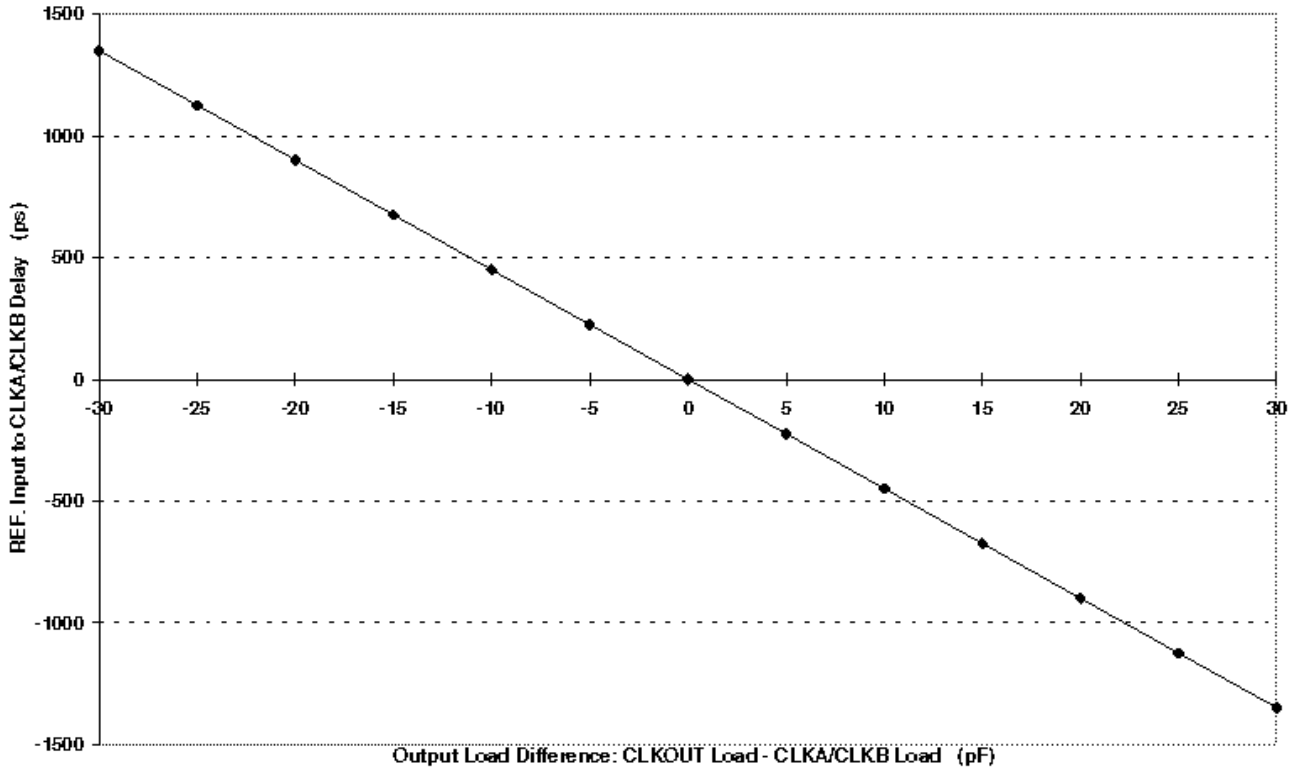
Switching Characteristics for CY2305ASI–1 Industrial Temperature Devices [5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
	Reference Frequency		10		170	MHz
	Reference Edge Rate	30% to 70% of V_{DD}	0.5		4	V/ns

Switching Characteristics for CY2305ASI–1 Industrial Temperature Devices (continued)[5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
	Reference Duty Cycle		25		75	%
t_1	Output Frequency	30 pF Load	10		100	MHz
		15 pF Load	10		170	
	Duty Cycle[4] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40.0	50.0	60.0	%
t_3	Rising Edge Rate,[4] (-1)	20% to 80% of V_{DD}, C_L = 30 pF	0.5		3	V/ns
		C_L = 15 pF	0.8		4	
t_3	Rising Edge Rate,[4] (-1H)	20% to 80% of V_{DD}, C_L = 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
t_4	Falling Edge Rate,[4] (-1)	80% to 20% of V_{DD}, C_L = 30 pF	0.5		3	V/ns
		C_L = 15 pF	0.8		4	
t_4	Falling Edge Rate,[4] (-1H)	80% to 20% of V_{DD}, C_L = 30 pF	TBD		TBD	V/ns
		C_L = 15 pF	TBD		TBD	
TTBI	Total Timing Budget Impact	Outputs @ 166 MHz, Includes Skew and Jitter. Tracking Skew Not Included			650	ps
t_5	Output to Output Skew[4]	All Outputs Equally Loaded			200	ps
t_6	Input to Output Skew (static phase offset)[4]	Measured at $V_{DD}/2$, REF to CLKOUT			250	ps
t_7	Device to Device Skew[4]	Measured at $V_{DD}/2$			500	ps
t_J	Cycle to Cycle Jitter[4]	Loaded Outputs			200	ps
					35	ps_{RMS}
t_{tsk}	Tracking Skew	Input Reference Clock @ < 50KHz Modulation with ±3.75% Spread			200	ps
t_{LOCK}	PLL Lock Time[4]	Stable Power Supply, Valid Clock at REF			1.0	ms

REF. Input to CLK1-CLK4 Delay vs. Loading Difference Between CLKOUT and CLK1-CLK4



Zero Delay and Skew Control

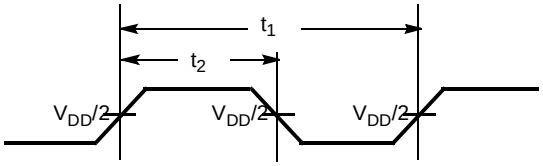
All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT is the internal feedback to the PLL, its relative loading can adjust the input-output delay. See *REF input to CLK Delay vs. Loading Difference*.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT and other outputs.

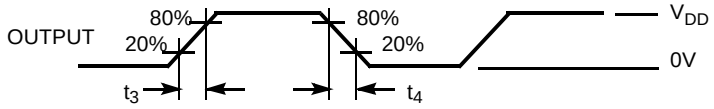
For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note "CY2305 as PCI and SDRAM Buffers."

Switching Waveforms

Duty Cycle Timing

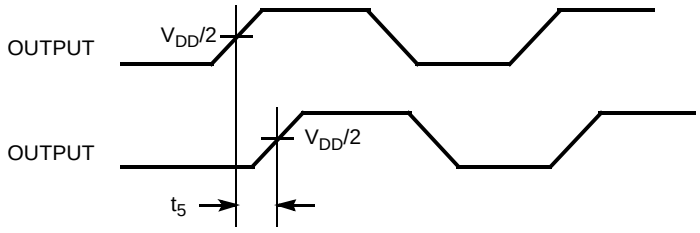


All Outputs Rise/Fall Time

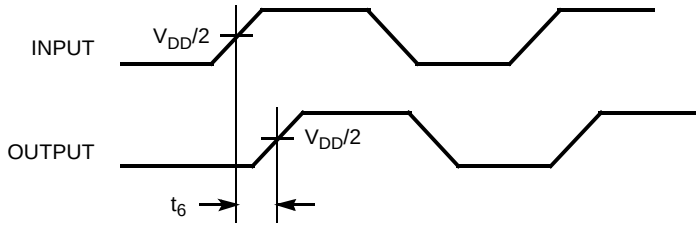


Switching Waveforms (continued)

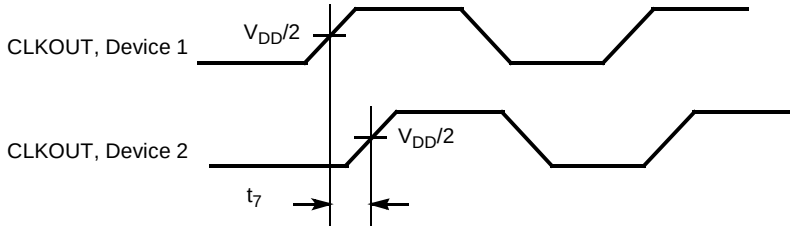
Output-Output Skew



Input-Output Propagation Delay



Device-Device Skew

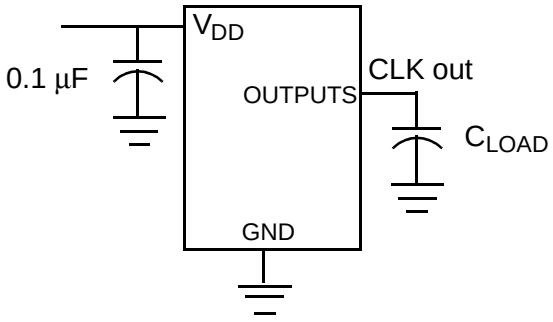


Typical Duty Cycle and IDD Trends

<Add the following graphs later...>

- Duty cycle vs. V_{DD} (conditioned: 30 pF or 15 pF load, 25°, Freq = 33 MHz, 66 MHz, 133 MHz, 166 MHz, 200 MHz)
- Duty cycle vs. Freq. (conditioned: 30 pF or 15 pF load, V_{DD} = 3.3V, –40 to +85°, Freq = 33 MHz, 66 MHz, 133 MHz, 166 MHz, 200 MHz)
- I_{DD} vs. number of outputs loaded (conditioned: 30 pF or 15 pF load, 3.3V, 25°, Freq = 33 MHz, 66 MHz, 133 MHz, 166 MHz, 200 MHz).

Test Circuit

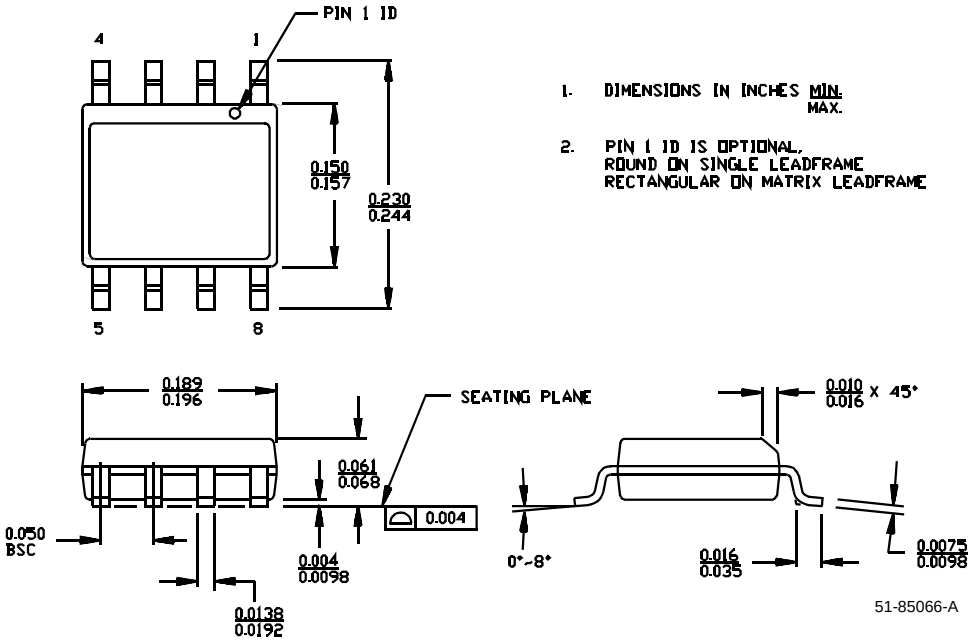


Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2305ASC-1	S8	8-pin 150-mil SOIC	Commercial
CY2305ASI-1	S8	8-pin 150-mil SOIC	Industrial
CY2305ASC-1H	S8	8-pin 150-mil SOIC	Commercial
CY2305ASI-1H	S8	8-pin 150-mil SOIC	Industrial

Package Diagram

8-lead (150-mil) SOIC S8



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**	112941	03/29/02	CTK	New Data Sheet