PRELIMINARY

CY23020-1

Twenty Output Zero Delay Buffer

Features

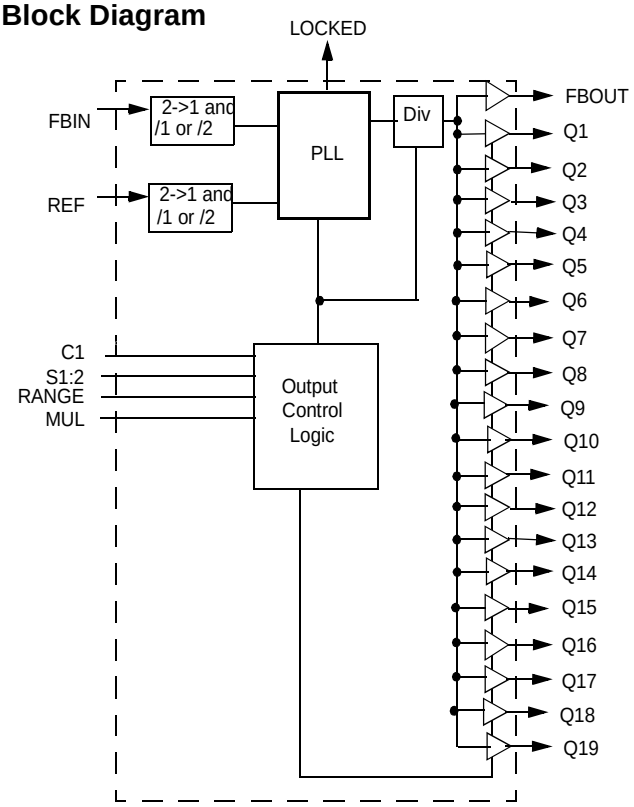
- **335 ps Total timing budget impact (TTBI)**
- **Spread Aware™—designed to work with SSFTG reference signals**
- **Outputs may be selected to be equal to the input frequency x1,or x2**
- **LVTTL/LVCMOS inputs/outputs to 200 MHz**
- **3.3V core power supply**
- **2.5V or 3.3V output signals**
- **Available in 48-pin TSSOP and QFN packages (contact factory for package availability)**

Overview

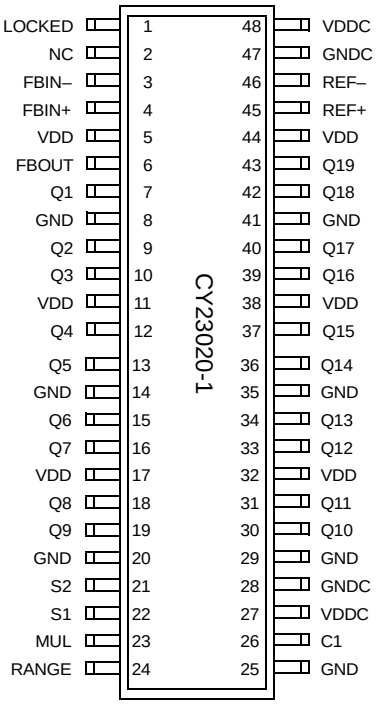
The CY23020-1 is a PLL-based clock driver designed to provide high performance. The clock driver provides output frequencies of up to 200 MHz.

The most prominent feature is the skew, jitter, and total timing budget impact performance that exceeds most previous Zero Delay Buffer (ZDB) products.

Block Diagram



Pin Configurations



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
REF+ REF-	45 46	I	***Reference Inputs:*** Output signals are synchronized to the crossing point of REF+ and REF– signals. Therefore REF- must be tied to VREF as defined in the DC characteristics table. For optimal performance, the impedances seen by these two inputs must be equal.
FBIN+ FBIN-	4 3	I	***Feedback Inputs:*** Input FBIN+ must be fed by one of the outputs to ensure proper functionality. If the trace between FBIN+ and FBOUT is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the clock signal at REF+ input. FBIN– must be tied to VREF as defined in the DC characteristics table. For best performance, the impedances seen by these two inputs must be equal.
FBOUT	6	O	***Feedback Output:*** In order to complete the phase locked loop, an output must be connected back to the FBIN+ pin. Any of the outputs may actually be used as the feedback source.
Q1:19	7, 9, 10, 12, 13, 15, 16, 18, 19, 30, 31, 33, 34, 36, 37, 39, 40, 42, 43	O	***Outputs:*** Refer to *Tables 1–4* for the characteristics of these outputs.
RANGE	24	I	***Frequency Range Selection Input:*** To determine the correct connection for this pin, refer to *Table* 2. This should be a static input
LOCKED	1	O	***PLL Locked Output:*** When this output is HIGH, the PLL in the CY23020-1 is in steady state operation mode (Locked). When this signal is LOW, the PLL is in the process of locking onto the reference signal.
S1:2	22, 21	I	***Output/PLL Enable Selection bits:*** To determine appropriate settings, refer to *Table 1*.
VDDC	27, 48	P	***Analog Power Connection:*** Connect to 3.3V.
GNDC	28, 47	G	***Analog Ground Connection:*** Connect to common system ground plane.
VDD	5, 11, 17, 32, 38, 44	P	***Output Buffer Power Connections:*** Connect to 2.5 or 3.3V, whichever is to be the reference for the output signals.
GND	8, 14, 20, 25, 29, 35, 41	G	***Ground Connections:*** Connect to common system ground plane.
MUL	23	I	***Multiplication factor select:*** When set HIGH, the outputs will run at twice the speed of the reference signal. This should be a static input
C1	26	I	***Output Configuration bit:*** Establishes either 2.5V or 3.3V Full Swing Operation. To determine appropriate setting, refer to *Table* 3. This should be a static input
NC	2	NC	***Do Not Connect:*** This pin must be left floating. This pin is used by the factory for testing purposes.

Notes:
1. Note A: Inputs *Range,Mul,and C1* are static inputs.
2. Note B:Default pull down resistors (~100kohm) are present on Range, Mul, and C1 inputs.

Table 1. Output Configuration

S1	S2	Qx source	PLL
0	0	Three-state	Shutdown
0	1	Reserved	
1	0	Reference Input	Shutdown
1	1	PLL Output	Active

Table 2. Frequency Range Setting

RANGE	Output Frequency Range
0	50–100 MHz
1	100–200 MHz

Table 3. Output Configuration Setting

C1	Output Type
0	3.3 V Full swing
1	2.5 V Full swing

Table 4. Frequency Multiplication table

MUL	Output Frequency
0	$F_{OUT} = F_{REF}$
1	$F_{OUT} = F_{REF} \times 2$

Spread Aware™

Many systems are designed to utilize Spread Spectrum Modulation clock technology. This technology is used to dramatically reduce Electro Magnetic Interference (EMI) in digital systems. Cypress has pioneered SSFTG development, and this product is designed to pass any SSFTG modulation that is present on the REF+ pin to its output clock signals. This capability also enhances the part to produce clocks with significantly smaller jitter and tracking skew on its output clocks. This is especially beneficial in systems that have downstream PLLs present.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

How to Implement Zero Delay

Typically, ZDBs multiply (fan-out) single clock signals quantity while simultaneously reducing or mitigating the time delay associated with passing the clock through a buffering device. In many cases the output clock is adjusted, in phase, to occur later or more often before the device’s input clock to compensate for a design’s physical delay inadequacies. Most commonly this is done using a simple PCB trace as a time delay element. The longer the trace the earlier the output clock edges occur with respect to the reference input clock edges.

In this way such effects as undesired transit time of a clock signal across a PCB can be compensated for.

Inserting Other Devices in Feedback Path

Due to the fact that the device has an external feedback path the user has a wide range of control over its output to input skewing effect. One of these is to be able to synchronize the outputs of an external clock that is resultant from any of the output clocks. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) that is put into the feedback path.

Referring to *Figure 1*, if the traces between the ASIC/buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin (B), the signals at the destination(s) device (C) will be driven high at the same time the Reference clock provided to the ZDB goes high. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay in the ASIC/Buffer must be accounted for.

There are constraints when inserting other devices. If the devices contain Phase Locked Loops (PLL’s) or excessively long delay times they can easily cause the overall clocking system to become unstable as the components interact. For these designs it is advisable to contact Cypress for applications support.

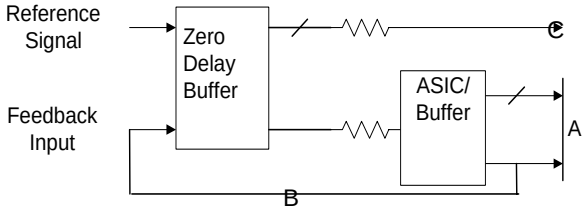


Figure 1. Output Buffer in the Feedback Path

Component Characterization Set-Up

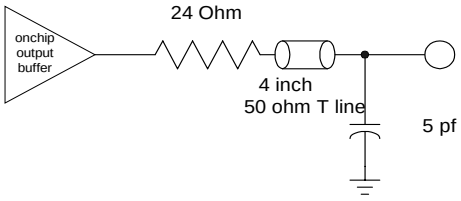


Figure 2. Termination Networks

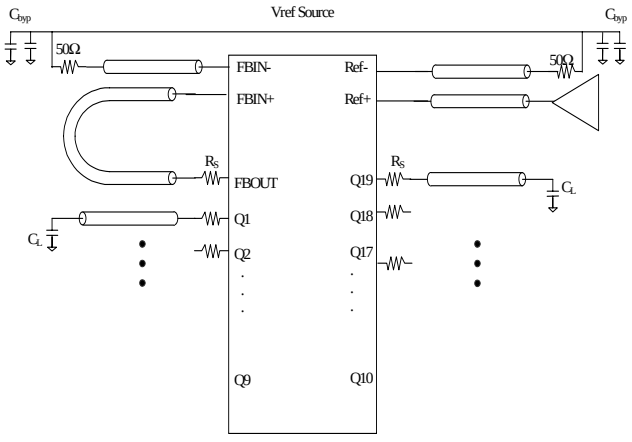


Figure 3. Establishing Reference Voltages

The CY23020-1 uses a differential input receiver to increase it's rejection of common mode input noise and thus increase device performance. To ensure that any noise appears equally on both the Ref- and Ref+ pins, it is necessary to match the external impedance and circuitry seen at these pins. Figure 3 shows how this may be accomplished. The reference voltage, V_{REF} can be generated by a resistor divider from a power supply. This potential will adjust the FBIN+ input's triggering threshold. The reference voltage should be well bypassed so as to not introduce any single ended noise to the device. Note that the impedance (50 ohms) is also matched to the FBIN+ line. The 50 ohm resistor is used to create a "like" load on the REF- input clock signal and matches the 50 ohm source impedance of the REF+ input signal. If the input impedance is significantly different than 50 ohms, the reference resistor should be adjusted accordingly.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}	Voltage on any VDD pin with respect to GND	-0.5 to +5.0	V
V_{IN}	Voltage on any input pin with respect to GND	-0.5 to V_{DD}+0.5	V
T_{STG}	Storage Temperature	-65 to +150	^{O}C
T_A	Operation Temperature	0 to +70	^{O}C
T_J	Junction Temperature	+150 max.	^{O}C
P_D	Package Power Dissipation (TSSOP)	1	W
P_D	Package Power Dissipation (QFN)	TBD	W

Full Swing DC Electrical Characteristics
TA = 0 to70°C, V_{DDC} = 3.3 ±5%, V_{DD} = 2.5 ±5%, or 3.3 ±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	REF+, FBIN+ Inputs only		2.0			V
V_{IL}	REF+, FBIN+ Inputs only				0.8	V
V_{IH}	Logic Inputs only		0.7xV_{DD}			V
V_{IL}	Logic Inputs only				0.3xV_{DD}	V
I_{PD}	Power Down current	PLL disable mode, S0:S1=0			100	µA
T_{VDD}	Supply Voltage Ramp Rate		TBD			V/ms
C_{IN}	Input Capacitance			5		pF

2.5V Full Swing DC Electrical Characteristics
TA = 0 to 70°C, V_{DDC} = 3.3 ±5%, V_{DD} = 2.5 ±5%, 1.19V < V_{REF} < 1.50V

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Unloaded, 200 MHz			180	mA
I_{IH}	Input Current in HIGH state	V_{IN}= V_{DD}			100	µA
I_{IL}	Input Current in LOW state	V_{IN}= 0			10	µA
I_{OH}	Output current in HIGH state	Measured at pin, no load network, V_{OH} = VDD-0.35 V			-14	mA
I_{OL}	Output current in LOW state	Measured at pin, no load network, V_{OL} =0.35 V	14			mA

2.5V Full Swing AC Electrical Characteristics
TA = 0 to70°C, V_{DDC} = 3.3 ±5%, V_{DD} = 2.5 ±5%, 1.19 V < V_{REF} < 1.50V, Load: (see *Figure 2*, CL = 5pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
F_{IN}	Input Frequency		50		200[2]	MHz
F_{OUT}	Output Frequency		50		200[2]	MHz

2.5V Full Swing AC Electrical Characteristics
TA = 0 to70°C, V_{DDC} = 3.3 ±5%, V_{DD} = 2.5 ±5%, 1.19 V < V_{REF} < 1.50V, Load: (see *Figure 2*, CL = 5pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
T_{ISR}	Input Slew Rate (+ or -)	Measured between 20% and 80% of input swing	1		6.5	V/ns
T_R	Output Rise Rate	Measured between 20% and 80% of output swing	1		6.5	V/ns
T_F	Output Fall Rate	Measured between 80% and 20% of output swing	1		6.5	V/ns
T_{IDC}	Input Duty Cycle	Tested at 50% swing	40		60	%
T_D	Output Duty Cycle	Measured at VDD/2	45		55	%
T_{PD}	REF - FBIN skew	$F_{out} = F_{ref}$	-175		175	ps
T_{PD2}	REF - FBIN skew	$F_{out} = F_{ref}x2$	-225		225	ps
T_{SK}	Output-Output Skew	Outputs are equally loaded			95	ps
T_{TBI}	Total Timing Budget Impact	REF to any output[1], $F_{out} = F_{ref}$			335	ps
T_{TBI2}	Total Timing Budget Impact	REF to any output[1], $F_{out} = F_{ref}x2$			450	ps
T_{JC}	Peak Cycle to Cycle Jitter (1000 cycles max)	All outputs active, $F_{out} = F_{ref}$			80	ps
T_{JC_RMS}	RMS Cycle to Cycle Jitter	All outputs active, $F_{out} = F_{ref}$			15	ps
T_{JP}	Period Jitter p-p	All outputs active, $F_{out} = F_{ref}$			80	ps
T_{JP_RMS}	RMS Period Jitter	All outputs active, $F_{out} = F_{ref}$			15	ps
T_{JL}	Long Term Jitter p-p	All outputs active, $F_{out} = F_{ref}$			130	ps
T_{JLRMS}	RMS Long Term Jitter	All outputs active, $F_{out} = F_{ref}$			20	ps
T_{JC2}	Peak Cycle to Cycle Jitter (1000 cycles max)	All outputs active, $F_{out} = F_{ref}x2$			130	ps
T_{JCRMS2}	RMS Cycle to Cycle Jitter	All outputs active, $F_{out} = F_{ref}x2$			50	ps
T_{JP2}	Period Jitter p-p	All outputs active, $F_{out} = F_{ref}x2$			130	ps
T_{JPRMS2}	RMS Period Jitter	All outputs active, $F_{out} = F_{ref}x2$			50	ps
T_{JL2}	Long Term Jitter p-p	All outputs active, $F_{out} = F_{ref}x2$			160	ps
T_{JLRMS2}	RMS Long Term Jitter	All outputs active, $F_{out} = F_{ref}x2$			50	ps
T_{lock}	Power-Up Lock Time				1	ms
T_{PWD}	Power Down time				1	ms
T_{TSK}	Spread Spectrum Tracking Skew				100	ps
PSRR	Power Supply Rejection Ratio	Fsupply 1 KHz-10 MHz		300		ps/V

3.3V, Full Swing DC Electrical Characteristics
TA = 0 to70°C, V_{DDC} = 3.3V ±5%, V_{DD} = 3.3V ±5%, 0.42 * V_{DD} < V_{REF} < 0.50 * V_{DD}

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply current	Unloaded, 200Mhz			200	mA
I_{IH}	Input Current in high state	Vin=V_{DD}			100	µA
I_{IL}	Input Current in low state	Vin=0			10	µA

3.3V, Full Swing DC Electrical Characteristics
TA = 0 to70°C, V_{DDC} = 3.3V ±5%, V_{DD} = 3.3V ±5%, 0.42 * V_{DD} < V_{REF} < 0.50 * V_{DD}

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{OH}	Output current in high state	measured at pin, no load network, Voh=2.4V			- 18	mA
I_{OL}	Output current in low state	measured at pin, no load network, Vol=0.4V	14			mA

3.3V, Full Swing AC Electrical Characteristics:
TA = 0 to70°C, V_{DDC} = 3.3V ±5%, V_{DD} = 3.3V ±5%, 0.42 * V_{DD} < V_{REF} < 0.50 * V_{DD}, Load: (see *Figure 2*, CL= 5pF),

Parameter	Description	Test Condition	Min	Typ	Max	Unit
F_{IN}	Input Frequency		50		200[2]	MHz
F_{OUT}	Output Frequency		50		200[2]	MHz
T_{ISR}	Input Slew Rate (+ or -)	Measured between 20% and 80% of input swing	1		6.5	v/ns
T_R	Output Rise Rate	Measured between 20% and 80% of output swing	1		6.5	V/ns
T_F	Output Fall Rate	Measured between 80% and 20% of output swing	1		6.5	V/ns
T_{IDC}	Input Duty Cycle	Tested at 50% swing	40		60	%
T_D	Output Duty Cycle	Measured at V_{DD}/2	45		55	%
T_{PD}	REF - FBIN skew	$F_{out} = F_{ref}$	-175		175	ps
T_{PD2}	REF - FBIN skew	$F_{out} = F_{ref}$x2	-225		225	ps
T_{SK}	Output-Output Skew				95	ps
T_{TBI}	Total Timing Budget Impact	Refin to any output[1],$F_{out} = F_{ref}$			335	ps
T_{TBI2}	Total Timing Budget Impact	Refin to any output[1],$F_{out} = F_{ref}$x2			450	ps
T_{JC}	Peak Cycle to Cycle Jitter (1000 cycles max)	All outputs active, $F_{out} = F_{ref}$			80	ps
T_{JC_RMS}	RMS Cycle to Cycle Jitter	All outputs active, $F_{out} = F_{ref}$			15	ps
T_{JP}	Period Jitter p-p	All outputs active, $F_{out} = F_{ref}$			80	ps
T_{JP_RMS}	RMS Period Jitter	All outputs active, $F_{out} = F_{ref}$			15	ps
T_{JL}	Long Term Jitter p-p	All outputs active, $F_{out} = F_{ref}$			130	ps
T_{JLRMS}	RMS Long Term Jitter	All outputs active, $F_{out} = F_{ref}$			20	ps
T_{JC2}	Peak Cycle to Cycle Jitter (1000 cycles max)	All outputs active, $F_{out} = F_{ref}$x2			130	ps
T_{JCRMS2}	RMS Cycle to Cycle Jitter	All outputs active, $F_{out} = F_{ref}$x2			50	ps
T_{JP2}	Period Jitter p-p	All outputs active, $F_{out} = F_{ref}$x2			130	ps
T_{JPRMS2}	RMS Period Jitter	All outputs active, $F_{out} = F_{ref}$x2			50	ps
T_{JL2}	Long Term Jitter p-p	All outputs active, $F_{out} = F_{ref}$x2			160	ps
T_{JLRMS2}	RMS Long Term Jitter	All outputs active, $F_{out} = F_{ref}$x2			50	ps
T_{lock}	Power up lock time				1	ms
T_{PWD}	Power Down time				1	ms
T_{TSK}	Spread Spectrum Tracking skew				100	ps

3.3V, Full Swing AC Electrical Characteristics:
TA = 0 to70°C, V_{DDC} = 3.3V ±5%, V_{DD} = 3.3V ±5%, 0.42 * V_{DD} < V_{REF} < 0.50 * V_{DD}, Load: (see *Figure 2*, CL= 5pF),

Parameter	Description	Test Condition	Min	Typ	Max	Unit
PSRR	Power Supply Rejection Ratio	Fsupply 1KHz-10Mhz		300		ps/v

Notes:

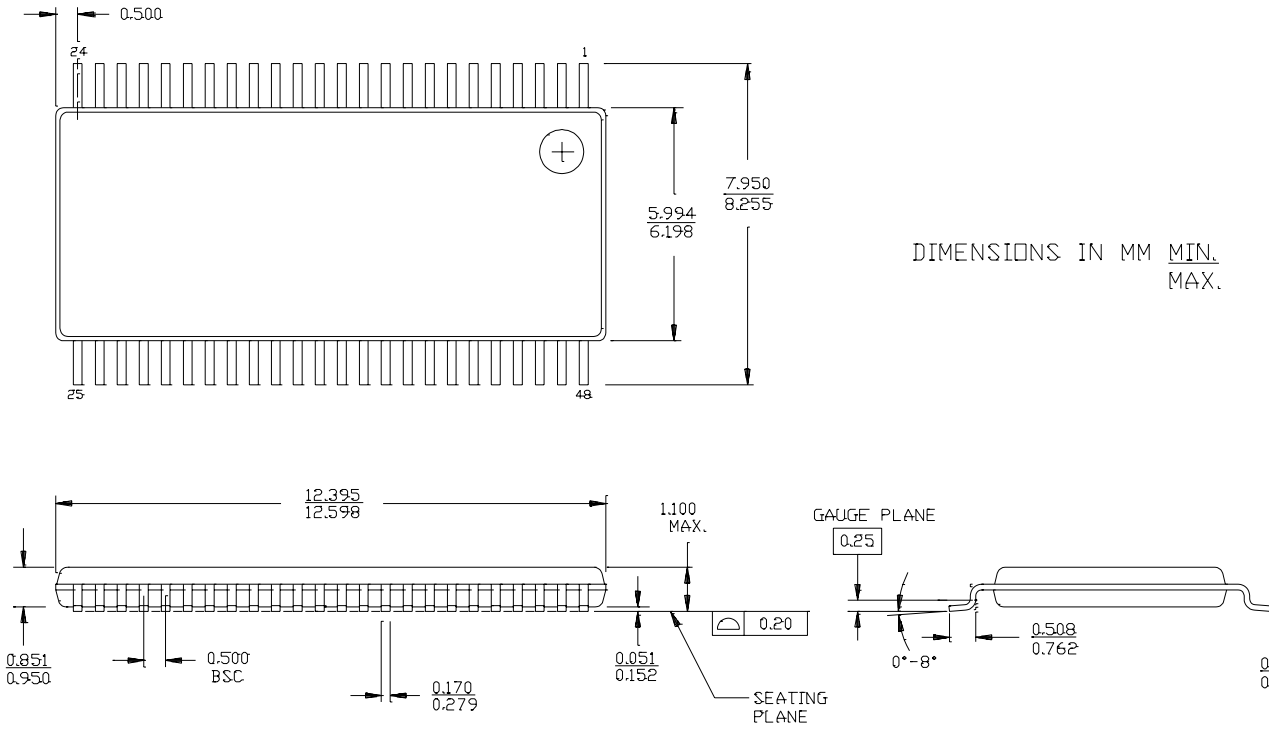
3. MAX(T_{PD_MAX}-T_{PD_MIN}, T_{PD_MAX},(-1)*T_{PD_MIN}) where T_{PD_MAX} is the longest delay of refin to any output measured over at least 1000cycles and T_{PD_MIN} is the minimum (may be negative) delay observed over all outputs over at least 1000 cycles. Full statistics, mean, min., max, stdv for each output will be measured.
4. Maximum Frequency for the TSSOP packaged version is 150 MHz for a load of 10 pf. This limitation is a result of the thermal performance of the package.
5. Theta J = 95°C/W for TSSOP package.

Ordering Information

Base Part Number	Option code	Package	Temperature Range
CY23020ZC	-1	48 pin TSSOP[3]	Commercial (0°–70°)
CY23020LFC	-1	48 pin QFN (contact factory for availability)	Commercial (0°–70°)

Package Diagram

48-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z48



Document Title: CY23020-1 Twenty Output Zero Delay Buffer Document Number: 38-07120				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109287	10/30/01	SZV	New Data Sheet