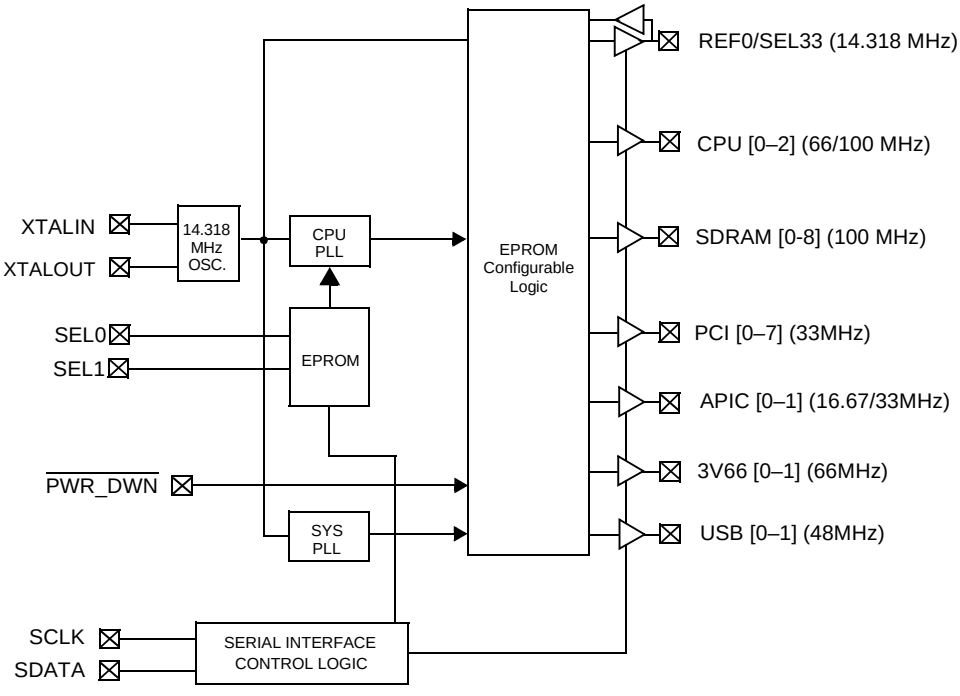
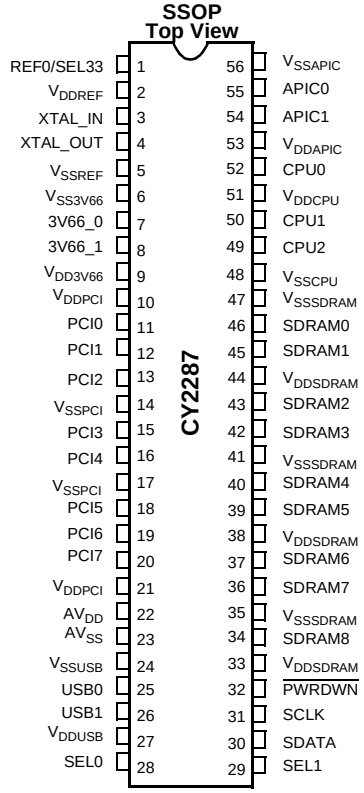
CY2287

100-MHz Spread Spectrum Clock Synthesizer/Driver with USB, Hublink, and SDRAM Support

Features	Benefits
• **Mixed 2.5V and 3.3V Operation**	Usable with Pentium® II, K6, and 6x86 Processors
• **Multiple output clocks at different frequencies** **— Three CPU clocks at 2.5V, up to 100 MHz** **— Nine 3.3V SDRAM clocks at 100 MHz** **— Eight synchronous PCI clocks at 33 MHz** **— Two synchronous APIC clocks at 16.67 MHz or 33 MHz** **— Two 3V66 clocks at 66 MHz** **— Two USB clocks at 48 MHz** **— One reference clock at 14.318 MHz**	Single-chip main motherboard clock generator — High-Speed Processor Support — Supports Two 4-Clock SDRAM DIMMs — Support for Six PCI Slots — Synchronous to the CPU Clock — Hublink Support — Universal Serial Bus Support — Also used as an input strap to determine APIC frequency
• **Spread Spectrum clocking** **— 31 kHz modulation frequency** **— EPROM programmable percentage of spreading** **— Default is –0.6%, which is recommended by Intel®** **— Additional options of –0.25% and –0.4% available**	Enables reduction of EMI
• **Power-down features**	Supports mobile systems
• **Serial Programming Interface**	Dynamic output control
• **Low skew and low jitter outputs**	Meets tight system timing requirements at high frequency
• **Test Mode**	Enables ATE and “bed of nails” testing
• **56-pin SSOP package**	Widely available, standard package enables lower cost

Logic Block Diagram





Pin Summary

Name	Pins	Description
REF/SEL33	1	3.3V 14.31818-MHz clock output and power-on external select strap option for APIC clock frequency. Strap LOW: APIC = PCI/2 Strap HIGH: APIC = 33.3 MHz
XTAL_IN[1]	3	14.31818-MHz crystal input
XTAL_OUT[1]	4	14.31818-MHz crystal output
PCI [0–7]	11, 12, 13, 15, 16, 18, 19, 20	3.3V PCI clock outputs
3V66 [0–1]	7, 8	3.3V Fixed 66.67-MHz clock outputs
USB [0–1]	25, 26	3.3V Fixed 48-MHz clock outputs
SEL [0–1]	28, 29	3.3V LVTTL compatible inputs for logic selection
$\overline{\text{PWRDWN}}$	32	3.3V LVTTL compatible input. Device enters powerdown mode when held LOW
CPU [0–2]	49, 50, 52	2.5V 66.67-MHz or 100-MHz (selectable) host bus clock output
SDRAM [0–8]	35, 36, 37, 39, 40, 42, 43, 45, 46	3.3V SDRAM clock outputs running 100 MHz
APIC [0–1]	54, 55	2.5V APIC clock outputs running synchronous with PCI clock frequency. Selectable 16.67 MHz or 33.3 MHz
DATA	30	SPI compatible DATA input
CLK	31	SPI compatible CLK input
V_{DDREF}	2	3.3V Power supply for REF output
V_{SSREF}	5	REF ground
V_{SS3V66}	6	3V66 Ground
V_{DD3V66}	9	3.3V Power supply for 3V66 outputs
V_{DDPCI}	10, 21	3.3V Power supply for PCI outputs
V_{SSPCI}	14, 17	PCI ground
AV_{DD}	22	3.3V Analog power supply
AV_{SS}	23	Analog ground
V_{SSUSB}	24	USB ground
V_{DDUSB}	27	3.3V Power supply for USB outputs
$V_{DDSDRAM}$	33, 38, 44	3.3V Power supply for SDRAM outputs
$V_{SSSDRAM}$	35, 41, 47	SDRAM ground
V_{SSCPU}	48	CPU ground
V_{DDCPU}	51	2.5V Power supply for CPU outputs
V_{DDAPIC}	53	2.5V Power supply for APIC outputs
V_{SSAPIC}	56	APIC ground

Note:

1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF. For crystals with different C_{LOAD}, please refer to the application note, “Crystal Oscillator Topics.”

Function Table

SEL2[2]	SEL1	SEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI (MHz)	USB (MHz)	REF (MHz)	APIC[4] (MHz)	APIC[5] (MHz)
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	TCLK[3]/2	TCLK/2	TCLK/3	TCLK/8	TCLK/2	TCLK	TCLK/16	TCLK/8
0	1	0	66.67	100	66.67	33.33	48	14.318	16.67	33.33
0	1	1	100	100	66.67	33.33	48	14.318	16.67	33.33
1	0	0	66.67	100	66.67	33.33	48	14.318	16.67	33.33
1	0	1	100	100	66.67	33.33	48	14.318	16.67	33.33
1	1	0	66.67	100	66.67	33.33	48	14.318	16.67	33.33
1	1	1	100	100	66.67	33.33	48	14.318	16.67	33.33

Spread Spectrum[2]	SEL2[2]	SEL1	SEL0	Spread Spectrum Margin
X	0	0	0	N/A
X	0	0	1	N/A
0	X	X	X	N/A
1	0	1	0	–0.6%
1	0	1	1	–0.6%
1	1	0	0	–0.25%
1	1	0	1	–0.25%
1	1	1	0	–0.4%
1	1	1	1	–0.4%

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.288	–5230
CPUCLK	100.0	99.432	–5680
USBCLK	48.0	48.008	+167

Notes:

2. Not a dedicated input pin. This selection must be addressed via Serial Programming Interface.
3. TCLK supplied on the XTALIN pin in Test Mode.
4. SEL33 = LOW (power-on latch input).
5. SEL33 = HIGH (power-on latch input).

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits must be programmed to “0”.
- SPI Address for the CY2287 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0

Byte 0: Spread Spectrum, USB, SDRAM8 Control Register (1 = Enable, 0 = Disable) Default = Enable (for Bit [0:2]) Default = Disable (for Bit [3:7])

Bit	Pin #	Description
Bit 7	--	Reserved
Bit 6	--	Reserved
Bit 5	--	Reserved
Bit4	--	SEL2
Bit3	--	Spread Spectrum (Default = Disable)
Bit2	26	USB1
Bit1	25	USB0
Bit0	49	CPU2

Byte 1: SDRAM Control Register (1 = Enable, 0 = Disable) Default = Enable

Bit	Pin #	Description
Bit 7	36	SDRAM7
Bit 6	37	SDRAM6
Bit 5	39	SDRAM5
Bit 4	40	SDRAM4
Bit 3	42	SDRAM3
Bit 2	43	SDRAM2
Bit 1	45	SDRAM1
Bit 0	46	SDRAM0

Byte 2: PCI Control Register (1 = Enable, 0 = Disable) Default = Enable (for Bit [1:7]) Default = Disable (for Bit 0)

Bit	Pin #	Description
Bit 7	20	PCI7
Bit 6	19	PCI6
Bit 5	18	PCI5
Bit 4	16	PCI4
Bit 3	15	PCI3
Bit 2	13	PCI2
Bit 1	12	PCI1
Bit 0	11	Reserved

Byte 3: Peripheral Control Register (0 = Enable, 1 = Disable) Default = Enable

Bit	Pin #	Description
Bit 7	8	3V66_1
Bit 6	7	3V66_0
Bit 5	11	PCI0
Bit 4	34	SDRAM8
Bit 3	54	APIC1
Bit 2	55	APIC0
Bit 1	50	CPU1
Bit 0	52	CPU0

Byte 4: Reserved Register (0 = Enable, 1 = Disable) Default = Disable

Bit	Pin #	Description
Bit 7	--	Reserved
Bit 6	--	Reserved
Bit 5	--	Reserved
Bit 4	--	Reserved
Bit 3	--	Reserved
Bit 2	--	Reserved
Bit 1	--	Reserved
Bit 0	--	Reserved

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +7.0V

Input Voltage..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Junction Temperature..... +150°C

Package Power Dissipation..... 1W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions Over Which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
$V_{DD3.3V}$	3.3V Supply Voltages	3.135	3.465	V
$V_{DD2.5V}$	2.5V Supply Voltages	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPU, USB, REF, APIC SDRAM, PCI, 3V66		 20 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{IH}	High-level Input Voltage	All inputs except SCLK/SDATA and crystal inputs[6]		2.0			V
		SCLK/SDATA		0.7			V_{DD}
V_{IL}	Low-level Input Voltage	All inputs except SCLK/SDATA and crystal inputs[6]				0.8	V
		SCLK/SDATA				0.3	V_{DD}
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$		–10		+10	µA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$		–10		+10	µA
I_{OH}	High-level Output Current	CPU	V_{OH} = 2.0V	–16		-60	mA
		USB, REF	V_{OH} = 2.4V	–15		–51	
		SDRAM	V_{OH} = 2.4V	–30		–100	
		PCI, 3V66	V_{OH} = 2.4V	–30		–100	
		APIC	V_{OH} = 2.0V	–16		-60	
I_{OL}	Low-level Output Current	CPU	V_{OL} = 0.4V	19		49	mA
		USB, REF	V_{OL} = 0.4V	10		24	
		SDRAM	V_{OL} = 0.4V	20		49	
		PCI, 3V66	V_{OL} = 0.4V	20		49	
		APIC	V_{OL} = 0.4V	19		49	
I_{OZ}	Output Leakage Current	Three-state				10	µA
I_{DD2}	2.5V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V, F_{CPU} = 100 MHz				100	mA
I_{DD3}	3.3V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V, F_{CPU} = 100 MHz				280	mA
I_{DDPD2}	2.5V Shutdown Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V[7]			<1	500	µA
I_{DDPD3}	3.3V Shutdown Current	AV_{DD}/V_{DDQ3} = 3.465V, V_{DD25} = 2.625V[7]			<9	500	µA

Notes:

6. Crystal inputs have CMOS thresholds, nominally $V_{DD}/2$.
7. Tested @ 500 µA. Actual performance is much better. Call Cypress if tighter spec is required.

CY2287 Switching Characteristics[8] Over the Operating Range

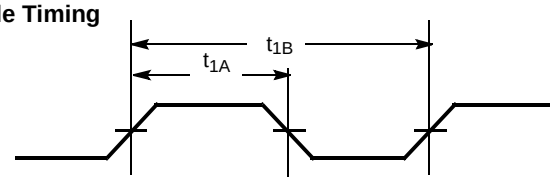
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[9]	$t_{1A}/(t_{1A} + t_{1B})$	45	55	%
t_2	CPU, APIC	Rising Edge Rate	Between 0.4V and 2.0V	1.0	4.0	V/ns
t_2	USB, REF	Rising Edge Rate	Between 0.4V and 2.4V	0.5	2.0	V/ns
t_2	PCI, 3V66	Rising Edge Rate	Between 0.4V and 2.4V	1.0	4.0	V/ns
t_2	SDRAM	Rising Edge Rate	Between 0.4V and 2.4V	1.0	4.0	V/ns
t_3	CPU, APIC	Falling Edge Rate	Between 2.0V and 0.4V	1.0	4.0	V/ns
t_3	USB, REF	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	V/ns
t_3	PCI, 3V66	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t_3	SDRAM	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t_4	CPU	CPU-CPU Skew	Measured at 1.25V		175	ps
t_4	SDRAM	SDRAM-SDRAM Skew	Measured at 1.5V		250	ps
t_4	APIC	APIC-APIC Skew	Measured at 1.25V		250	ps
t_4	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_4	3V66	3V66-3V66 Skew	Measured at 1.5V		175	ps
t_4	3V66, PCI	3V66-PCI Clock Skew	3V66 leads[10]	1.5	4.0	ns
t_4	APIC, PCI	APIC-PCI Clock Skew	Coincident every edge[10, 11]		500	ps
t_5	SDRAM, 3V66	SDRAM-3V66 Clock Skew	Coincident every other 3V66 edge[10]		500	ps
t_{6_66}	CPU, 3V66	CPU-3V66 Clock Skew	CPU leads[10]	7.0	8.0	ns
t_{6_100}	CPU, 3V66	CPU-3V66 Clock Skew	Coincident every other 3V66 edge[10]		500	ps
t_{7_66}	CPU, SDRAM	CPU-SDRAM Clock Skew	SDRAM leads[10, 12]	2.0	3.0	ns
t_{7_100}	CPU, SDRAM	CPU-SDRAM Clock Skew	CPU leads, measured every edge[10]	4.5	5.5	ns
t_8	CPU	Cycle-Cycle Clock Jitter	Measured at 1.25V, $t_{8A} - t_{8B}$		250	ps
t_8	SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.5V, $t_{8A} - t_{8B}$		250	ps
t_8	APIC	Cycle-Cycle Clock Jitter	Measured at 1.25V, $t_{8A} - t_{8B}$		500	ps
t_8	USB	Cycle-Cycle Clock Jitter	Measured at 1.5V, $t_{8A} - t_{8B}$		500	ps
t_8	3V66	Cycle-Cycle Clock Jitter	Measured at 1.5V, $t_{8A} - t_{8B}$		500	ps
t_8	REF	Cycle-Cycle Clock Jitter	Measured at 1.5V, $t_{8A} - t_{8B}$		1000	ps
t_{STABLE}	All Outputs	Settle Time	All clock stabilization from power-up		3	ms

Notes:

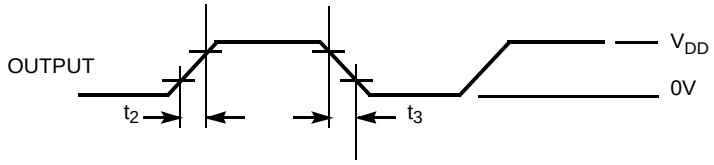
8. All parameters specified with loaded outputs as follows: CPU, APIC, REF, USB = 12.5 pF: SDRAM, 3V66, PCI=20 pF.
9. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
10. Measured at 1.25V for 2.5V clocks and 1.5V for 3.3V clocks.
11. Coincident every other APIC edge if APIC running at 16 MHz.
12. Measured every third CPU edge.

Switching Waveforms

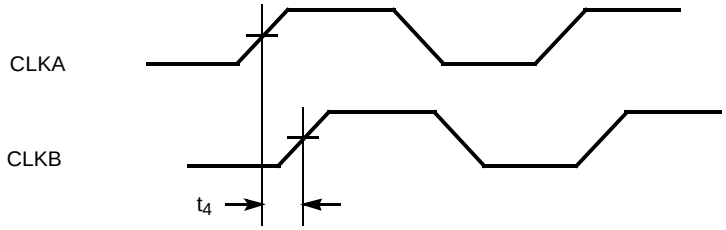
Duty Cycle Timing



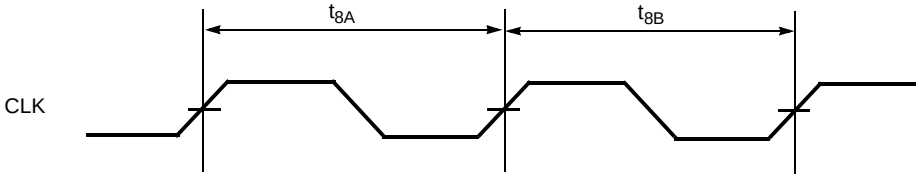
All Outputs Rise/Fall Time



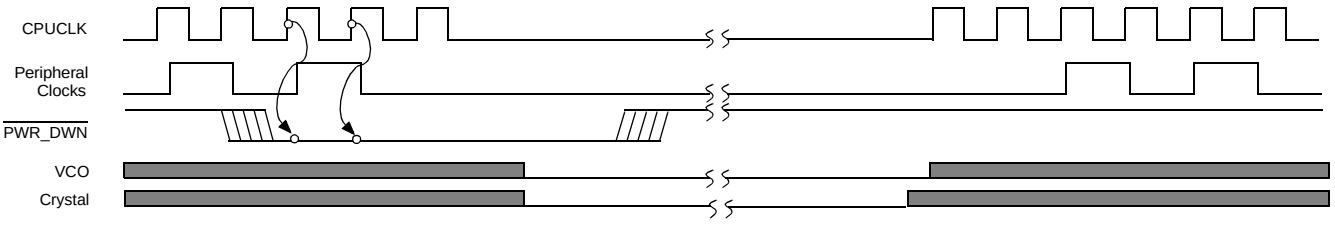
CLK-CLK Output Skew



Cycle-Cycle Clock Jitter



$\overline{\text{PWR\_DOWN}}$ [13, 14, 15]

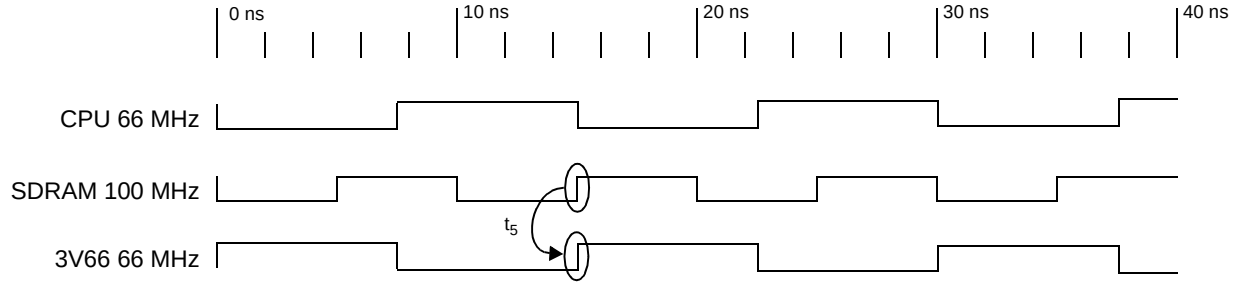


Notes:

13. Once the PWR_DWN signal is sampled LOW for two consecutive rising edges of CPU clock, clocks of interest will be held LOW on the next HIGH-to-LOW transition.
14. Waveforms are not to scale.
15. Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

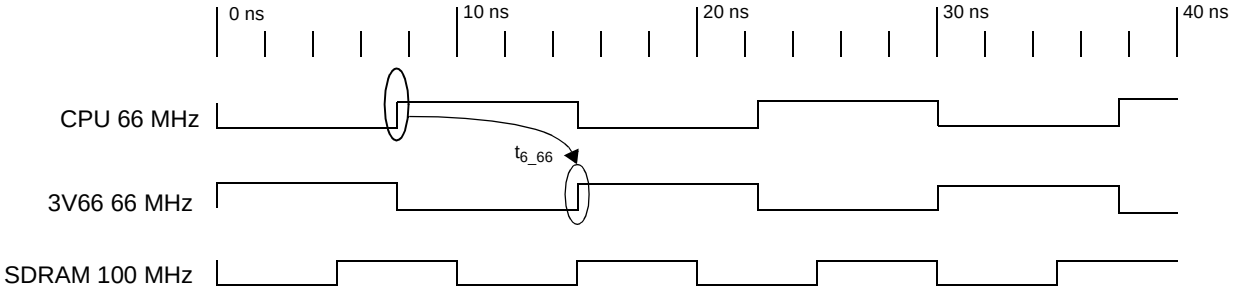
Switching Waveforms (continued)

CLK-CLK Output Skew (CPU @ 66 MHz)



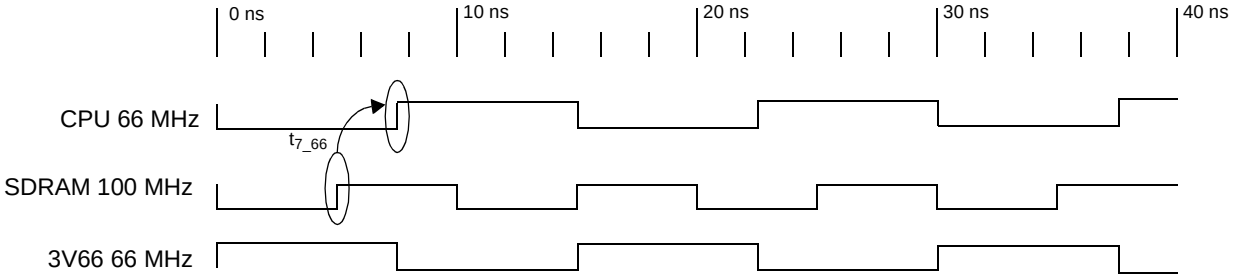
SDRAM to 3V66 Skew, SDRAM leads 3V66 by 0.0 ns (500-ps window)

CLK-CLK Output Skew (CPU @ 66 MHz)



CPU to 3V66 Skew, CPU leads 3V66 by 7.5ns (500-ps window)

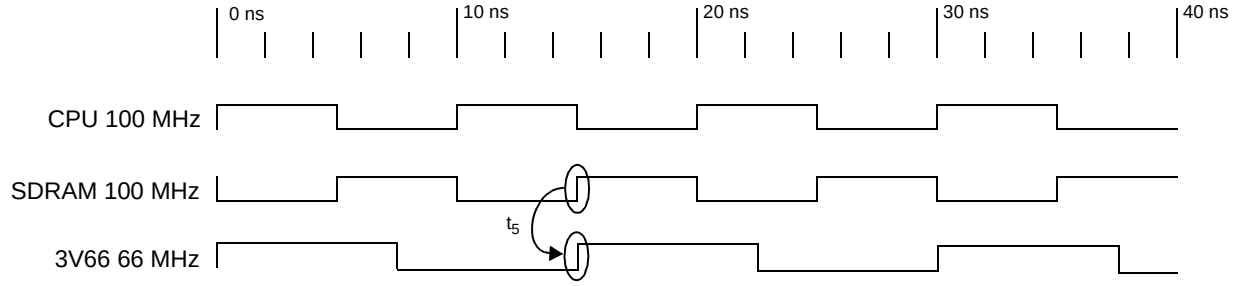
CLK-CLK Output Skew (CPU @ 66 MHz)



CPU to SDRAM Skew, SDRAM leads CPU by 2.5 ns (500-ps window)

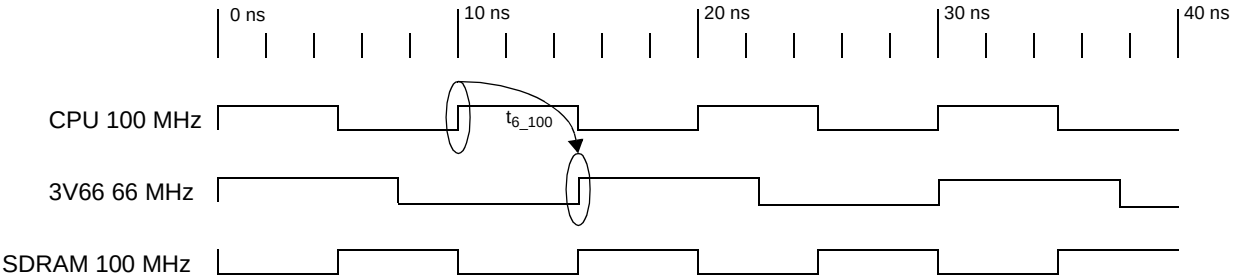
Switching Waveforms (continued)

CLK-CLK Output Skew (CPU @ 100 MHz)



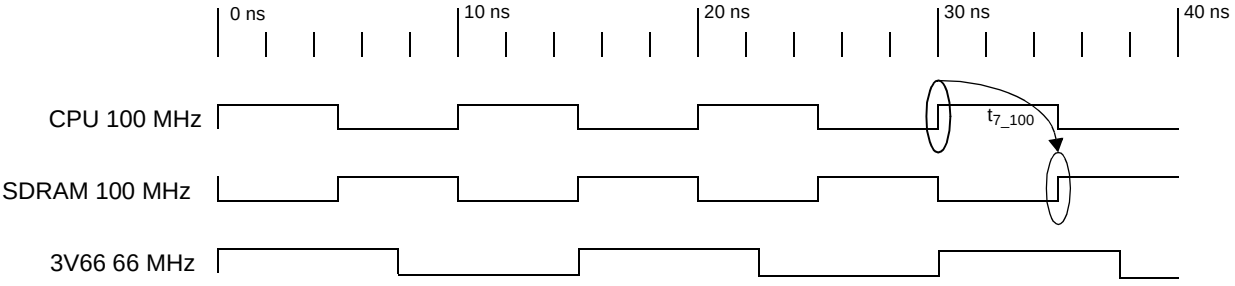
SDRAM to 3V66 Skew, SDRAM leads 3V66 by 0.0 ns (500-ps window)

CLK-CLK Output Skew (CPU @ 100 MHz)



CPU to 3V66 Skew, CPU leads 3V66 by 0.0 ns (500-ps window)

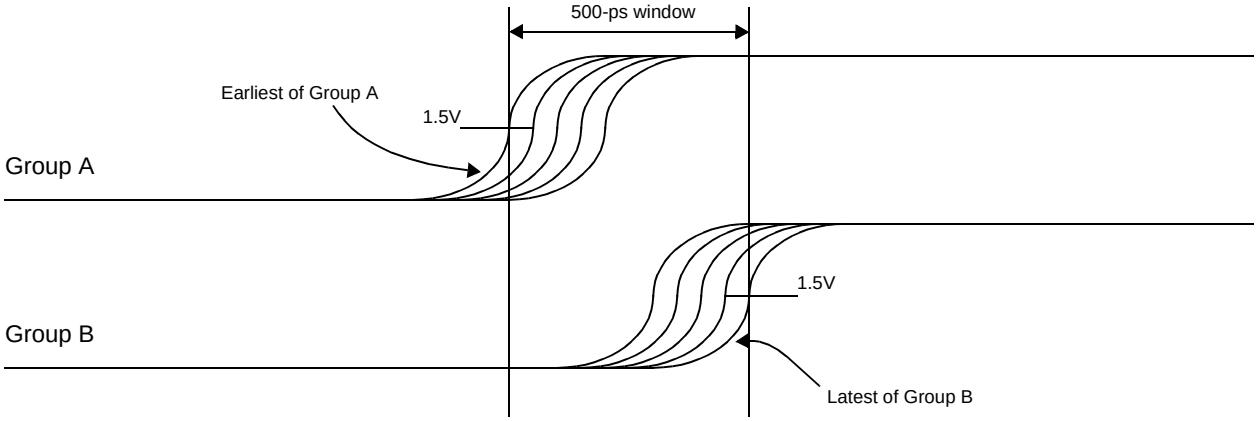
CLK-CLK Output Skew (CPU @ 100 MHz)



CPU to SRAM Skew, CPU leads SDRAM by 5.0 ns (500-ps window)

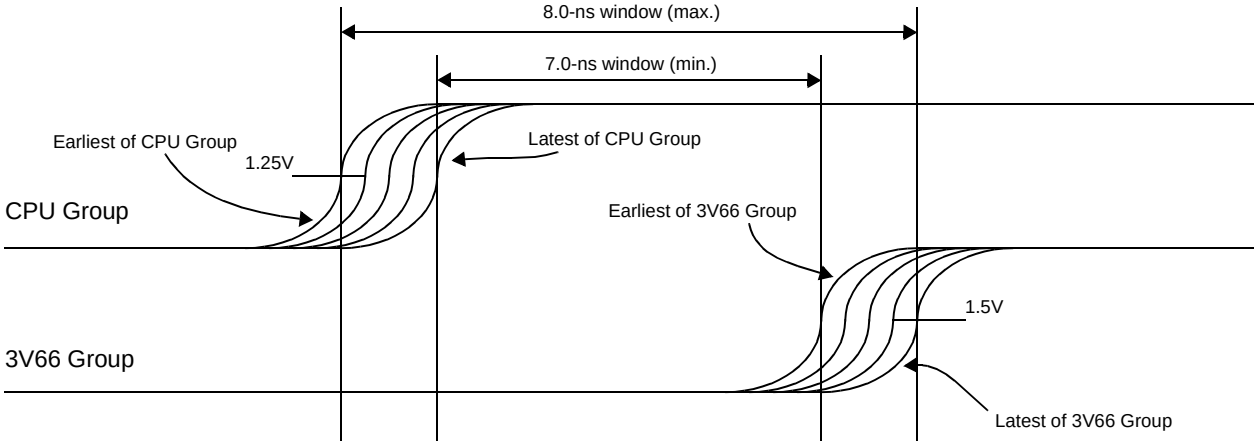
Switching Waveforms (continued)

Window Measurement Clarification



Example of SDRAM to 3V66 Skew Measurement (CPU @ 66 or 100 MHz)
SDRAM leads 3V66 by 0.0 ns (500-ps window)

Window Measurement Clarification

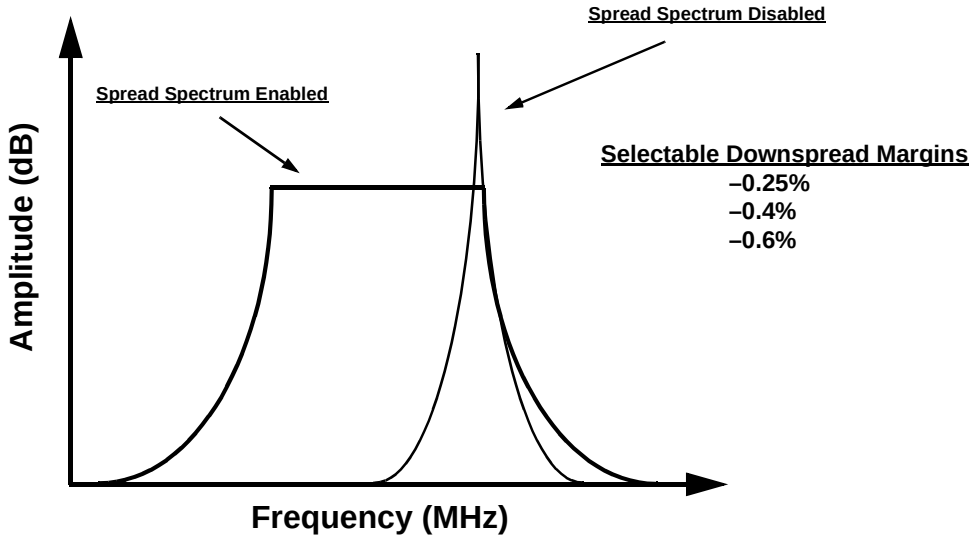


Example of CPU to 3V66 Skew Measurement (CPU @ 66 MHz)
CPU leads 3V66 by 7.5 ns (500-ps window)

Switching Waveforms (continued)

Spread Spectrum Clocking

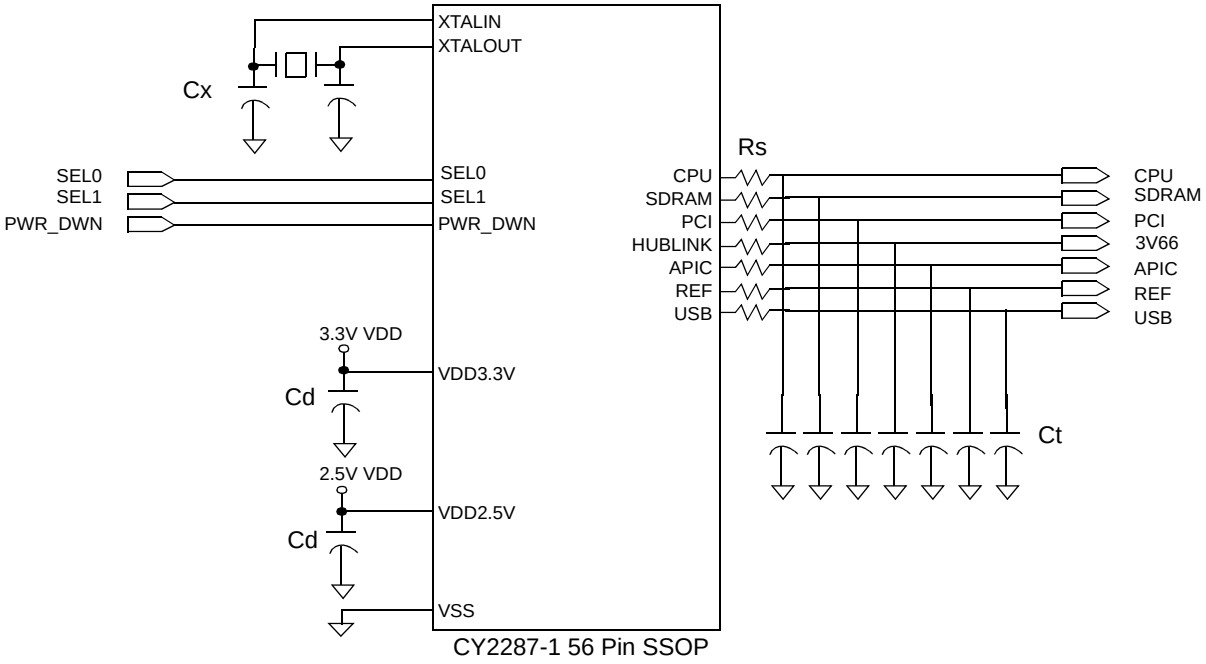
Description	Output	Min.	Max.	Unit
Modulation Frequency	CPU, PCI, SDRAM, APIC, 3V66	30.0	33.0	kHz
Down Spread Margin at the Fundamental Frequency	CPU, PCI, SDRAM, APIC, 3V66	–0.25	–0.6	%



Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.

Application Circuit

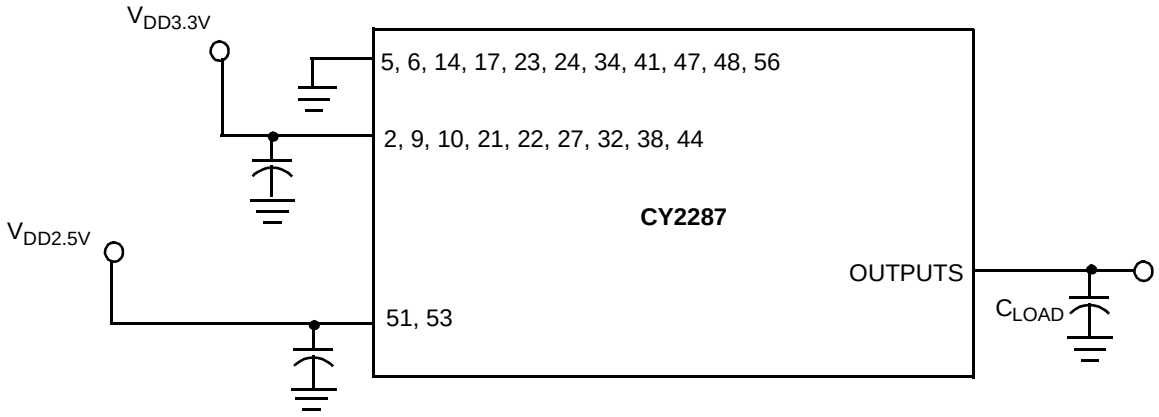


Cd = Decoupling Capacitors (NOTE: May use 0.1 µF, but value will vary with frequency of operation and output current)
Ct = Optional EMI-Reducing Capacitors
Cx = Optional Load Matching Capacitors
Rs = Termination Resistor

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 2.2 nF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (CPU/APIC = 29Ω, USB/REF = 40Ω, SDRAM (3.3V)= 16Ω, PCI/3V66 = 30Ω—all nominal driver output impedances), and R_{series} is the series terminating resistor.
  $$R_{series} \geq R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: Each supply pin must have an individual decoupling capacitor.

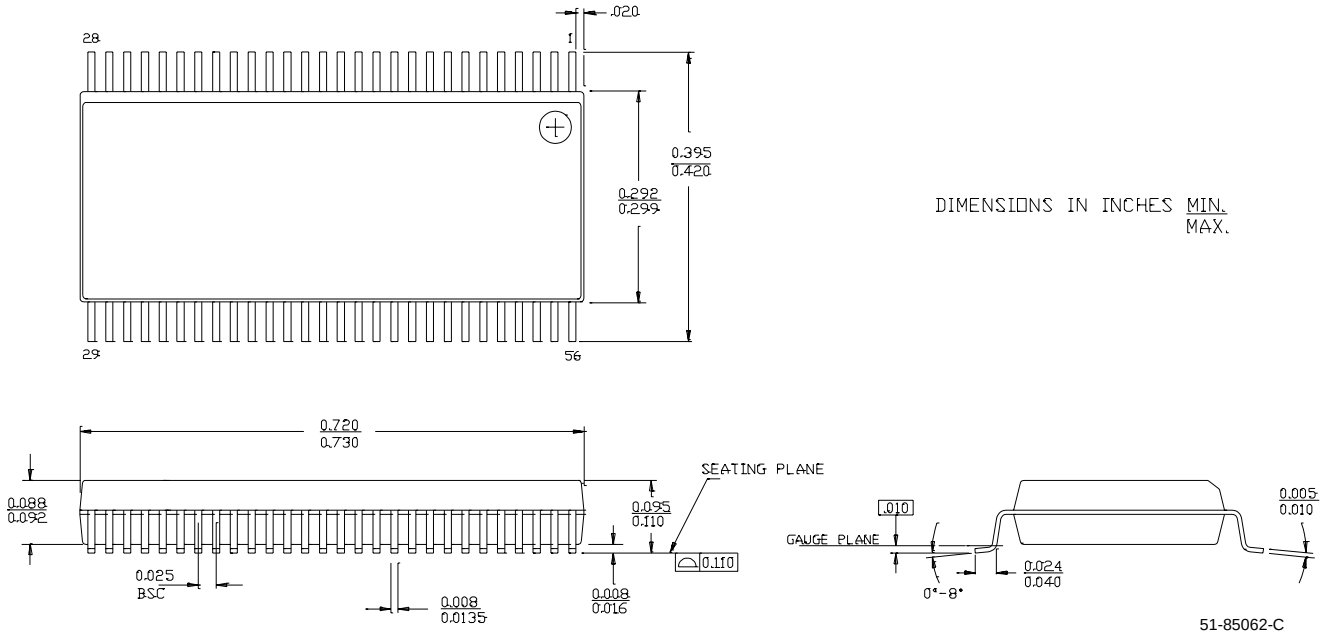
Note: All capacitors must be placed as close to the pins as is physically possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2287PVC–1	O56	56-Pin SSOP	Commercial

Package Diagram

56-Lead Shrunk Small Outline Package O56



Document Title: CY2287 100-MHz Spread Spectrum Clock Synthesizer/Driver with USB, Hublink, and SDRAM Support Document Number: 38-07202				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111722	12/19/01	DSG	Change from Spec number: 38-00711 to 38-07202