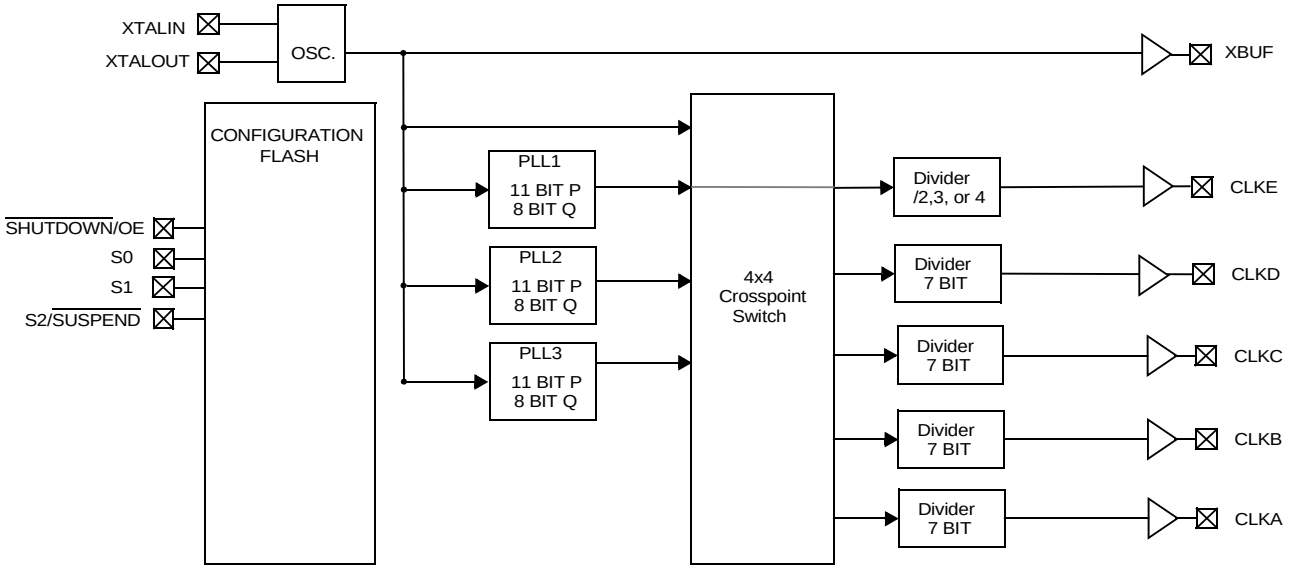
CY22392

Three-PLL General Purpose FLASH Programmable Clock Generator

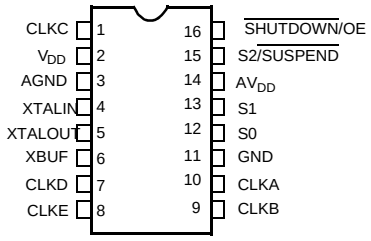
Features	Benefits
Three integrated phase-locked loops	Generates up to 3 unique frequencies on 6 outputs up to 200 MHz from an external source. Functional upgrade for current CY2292 family.
Ultra Wide Divide Counters (8-bit Q, 11-bit P, and 7-bit Post Divide)	Allows for 0 ppm Frequency Generation and Frequency Conversion under the most demanding applications.
Improved Linear Crystal Load Capacitors	Improves frequency accuracy over temperature, age, process, and initial offset.
Flash programmability	Non-Volatile programming enables easy customization, ultra-fast turnaround, performance tweaking, design timing margin testing, inventory control, lower part count, and more secure product supply. In addition, any part in the family can also be programmed multiple times which reduces programming errors and provides an easy upgrade path for existing designs.
Field programmable	In-house programming of samples and prototype quantities is available using the CY3672 FTG Development Kit. Production quantities are available through Cypress Semiconductor's value added Distribution partners or by using third party programmers from BP Microsystems, HiLo Systems, and others.
Low-jitter, high-accuracy outputs	Performance suitable for high-end multimedia, communications, industrial, A/D Converters, and consumer applications.
Power-management options (Shutdown, OE, Suspend)	Supports numerous low-power application schemes and reduces EMI by allowing unused outputs to be turned off.
Configurable Crystal Drive Strength	Adjust Crystal Drive Strength for compatibility with virtually all crystals.
Frequency Select via 3 External LVTTL Inputs	3-Bit External Frequency Select Options for PLL1, CLKA, and CLKB.
3.3V operation	Industry-standard supply voltage.
16-pin TSSOP Packages	Industry-standard packaging saves on board space.
CyClocksRT™ Support	Easy to use software support for design entry.

Logic Block Diagram



Pin Configuration

CY22392
16-pin TSSOP



Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY22392FC	6	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	Up to 200 MHz	Commercial Temperature
CY22392FI	6	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	Up to 166 MHz	Industrial Temperature

Pin Summary

Name	Pin Number	Description
CLKC	1	Configurable clock output C
V_{DD}	2	Power supply
AGND	3	Analog Ground
XTALIN	4	Reference crystal input or external reference clock input
XTALOUT	5	Reference crystal feedback
XBUF	6	Buffered reference clock output
CLKD	7	Configurable clock output D
CLKE	8	Configurable clock output E
CLKB	9	Configurable clock output B
CLKA	10	Configurable clock output A
GND	11	Ground
S0	12	General Purpose Input for Frequency Control; bit 0
S1	13	General Purpose Input for Frequency Control; bit 1
AV_{DD}	14	Analog Power Supply
S2/$\overline{\text{SUSPEND}}$	15	General Purpose Input for Frequency Control; bit 2. Optionally Suspend mode control input.
$\overline{\text{SHUTDOWN}}$/OE	16	Places outputs in three-state condition and shuts down chip when LOW. Optionally, only places outputs in tristate condition and does not shut down chip when LOW

Operation

The CY22392 is an upgrade to the existing CY2292. The new device has a wider frequency range, greater flexibility, improved performance, and incorporates many features that reduce PLL sensitivity to external system issues.

The device has three PLLs which, when combined with the reference, allow up to four independent frequencies to be output on up to six pins. These three PLLs are completely programmable.

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to the crosspoint switch. The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed by external CMOS inputs, S0, S1, S2. See the following section on General-Purpose Inputs for more details.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch.

PLL3 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the cross-point switch.

General-Purpose Inputs

S0, S1, and S2 are general-purpose inputs that can be programmed to allow for eight different frequency settings. Options that may be switched with these general purpose inputs are as follows; the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA.

CLKA and CLKB both have 7-bit dividers that point to one of two programmable settings (register 0 and register 1). Both clocks share a single register control, so both must be set to register 0, or both must be set to register 1.

For example: the part may be programmed to use S0, S1, and S2 (0,0,0 to 1,1,1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch free.

Crystal Input

The input crystal oscillator is an important feature of this device because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This allows for maximum compatibility with crystals from various manufacturers, processes, performances, and qualities.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors should not be used for MPEG, POTS dial tone, Communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

Output Configuration

Under normal operation there are four internal frequency sources that may be routed via a programmable crosspoint switch to any of the four programmable 7-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. In addition, many outputs have a unique capability for even greater flexibility. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. Each of the eight possible combinations of S0, S1, S2 controls which of the two programmable registers is loaded into CLKA's 7-bit post divider. See the section "General-Purpose Inputs" for more information.

CLKB's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. Each of the eight possible combinations of S0, S1, and S2 controls which of the two programmable registers is loaded into CLKA's 7-bit post divider. See the section "General-Purpose" Inputs for more information.

CLKC's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKD's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4.

XBUF is simply the buffered reference.

The Clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination it is generally not recommended.

Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 5 μA (typical). After leaving shutdown mode, the PLLs will have to relock.

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.

Improving Jitter

Jitter Optimization Control is useful in mitigating problems related to similar clocks switching at the same moment, causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning, allowing superior jitter performance.

Power Supply Sequencing

For parts with multiple V_{DD} pins, there are no power supply sequencing requirements. The part will not be fully operational until all V_{DD} pins have been brought up to the voltages specified in the “Operating Conditions” table.

All grounds should be connected to the same ground plane.

CyClocks RT™ Software

CyClocks RT is our second-generation application that allows users to configure this device. The easy-to-use interface offers complete control of the many features of this family including input frequency, PLL and output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. CyClocks RT also has a power estimation feature that allows you to see the power consumption of your specific configuration. You can download a copy of CyClocks RT for free on Cypress’s web site at www.cypress.com.

Junction Temperature Limitations

It is possible to program the CY22392 such that the maximum Junction Temperature rating is exceeded. The package θ_{JA} is 115 C/W. Use the CyClocks RT power estimation feature to verify that the programmed configuration meets the Junction Temperature and Package Power Dissipation maximum ratings.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to + (AV_{DD} + 0.5V)

Storage Temperature ..... –65°C to +125°C

Junction Temperature.....125°C

Data Retention @ Tj = 125°C.....>10 years

Maximum Programming Cycles 100

Package Power Dissipation..... 350 mW

Static Discharge Voltage

(per MIL-STD-883, Method 3015) 2000V

Latch up (per JEDEC 17) ..... $\geq$ ±200 mA

Operating Conditions[1]

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}/AV_{DD}	Supply Voltage	3.135	3.3	3.465	V
T_A	Commercial Operating Temperature, Ambient	0		+70	°C
	Industrial Operating Temperature, Ambient	–40		+85	°C
C_{LOAD_OUT}	Max. Load Capacitance			15	pF
f_{REF}	External Reference Crystal	8		30	MHz
	External Reference Clock[2], Commercial	1		166	MHz
	External Reference Clock[2], Industrial	1		150	MHz

Notes:

1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current[3]	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	24		mA
I_{OL}	Output Low Current[3]	$V_{OL} = 0.5$V, $V_{DD} = 3.3$ V	12	24		mA
C_{XTAL_MIN}	Crystal Load Capacitance[3]	Capload at minimum setting		6		pF
C_{XTAL_MAX}	Crystal Load Capacitance[3]	Capload at maximum setting		30		pF
C_{LOAD_IN}	Input Pin Capacitance[3]	Except crystal pins		7		pF
V_{IH}	HIGH-Level Input Voltage	CMOS levels,% of AV_{DD}	70%			AV_{DD}
V_{IL}	LOW-Level Input Voltage	CMOS levels,% of AV_{DD}			30%	AV_{DD}
I_{IH}	Input HIGH Current	$V_{IN} = AV_{DD} – 0.3$ V		<1	10	µA
I_{IL}	Input LOW Current	$V_{IN} = +0.3$ V		<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs			10	µA
I_{DD}	Total Power Supply Current	3.3V Power Supply; 2 outputs @ 166 MHz; 4 outputs @ 83 MHz		100		mA
		3.3V Power Supply; 2 outputs @ 20 MHz; 4 outputs @ 40 MHz		50		mA
I_{DDS}	Total Power Supply Current in Shutdown Mode	Shutdown active		5	20	µA

Switching Characteristics

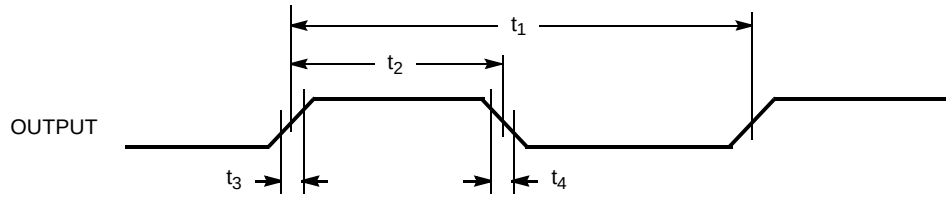
Parameter	Name	Description	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency[3, 4]	Clock output limit, Commercial			200	MHz
		Clock output limit, Industrial			166	MHz
t_2	Output Duty Cycle[3, 5]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout < 100 MHz, divider >= 2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout > 100 MHz or divider = 1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising Edge Slew Rate[3]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_4	Falling Edge Slew Rate[3]	Output clock fall time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_5	Output three-state Timing[3]	Time for output to enter or leave three-state mode after $\overline{\text{SHUTDOWN}}$/OE switches		150	300	ns
t_6	Clock Jitter[3, 6]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$		400		ps
t_7	Lock Time[3]	PLL Lock Time from Power-up		1.0	3	ms

Notes:

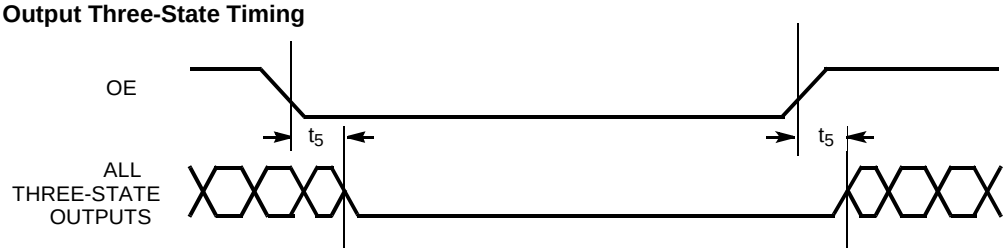
3. Guaranteed by design, not 100% tested.
4. Guaranteed to meet 20%–80% output thresholds and duty cycle specifications.
5. Reference Output duty cycle depends on XTALIN duty cycle.
6. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.

Switching Waveforms

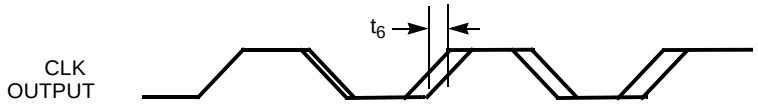
All Outputs, Duty Cycle and Rise/Fall Time



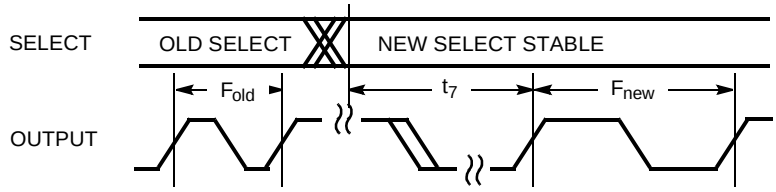
Output Three-State Timing



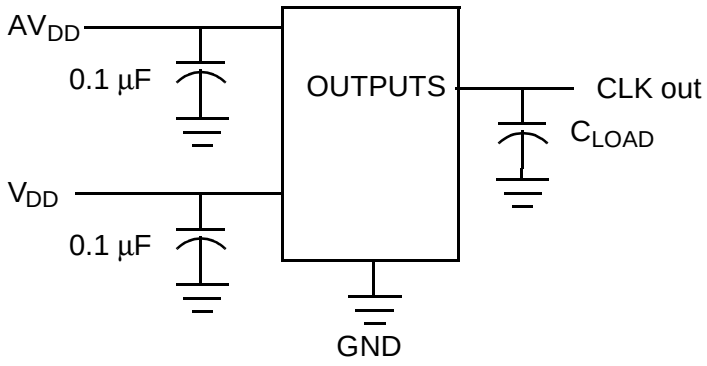
CLK Output Jitter



Frequency Change



Test Circuit



Ordering Information

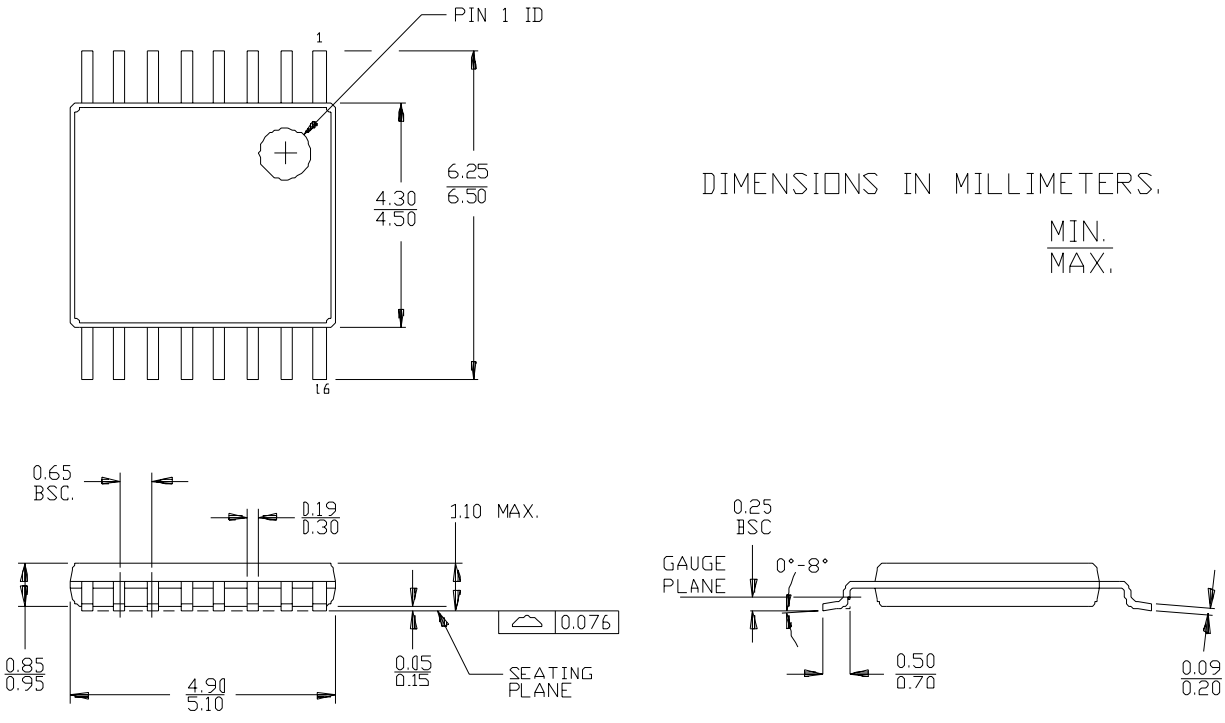
Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY22392FC	Z16	16-TSSOP	Commercial (T_A = 0°C to 70°C)	3.3V
CY22392FI	Z16	16-TSSOP	Industrial (T_A = –40°C to 85°C)	3.3V
CY22392ZC-xxx[7]	Z16	16-TSSOP	Commercial (T_A = 0°C to 70°C)	3.3V
CY22392ZI-xxx[7]	Z16	16-TSSOP	Industrial (T_A = –40°C to 85°C)	3.3V
CY3672	FTG Development Kit			

Notes:

7. The CY22392ZC-xxx and CY22392ZI-xxx are factory programmed configurations. Factory programming is available for high-volume design opportunities of 100 Ku/year or more in production. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Diagram

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



Revision History

Document Title: CY22392 Three PLL General Purpose Flash Programmable Clock Generator Document Number: 38-07013				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106738	07/03/01	TLG	New Data Sheet
*A	108515	08/23/01	JWK	Updates based on characterization results. Removed “Preliminary” heading. Added paragraph on Junction Temperature limitations and part configurations. Removed soldering temperature rating. Split crystal load into two typical specs representing digital settings range. Changed t_5 max to 300 ns. Changed t_7 typical to 1.0 ms.
*B	110052	12/09/01	CKN	Preliminary to Final.

CY22392

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Power-management options (Shutdown, OE, Suspend)	Supports numerous low-power application schemes and reduces EMI by allowing unused outputs to be turned off.
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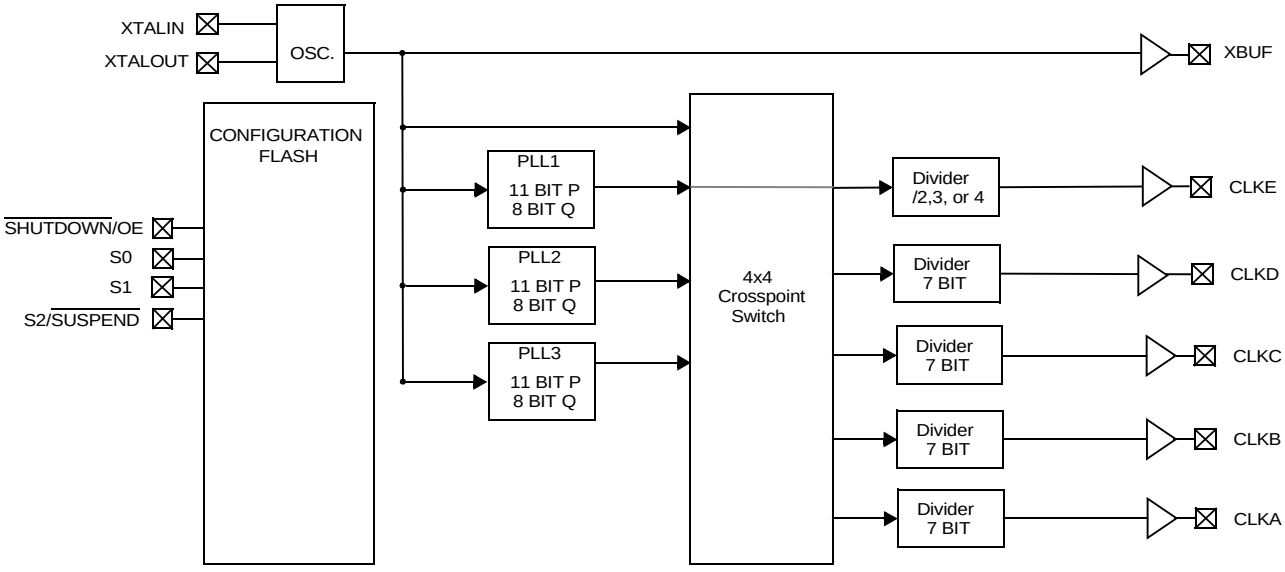
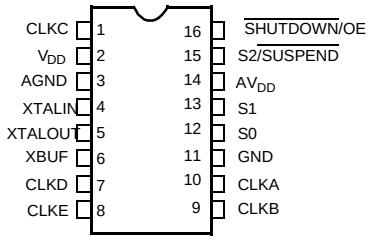


Pin Configuration

CY22392
16-pin TSSOP



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XTALOUT	5	Reference crystal feedback
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S1	13	General Purpose Input for Frequency Control; bit 1
AV_{DD}	14	Analog Power Supply
S2/$\overline{\text{SUSPEND}}$	15	General Purpose Input for Frequency Control; bit 2. Optionally Suspend mode control input.
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Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to the crosspoint switch. The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed by external CMOS inputs, S0, S1, S2. See the following section on General-Purpose Inputs for more details.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch.

PLL3 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the cross-point switch.

General-Purpose Inputs

S0, S1, and S2 are general-purpose inputs that can be programmed to allow for eight different frequency settings. Options that may be switched with these general purpose inputs are as follows; the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA.

CLKA and CLKB both have 7-bit dividers that point to one of two programmable settings (register 0 and register 1). Both clocks share a single register control, so both must be set to register 0, or both must be set to register 1.

For example: the part may be programmed to use S0, S1, and S2 (0,0,0 to 1,1,1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch free.

Crystal Input

The input crystal oscillator is an important feature of this device because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This allows for maximum compatibility with crystals from various manufacturers, processes, performances, and qualities.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors should not be used for MPEG, POTS dial tone, Communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

Output Configuration

Under normal operation there are four internal frequency sources that may be routed via a programmable crosspoint switch to any of the four programmable 7-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. In addition, many outputs have a unique capability for even greater flexibility. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. Each of the eight possible combinations of S0, S1, S2 controls which of the two programmable registers is loaded into CLKA's 7-bit post divider. See the section "General-Purpose Inputs" for more information.

CLKB's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. Each of the eight possible combinations of S0, S1, and S2 controls which of the two programmable registers is loaded into CLKA's 7-bit post divider. See the section "General-Purpose" Inputs for more information.

CLKC's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKD's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4.

XBUF is simply the buffered reference.

The Clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination it is generally not recommended.

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Jitter Optimization Control is useful in mitigating problems related to similar clocks switching at the same moment, causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning, allowing superior jitter performance.

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All grounds should be connected to the same ground plane.

CyClocks RT™ Software

CyClocks RT is our second-generation application that allows users to configure this device. The easy-to-use interface offers complete control of the many features of this family including input frequency, PLL and output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. CyClocks RT also has a power estimation feature that allows you to see the power consumption of your specific configuration. You can download a copy of CyClocks RT for free on Cypress’s web site at www.cypress.com.

Junction Temperature Limitations

It is possible to program the CY22392 such that the maximum Junction Temperature rating is exceeded. The package θ_{JA} is 115 C/W. Use the CyClocks RT power estimation feature to verify that the programmed configuration meets the Junction Temperature and Package Power Dissipation maximum ratings.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to + (AV_{DD} + 0.5V)

Storage Temperature ..... –65°C to +125°C

Junction Temperature.....125°C

Data Retention @ Tj = 125°C.....>10 years

Maximum Programming Cycles 100

Package Power Dissipation..... 350 mW

Static Discharge Voltage

(per MIL-STD-883, Method 3015) 2000V

Latch up (per JEDEC 17) ..... $\geq$ ±200 mA

Operating Conditions[1]

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}/AV_{DD}	Supply Voltage	3.135	3.3	3.465	V
T_A	Commercial Operating Temperature, Ambient	0		+70	°C
	Industrial Operating Temperature, Ambient	–40		+85	°C
C_{LOAD_OUT}	Max. Load Capacitance			15	pF
f_{REF}	External Reference Crystal	8		30	MHz
	External Reference Clock[2], Commercial	1		166	MHz
	External Reference Clock[2], Industrial	1		150	MHz

Notes:

1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current[3]	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	24		mA
I_{OL}	Output Low Current[3]	$V_{OL} = 0.5$V, $V_{DD} = 3.3$ V	12	24		mA
C_{XTAL_MIN}	Crystal Load Capacitance[3]	Capload at minimum setting		6		pF
C_{XTAL_MAX}	Crystal Load Capacitance[3]	Capload at maximum setting		30		pF
C_{LOAD_IN}	Input Pin Capacitance[3]	Except crystal pins		7		pF
V_{IH}	HIGH-Level Input Voltage	CMOS levels,% of AV_{DD}	70%			AV_{DD}
V_{IL}	LOW-Level Input Voltage	CMOS levels,% of AV_{DD}			30%	AV_{DD}
I_{IH}	Input HIGH Current	$V_{IN} = AV_{DD} – 0.3$ V		<1	10	µA
I_{IL}	Input LOW Current	$V_{IN} = +0.3$ V		<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs			10	µA
I_{DD}	Total Power Supply Current	3.3V Power Supply; 2 outputs @ 166 MHz; 4 outputs @ 83 MHz		100		mA
		3.3V Power Supply; 2 outputs @ 20 MHz; 4 outputs @ 40 MHz		50		mA
I_{DDS}	Total Power Supply Current in Shutdown Mode	Shutdown active		5	20	µA

Switching Characteristics

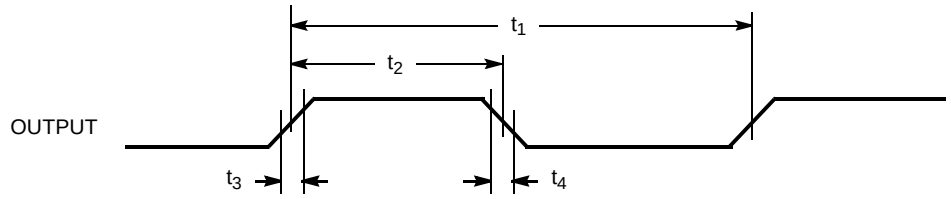
Parameter	Name	Description	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency[3, 4]	Clock output limit, Commercial			200	MHz
		Clock output limit, Industrial			166	MHz
t_2	Output Duty Cycle[3, 5]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout < 100 MHz, divider >= 2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout > 100 MHz or divider = 1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising Edge Slew Rate[3]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_4	Falling Edge Slew Rate[3]	Output clock fall time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_5	Output three-state Timing[3]	Time for output to enter or leave three-state mode after $\overline{\text{SHUTDOWN}}$/OE switches		150	300	ns
t_6	Clock Jitter[3, 6]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$		400		ps
t_7	Lock Time[3]	PLL Lock Time from Power-up		1.0	3	ms

Notes:

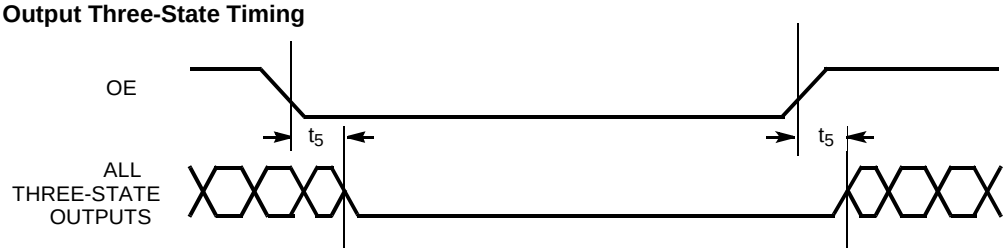
3. Guaranteed by design, not 100% tested.
4. Guaranteed to meet 20%–80% output thresholds and duty cycle specifications.
5. Reference Output duty cycle depends on XTALIN duty cycle.
6. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.

Switching Waveforms

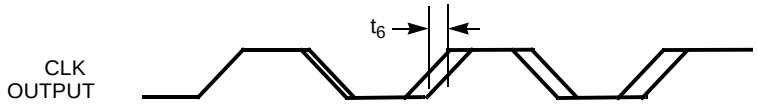
All Outputs, Duty Cycle and Rise/Fall Time



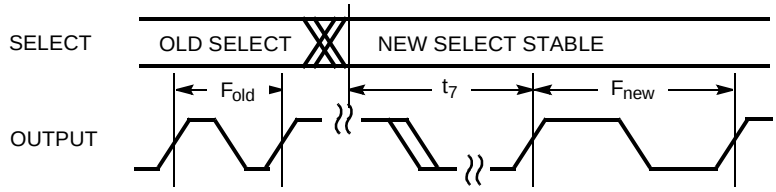
Output Three-State Timing



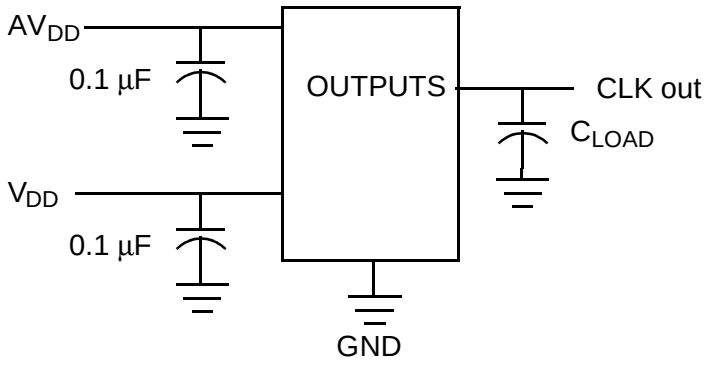
CLK Output Jitter



Frequency Change



Test Circuit



Ordering Information

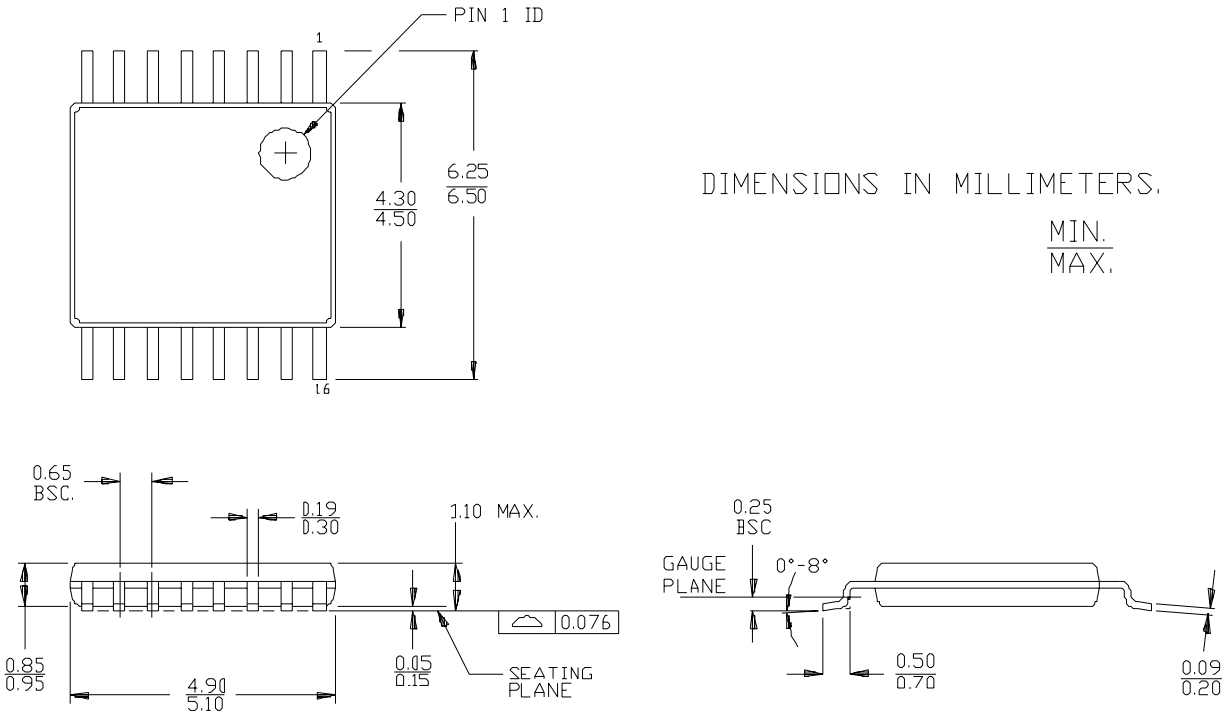
Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY22392FC	Z16	16-TSSOP	Commercial (T_A = 0°C to 70°C)	3.3V
CY22392FI	Z16	16-TSSOP	Industrial (T_A = –40°C to 85°C)	3.3V
CY22392ZC-xxx[7]	Z16	16-TSSOP	Commercial (T_A = 0°C to 70°C)	3.3V
CY22392ZI-xxx[7]	Z16	16-TSSOP	Industrial (T_A = –40°C to 85°C)	3.3V
CY3672	FTG Development Kit			

Notes:

7. The CY22392ZC-xxx and CY22392ZI-xxx are factory programmed configurations. Factory programming is available for high-volume design opportunities of 100 Ku/year or more in production. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Diagram

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



Revision History

Document Title: CY22392 Three PLL General Purpose Flash Programmable Clock Generator Document Number: 38-07013				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106738	07/03/01	TLG	New Data Sheet
*A	108515	08/23/01	JWK	Updates based on characterization results. Removed “Preliminary” heading. Added paragraph on Junction Temperature limitations and part configurations. Removed soldering temperature rating. Split crystal load into two typical specs representing digital settings range. Changed t_5 max to 300 ns. Changed t_7 typical to 1.0 ms.
*B	110052	12/09/01	CKN	Preliminary to Final.