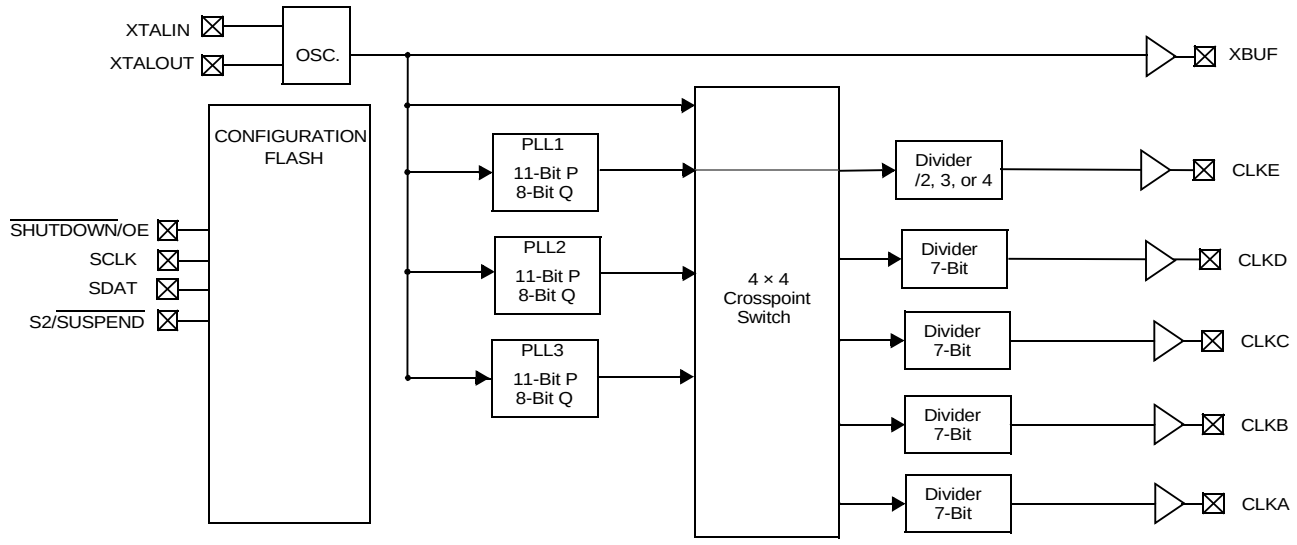
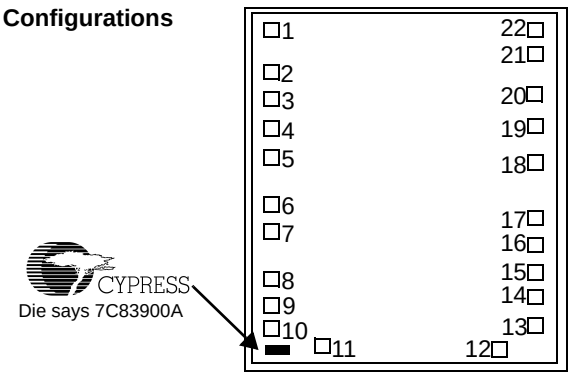
Three-PLL Serial Programmable FLASH Programmable Clock Generator

Features	Benefits
Three integrated phase-locked loops (PLLs)	Generates up to three unique frequencies on up to six outputs from an external source
Ultrawide divide counters (8-bit Q, 11-bit P, and 7-bit post divide)	Allows for 0-ppm frequency generation and frequency conversion under the most demanding applications
Improved linear crystal load capacitors	Improves frequency accuracy over temperature, age, process, and initial offset
Flash programmability	Nonvolatile programming enables easy customization, ultra-fast turnaround, performance tweaking, design timing margin testing, inventory control, lower part count, and more secure product supply. In addition, any part in the family can also be programmed multiple times which reduces programming errors and provides an easy upgrade path for existing designs.
Field programmable	Low-cost distribution or in-house programming support available for all opportunities with Cypress proprietary programmers or BP Micro and others
Low-jitter, high-accuracy outputs	Performance suitable for high-end multimedia, communications, industrial, A/D converters, and consumer applications
Power-management options (shutdown, OE, suspend)	Supports numerous low-power application schemes and reduces EMI by allowing unused outputs to be turned off
Configurable crystal drive strength	Adjust Crystal Drive strength for compatibility with virtually all crystals
Frequency select via three external LVTTL inputs	Three-bit external frequency select options for PLL1, CLKA, and CLKB
3.3V operation	Industry-standard supply voltage
CyClocksRT™ support	Easy to use software support for design entry
Advanced Features	**Benefits**
Serial programmable	Allows in-system programming into volatile configuration memory. All frequency settings can be changed providing literally millions of frequency options.
Configurable output buffer	Adjust output buffer strength to lower EMI or improve timing margin
Digital CXO	Fine tune crystal oscillator frequency by changing load capacitance

Logic Block Diagram



Pad Configurations



Note:
Active Die Size: X = 74.2 mils/1886 um
Y = 88.5 mils/2249 um
Scribe: X,Y = 3.4 mil/86.4 um
Bond pad opening: 2.75 x 2.75 mil
Pad pitch: 4.7 mils (pad center to pad center)
Wafer thickness: 14 mils

Pin Description

Pin Name	Pad Number	Pin Description
CLKC	1	Configurable clock output C
V_{DD}	2	Power supply
LV_{DD}	3	Low voltage clock output power supply
AGND	4	Analog ground
GND	5	Ground
XTALIN	6	Reference crystal input or external reference clock input
XTALOUT	7	Reference crystal feedback
XBUF	8	Buffered reference clock output
LV_{DD}	9	Low-voltage clock output power supply
CLKD or LCLKD	10	Configurable clock output D; LCLKD referenced to LVDD
CLKE or LCLKE	11	Configurable clock output E; LCLKE referenced to LVDD
CLKB or LCLKB	12	Configurable clock output B; LCLKB referenced to LVDD
CLKA or LCLKA	13	Configurable clock output A; LCLKA referenced to LVDD
GND/LGND	14,15	Ground
SDAT (S0)	16	Two-wire serial port data. S0 value latched during startup.
SCLK (S1)	17	Two-wire serial port clock. S1 value latched during startup.
LV_{DD}	18	Low voltage clock output power supply
V_{DD}	19	Power supply
AV_{DD}	20	Analog power supply
S2/ SUSPEND	21	General purpose input for frequency control; bit 2. Optionally suspend mode control input.
$\overline{\text{SHUTDOWN}}$/OE	22	Places outputs in three-state condition and shuts down chip when LOW. Optionally, only places outputs in three-state condition and does not shut down chip when LOW.
Wafer back side	Wafer back side	Ground

Operation

The CY22390 has three PLLs which, when combined with the reference, allow up to four independent frequencies to be output on up to six pins. These three PLLs are completely programmable.

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an eight-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to the crosspoint switch. The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed via serial programming or by external CMOS inputs, S0, S1, S2. See the following section on General-Purpose Inputs for more detail.

PLL2 generates a frequency that is equal to the reference divided by an eight-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch. The frequency of PLL2 can be changed via serial programming.

PLL3 generates a frequency that is equal to the reference divided by an eight-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the crosspoint switch. The frequency of PLL3 can be changed via serial programming.

General-purpose Inputs

S2 is a general-purpose input that can be programmed to allow for two different frequency settings. Options that may be switched with this general purpose input are as follows; the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA.

The two frequency settings are contained within an eight row frequency table. The values of SCLK (S1) and SDAT (S0) pins are latched during startup and used as the other two indexes into this array.

CLKA and CLKB both have seven-bit dividers that point to one of two programmable settings (register 0 and register 1). Both clocks share a single register control, so both must be set to register 0, or both must be set to register 1.

For example, the part may be programmed to use S0, S1, and S2 (0,0,0 to 1,1,1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch-free.

Crystal Input

The input crystal oscillator is an important feature of this part because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This allows for maximum compatibility with crystals from various manufacturers, process, performance, and quality.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors should not be used for MPEG, POTS dial tone, communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

Digital CXO

The serial programming interface may be used to dynamically change the capacitor load value on the crystal. A change in crystal load capacitance corresponds with a change in the reference frequency.

For special pullable crystals specified by Cypress, the capacitance pull range is +150 ppm to –150 ppm from mid-range.

Be aware that adjusting the frequency of the reference will affect all frequencies on all PLLs in a similar manner since all frequencies are derived from the single reference.

Output Configuration

Under normal operation there are four internal frequency sources that may be routed via a programmable crosspoint switch to any of the four programmable seven-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one of two programmable registers. See the section on General Purpose Inputs for more information.

CLKB's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one of two programmable registers. See the section on General Purpose Inputs for more information.

CLKC's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one programmable register.

CLKD's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one programmable register.

CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4.

XBUF is simply the buffered reference.

The Clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination, it is generally not recommended.

Power-saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 5 mA (typical). After leaving shutdown mode, the PLLs will have to relock.

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.

With the serial interface, each PLL and/or output can be individually disabled. This provides total control over the power savings.

Improving Jitter

Jitter Optimization Control is useful in mitigating problems related to similar clocks switching at the same moment, causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning, allowing superior jitter performance.

Power Supply Sequencing

For parts with multiple V_{DD} pins, there are no power supply sequencing requirements. The part will not be fully operational until all V_{DD} pins have been brought up to the voltages specified in the “Operating Conditions” table.

All grounds should be connected to the same ground plane as well as to the back of the die.

CyClocksRT™ Software

CyClocksRT™ is our second-generation application that allows users to configure this device using the CY22393, CY22394, or CY22395 interface. The easy-to-use interface offers complete control of the many features of this device including input frequency, PLL and output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. CyClocksRT also has a power estimation feature that allows you to see the power consumption of your specific configuration. You can download a free copy of CyClocksRT on Cypress’s web site at www.cypress.com.

CyClocksRT is used to generate P, Q, and divider values used in serial programming. There are many internal frequency rules which are not documented in this data sheet, but are required for proper operation of the device. These rules can be checked by using the latest version of CyClocksRT.

Programming information for this device is available from the factory. The bitmap definitions for this device are contained in a document named “SONOS bitmap for CY22390,” which is available from Cypress.

Junction Temperature Limitations

The θ_{JA} of the package used for this part should be considered. It may be possible to program this part such that the maximum junction temperature is exceeded.

Serial Interface Operation

The serial port uses industry standard signaling in both standard and fast modes. This section describes the unique features of the serial interface in this family of devices.

Device Address

The device address is a seven-bit value that is configured during field programming. By programming different device addresses, two or more parts can be connected to the serial interface and be independently controlled. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

Memory Address

This family of devices supports one-byte memory addressing. The memory address is always sent after each Device Address/Write bit combination. It describes the memory location within the device to be accessed. The memory address is incremented after each acknowledge, allowing sequential memory access.

To read a memory location, a write operation must be performed with the memory address to be read, and zero data bytes. This is followed by a repeated start bit and the Device Address/Read byte, after which the desired memory location is available for reading.

Valid memory locations are shown in the “Serial Programming Memory Bitmap” section of the “SONOS bitmap for CY22390” document. All registers are Read- and Write-capable. Some reserved registers are not shown. For proper device operation, do not write data outside of the addresses shown.

Memory Data

For Writes, all of the bytes sent to the device between the Memory Address and a stop bit or repeated start bit are interpreted as data. Each data byte is written to the current memory address, which is incremented after each acknowledge.

For Reads, data is shifted out immediately after the Device Address/Read byte. Bytes are shifted out sequentially until a not-acknowledge followed by a stop bit are received by the device.

Dynamic Updates

The output divider registers are not synchronized with the output clocks. Changing the divider value of an active output will likely cause a glitch on that output.

PLL P and Q data is spread between three bytes. Each byte becomes active on the acknowledge for that byte, so changing P and Q data for an active PLL will likely cause the PLL to try to lock on an out-of-bounds condition. For this reason, it is recommended that the PLL being programmed be turned off during the update. This can be done by setting the PLL*_En bit LOW.

PLL1, CLKA, and CLKB each have multiple registers supplying data. Programming these resources can be accomplished safely by always programming an inactive register, and then transitioning to that register. This allows these resources to stay on during programming.

The serial interface is active even with the $\overline{\text{SHUTDOWN}}$/OE pin LOW as the serial interface logic uses static components and is completely self-timed. The part will not meet the I_{DDS} current limit with transitioning inputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage	–0.5V to +7.0V
DC Input Voltage	–0.5V to + (AV_{DD} + 0.5V)
Storage Temperature	–65°C to +125°C
Junction Temperature	125°C
Data Retention @ T_D = 125°C	> 10 years
Maximum Programming Cycles	100
Static Discharge Voltage (per MIL-STD-883, Method 3015)	≥ 2000V
Latch-up (per JEDEC 17)	≥ ± 200 mA

Operating Conditions[1]

Parameter	Description	Min.	Typ	Max.	Unit
$V_{DD}/AV_{DD}/LV_{DD}$	Supply Voltage	3.135	3.3	3.465	V
T_D	Die Temperature	-40		+125	°C
T_{DP}	Programming Die Temperature	25		+100	°C
C_{LOAD_OUT}	Max. Load Capacitance			15	pF
f_{REF}	External Reference Crystal	8		30	MHz
	External Reference Clock[2] Commercial	1		166	MHz
	External Reference Clock[2] Industrial	1		150	MHz

3.3V Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current[3]	V_{OH} = (L)V_{DD} - 0.5, (L)V_{DD} = 3.3 V	12	24		mA
I_{OL}	Output Low Current[3]	V_{OL} = 0.5, (L)V_{DD} = 3.3 V	12	24		mA
C_{XTAL_MIN}	Crystal Load Capacitance[3]	Capload at minimum setting		6		pF
C_{XTAL_MAX}	Crystal Load Capacitance[3]	Capload at maximum setting		30		pF
C_{IN}	Input Pin Capacitance[3]	Except crystal pins		7		pF
V_{IH}	HIGH-Level Input Voltage	CMOS levels,% of AV_{DD}	70%			AV_{DD}
V_{IL}	LOW-Level Input Voltage	CMOS levels,% of AV_{DD}			30%	AV_{DD}
I_{IH}	Input HIGH Current	V_{IN} = AV_{DD} – 0.3 V		<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.3 V		<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs			10	µA
I_{DD}	Total Power Supply Current	3.3V Power Supply; 2 outputs @ 20 MHz; 4 outputs @ 40MHz		50		mA
		3.3V Power Supply; 2 outputs @ 166 MHz; 4 outputs @ 83 MHz		100		mA
I_{DDS}	Total Power Supply Current in Shut-down Mode	Shutdown active		5	20	µA

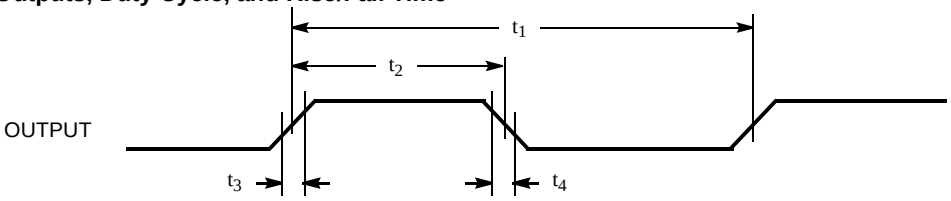
Notes:
1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
3. Guaranteed by design, not 100% tested.

3.3V Switching Characteristics

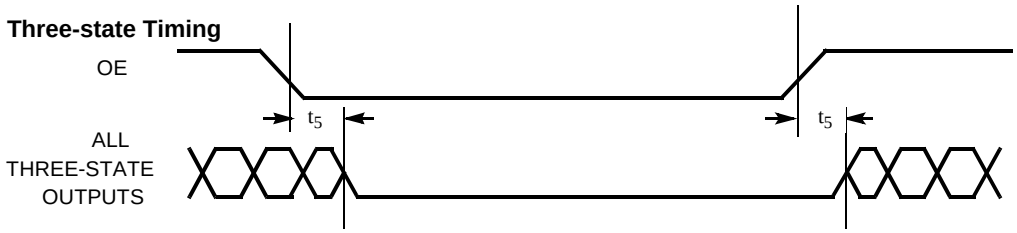
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency[3, 4]	Clock output limit, CMOS, Commercial			200	MHz
		Clock output limit, CMOS, Industrial			166	MHz
t_2	Output Duty Cycle[3, 5]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout < 100 MHz, divider > = 2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout > 100 MHz or divider = 1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising Edge Slew Rate[3]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_4	Falling Edge Slew Rate[3]	Output clock fall time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_5	Output three-state Timing[3]	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches		150	300	ns
t_6	Clock Jitter[3, 6]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$		400		ps
v_7	P+/P- Crossing Point[3]	Crossing point referenced to Vdd/2, balanced resistor network	–0.2	0	0.2	V
t_8	P+/P- Jitter[3, 6]	Peak-to-peak period jitter, P+/P– outputs measured at crossing point		200		ps
t_9	Lock Time[3]	PLL Lock Time from Power-up		1	3	ms

Switching Waveforms[7]

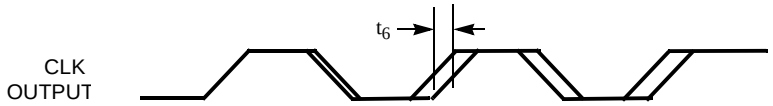
All Outputs, Duty Cycle, and Rise/Fall Time



Three-state Timing



CLK Output Jitter

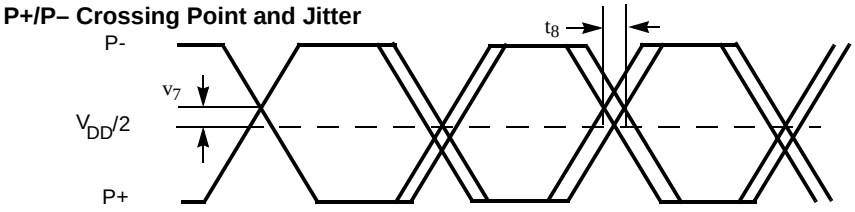


Notes:

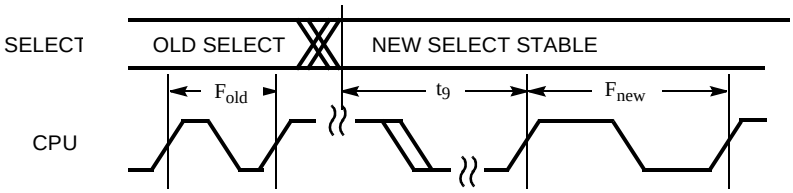
4. Guaranteed to meet 20% - 80% output thresholds, duty cycle, and crossing point specifications.
5. Reference Output duty cycle depends on XTALIN duty cycle.
6. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.
7. I2C timing diagrams are contained in the programming specification.

Switching Waveforms[7]

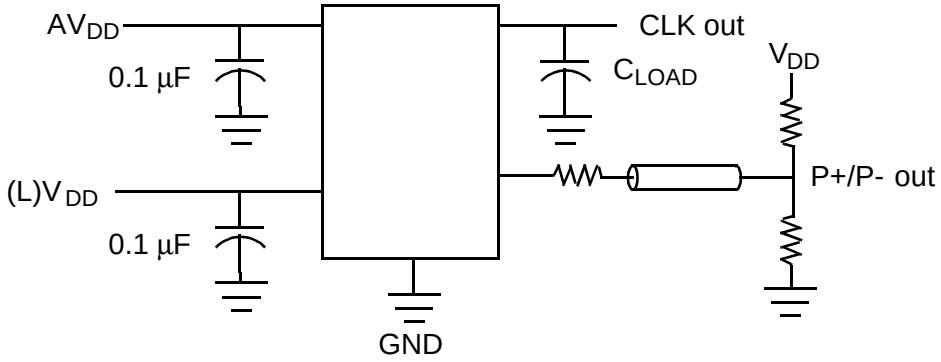
P+/P– Crossing Point and Jitter



Frequency Change



Test Circuit



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**	113755	05/20/02	ADP	New Data Sheet