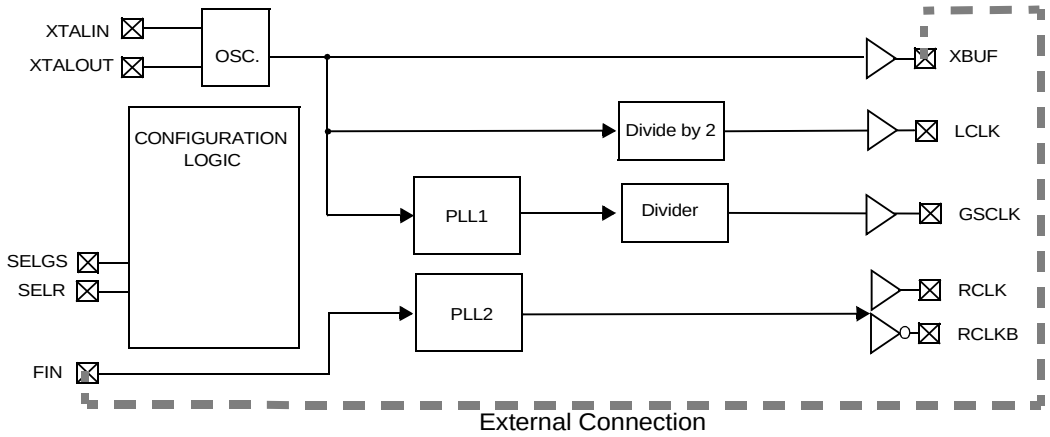
CY22312

Two-PLL Clock Generator with Direct Rambus™ (Lite) Support

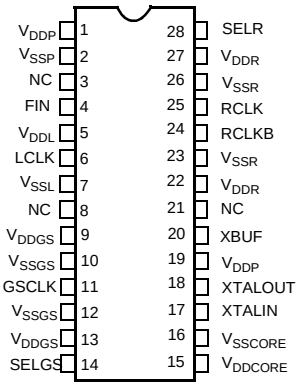
Features	Benefits
Two integrated phase-locked loops	High-performance PLL tailored for multimedia applications
Ultra-accurate PLLs	High performance even with difficult multiplier ratios
Compatible crystal load capacitors	Identical oscillator circuit to CY24141
Direct Rambus™ clock support	One pair of differential output drivers, identical specification to CY2212
Two input selects	Selectable 54.0/53.946 MHz output and 300/400 MHz Rambus® output
3.3V core, 3.3V and 2.5V outputs	Supports SONY output voltage requirements
28-pin TSSOP package	Industry-standard packaging saves on board space

Logic Block Diagram



Pin Configuration

CY22312
28-pin TSSOP



Frequency Select Tables

GSSEL	PPM	GSCLK	Unit
0	0	54	MHz
1	–1.000	53.94605395	MHz

RSEL	PPM	RCLK, RCLKB	Unit
0	0	294.912	MHz
1	0	393.216	MHz

Pin Summary

Name	Pin Numbers	Description
V_{DDP}	1, 19	Power Supply for FIN, XBUF, and Crystal Oscillator
V_{SSP}	2	Ground
NC	3, 8, 21	No Connect (Reserved for Test Mode)
FIN	4	18.432-MHz input, must be externally connected to XBUF
V_{DDL}	5	Power Supply for LCLK
LCLK	6	9.216-MHz output, FIN/2
V_{SSL}	7	Ground
V_{DDGS}	9, 13	Power Supply for GSCLK
V_{SSGS}	10, 12	Ground
GSCLK	11	53.946-MHz/54-MHz output, frequency selectable with SELGS pin
SELGS	14	GSCLK Select Input, Internal Pull-Down Resistor, Referenced to V_{DDCORE}
V_{DDCORE}	15	Power Supply for Core
V_{SSCORE}	16	Ground
XTALIN	17	Reference Crystal Input
XTALOUT	18	Reference Crystal Output
XBUF	20	Buffered Reference Output, must be externally connected to FIN
V_{DDR}	22, 27	Power Supply for RCLK and RCLKB
V_{SSR}	23, 26	Ground
RCLKB	24	Direct Rambus output (complement)
RCLK	25	Direct Rambus output
SELR	28	Direct Rambus PLL Multiplier Select Input, Internal Pull-Up Resistor, Referenced to V_{DDR}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +4.0V

DC Input Voltage ..... –0.5V to + (V_{DD} + 0.5V)

Storage Temperature ..... –65°C to +125°C

Static Discharge Voltage (per MIL-STD-883, Method 3015) 2000V

Latch up (per JEDEC 17) ..... ≥ ±200 mA

Operating Conditions[1]

Parameter	Description	Min.	Typ	Max.	Unit
V_{DDR}, V_{DDCORE}, V_{DDP}	Supply Voltage for Core, Crystal Oscillator, and 3.3V outputs	3.15	3.45	3.6	V
V_{DDGS}, V_{DDL}	Supply Voltage for 2.5V outputs	2.25	2.5	2.75	V
T_A	Operating Temperature, Ambient	0		+70	°C
C_{LOAD_OUT}	Max. Load Capacitance, CMOS outputs			15	pF
f_{REF}	External Reference Crystal		18.432		MHz

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current, 3.3V outputs[2]	V_{OH} = V_{DD} – 0.5, V_{DD} = 3.3V	12	24		mA
	Output High Current, 2.5V outputs[2]	V_{OH} = V_{DD} – 0.5, V_{DD} = 2.5V	8	16		mA
I_{OL}	Output Low Current, 3.3V outputs[2]	V_{OL} = 0.5V, V_{DD} = 3.3V	12	24		mA
	Output Low Current, 2.5V outputs[2]	V_{OL} = 0.5V, V_{DD} = 2.5V	8	16		mA
C_{XTAL}	Crystal Load Capacitance[2]	Total effective load of internal load caps		12.9		pF
C_{LOAD_IN}	Input Pin Capacitance[2]	Except crystal pins		7		pF
V_{IH}	HIGH-Level Input Voltage	CMOS levels,% of referenced power supply	70%			V_{DD}
V_{IL}	LOW-Level Input Voltage	CMOS levels,% of referenced power supply			30%	V_{DD}
R_{I_GS}	SELGS Input Resistor	Pull-down resistor on SELGS	80	100	135	kΩ
R_{I_R}	SELR Input Resistor	Pull-up resistor on SELR	10		100	kΩ
I_{DD}	Total Power Supply Current	Sum of all supply currents			120	mA

Direct Rambus Electrical Characteristics[2]

Parameter	Description	Min.	Max.	Unit.
V_{CM}	Differential output common-mode voltage	1.35	1.75	V
V_X	Differential output crossing-point voltage	1.25	1.85	V
V_{COS}	Output Voltage swing (p-p single-ended)[3]	0.4	0.7	V
V_{COH}	Output high voltage		2.1	V
V_{COL}	Output low voltage	1.0		V
r_{OUT}	Output dynamic resistance (at pins)[4]	12	50	Ω

Notes:

1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. Guaranteed by design, not 100% tested
3. V_{COS} = V_{OH} – V_{OL}.
4. r_{OUT} = Δ V_O/ Δ I_O. This is defined at the output pins, not at the measurement point of *Figure 12*.

Switching Characteristics[2]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
F_{PPM}	Frequency Error	Part to Part, does not include PCB variation[5]		±5	±10	PPM
		Over commercial temperature range[6]		±2	±5	PPM
DC	Output Duty Cycle	Duty cycle for all outputs, measured at $V_{DD}/2$	45%	50%	55%	
t_3	Rising Edge Slew Rate	CMOS clock rise time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_4	Falling Edge Slew Rate	CMOS clock fall time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_{CR}, t_{CF}	Rise and Fall times	RCLK rise and fall time, 20% to 80% of V_{DD}	160		400	ps
t_{CR-CF}	Rise and Fall difference[7]	RCLK rise and fall time difference, 20% to 80% of V_{DD}			100	ps
t_5	Lock Time	PLL Lock Time from Power-up		1.0	3	ms

Jitter Specifications[2]

Parameter	Description	Conditions	Typ.	Max.	Unit
t_{6_XBUF}	XBUF jitter[2]	Cycle-Cycle Jitter - 18.432 MHz		250	ps
t_{6_LCLK}	LCLK jitter[2]	Cycle-Cycle Jitter - 9.216 MHz		250	ps
t_{6_GSCLK}	GSCLK jitter[2]	Cycle-Cycle Jitter - 54 MHz, V_{DDGS} = 2.25V - 2.75V		250	ps
		Cycle-Cycle Jitter - 53.946 MHz, V_{DDGS} = 2.25V - 2.75V		250	ps
t_{7_XBUF}	XBUF 1000 cycle jitter[2]	1000 Cycle-Cycle Jitter - 18.432 MHz		250	ps
t_{7_LCLK}	LCLK 1000 cycle jitter[2]	1000 Cycle-Cycle Jitter - 9.216 MHz		250	ps
t_{7_GSCLK}	GSCLK 1000 cycle jitter[2,8]	1000 Cycle-Cycle Jitter - 54 MHz, V_{DDGS} = 2.25V - 2.75V		400	ps
		1000 Cycle-Cycle Jitter - 53.946 MHz, V_{DDGS} = 2.25V - 2.75V		400	ps
t_8	RCLK 1-6 cycle jitter[2,9]	Cycle-Cycle Jitter, 1-6 Cycles, 400 MHz		100	ps
		Cycle-Cycle Jitter, 1-6 Cycles, 300 MHz		140	ps
t_9	RCLK Long-term jitter[2,10]	Long-term Jitter, 400 MHz		300	ps
		Long-term Jitter, 300 MHz		400	ps
t_{10}	RCLK duty cycle error[2,11]	Cycle-Cycle Duty Cycle Error, 400 MHz		50	ps
		Cycle-Cycle Duty Cycle Error, 300 MHz		70	ps

Notes:

5. Tested across three lots on same board, PCB boards can vary more than ± 5 PPM.
6. Crystal should not be heated for this test, only IC.
7. Measured on same pin of a single device.
8. ± 4 Sigma, V_{DD} = 3.3V.
9. Output short-term jitter specification is peak-to-peak and defined in *Figure 13*.
10. RCLK Long Term jitter shown in *Figure 9*.
11. RCLK Duty Cycle Error shown in *Figure 10*.

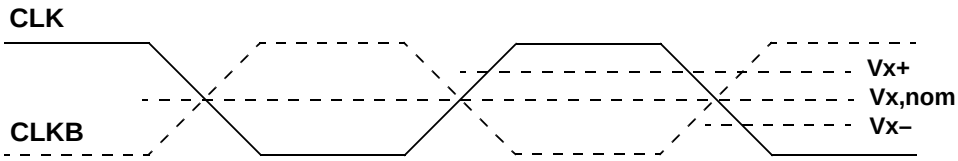


Figure 1. RCLK Crossing Point Voltage

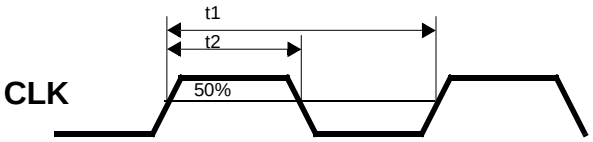
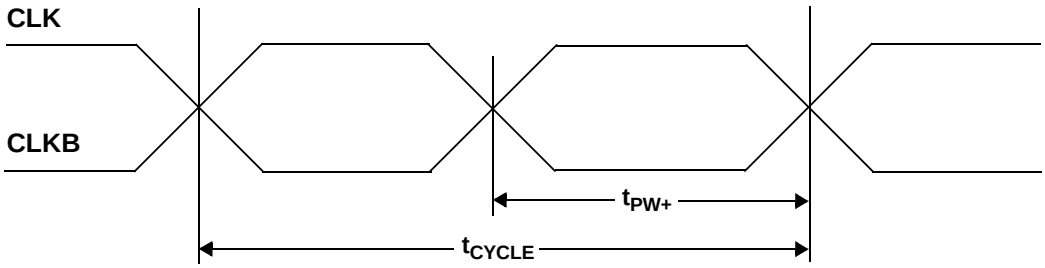


Figure 2. CMOS Duty Cycle Definition



$$DC = t_{PW+}/t_{CYCLE}$$

Figure 3. RCLK Duty Cycle Definition

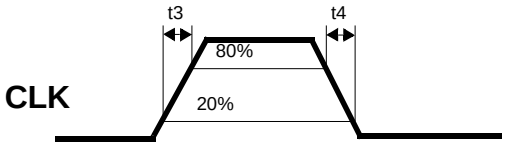


Figure 4. Output Rise and Fall Time Definitions

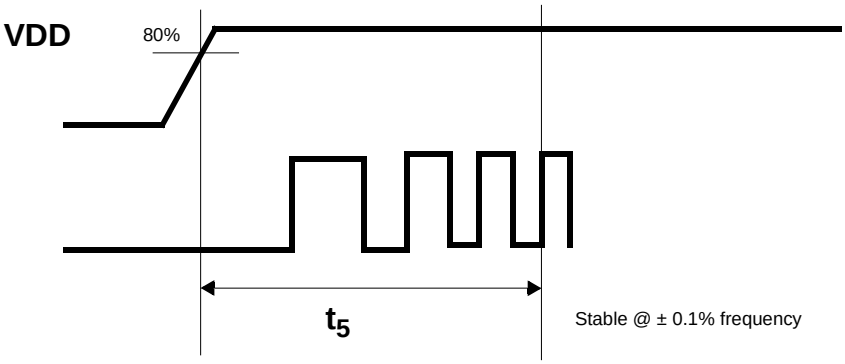


Figure 5. PLL Lock Time

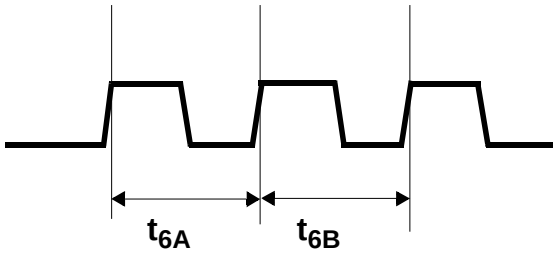


Figure 6. Cycle-to-Cycle Jitter

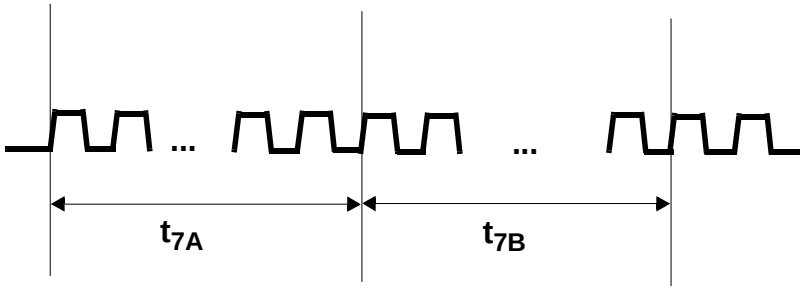
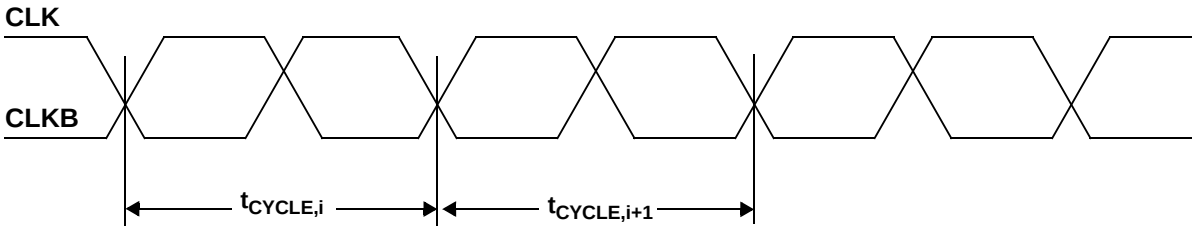
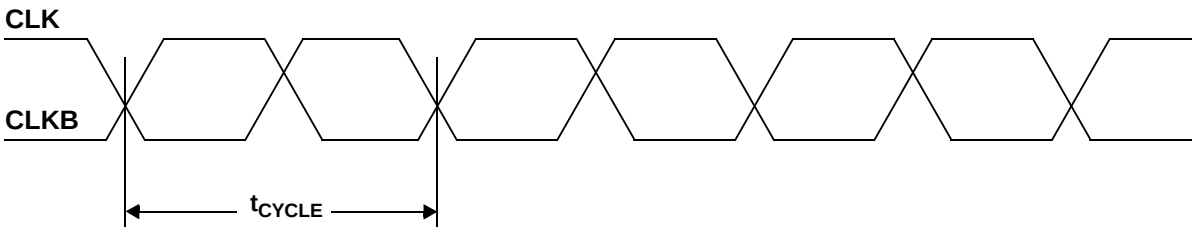


Figure 7. 1000 Cycle Jitter



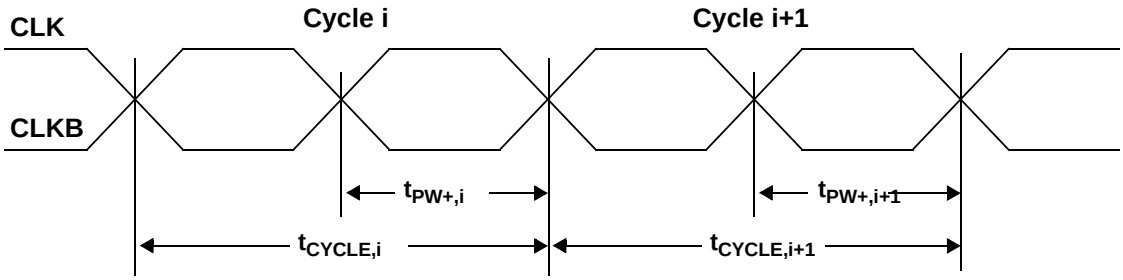
$t_8 = t_{CYLCE,i} - t_{CYCLE,i+1}$ **over 10000 consecutive cycles**

Figure 8. RCLK Cycle-to-Cycle Jitter



$t_9 = t_{CYCLE,max} - t_{CYCLE,min}$ **over 10000 cycles**

Figure 9. RCLK Long-term Jitter



$$t_{10} = t_{PW+,i} - t_{PW+,i+1}$$

Figure 10. RCLK Duty Cycle Error

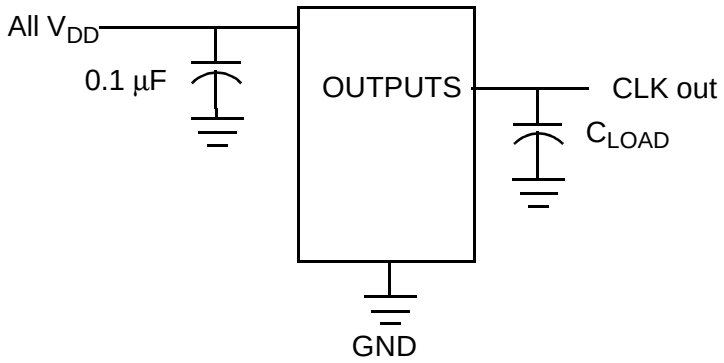


Figure 11. CMOS Output Test Circuits

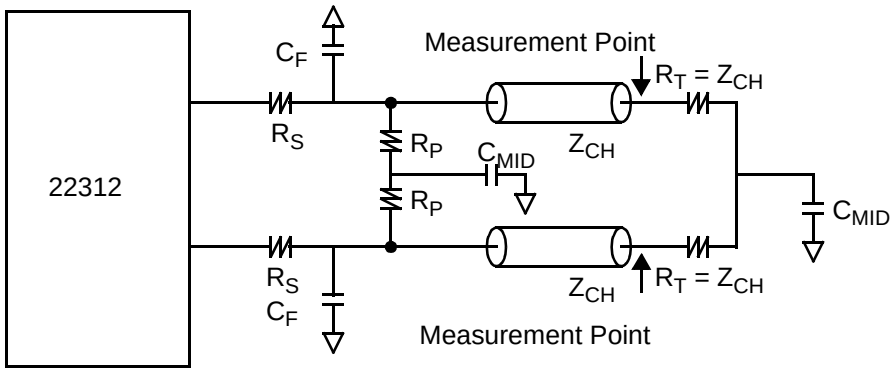
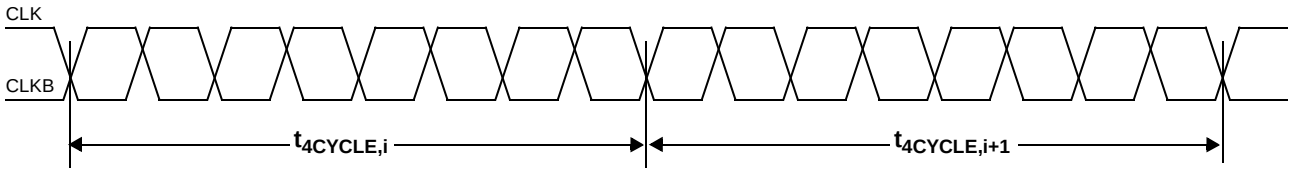


Figure 12. RCLK Test Circuit

Figure 13 shows the definition of 4-cycle short-term jitter. Short-term jitter is defined with respect to the falling edge of the CLK. 4-cycle short-term jitter is the difference between the cumulative cycle times of adjacent 4 cycles. Equal requirements apply for rising edges of the CLK signal. Equal requirements also apply for 2-cycle short-term jitter and 3-cycle short-term jitter, and for 5-cycle short-term jitter and 6-cycle short-term jitter. t_J is defined as the clock output short-term jitter over 2, 3, 4, 5, or 6 cycles.



$$t_J = t_{4CYCLE,i} - t_{4CYCLE,i+1 \text{ over 10000 consecutive cycles}}$$

Figure 13. Short Term Jitter

Table 1. RCLK Test Circuit Component Values

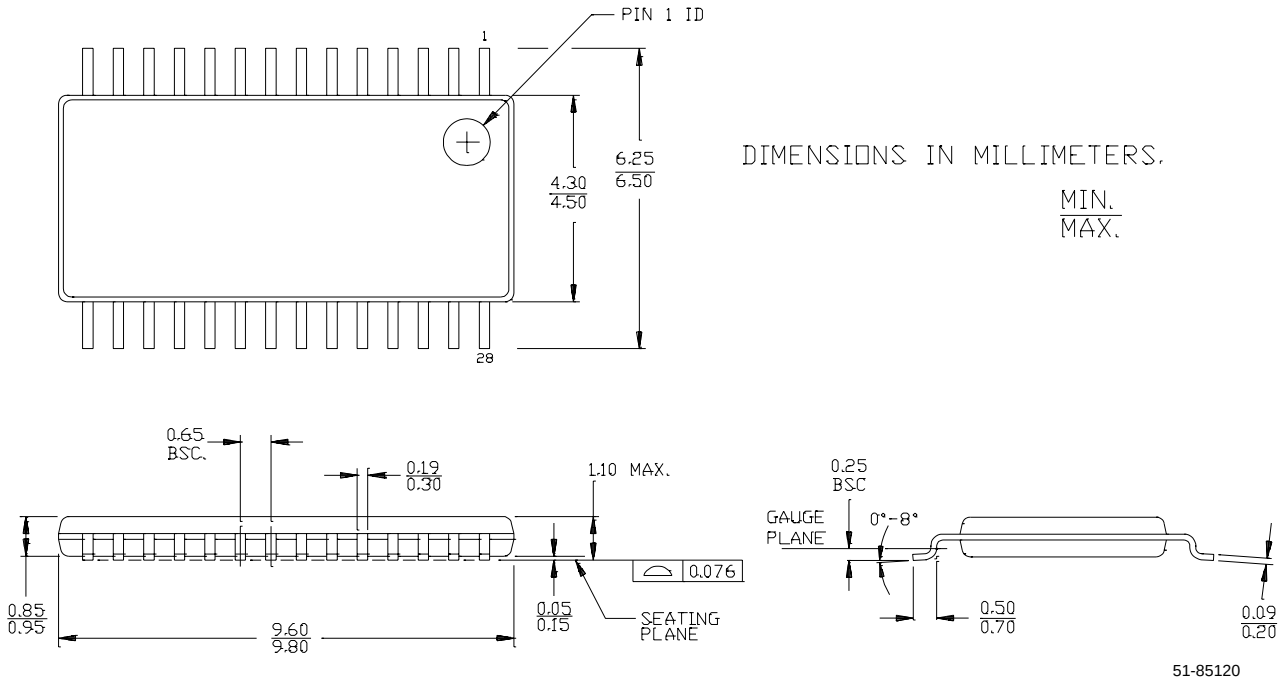
Symbol	Parameter	Value	Tolerance	Unit
R_S	Series Resistor	68	±5%	Ω
R_P	Parallel Resistor	39	±5%	Ω
C_{MID}	AC Ground Capacitor	0.01	±20%	µF

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltages
CY22312ZC	Z29	28-TSSOP	Commercial (T_A=0°C to 70°C)	3.3V

Package Diagram

28-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z29



51-85120

Document Title: CY22312 Two-PLL Clock Generator with Direct Rambus™ (Lite) Support Document Number: 38-07316				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111465	03/01/02	JWK	New Data Sheet

CY22312

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Features	Benefits
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Ultra-accurate PLLs	High performance even with difficult multiplier ratios
Compatible crystal load capacitors	Identical oscillator circuit to CY24141
Direct Rambus™ clock support	One pair of differential output drivers, identical specification to CY2212
Two input selects	Selectable 54.0/53.946 MHz output and 300/400 MHz Rambus® output
3.3V core, 3.3V and 2.5V outputs	Supports SONY output voltage requirements
28-pin TSSOP package	Industry-standard packaging saves on board space

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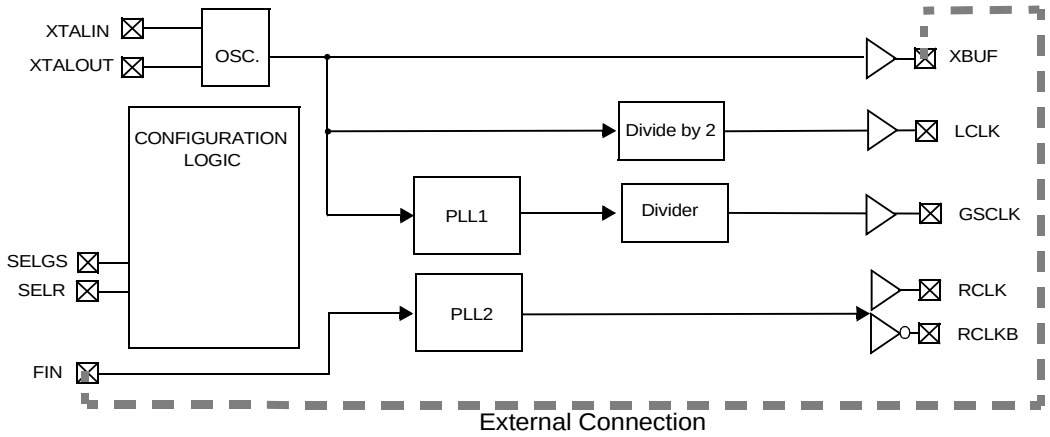
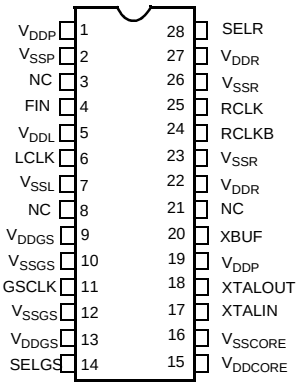


Pin Configuration

CY22312
28-pin TSSOP



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1	–1.000	53.94605395	MHz

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1	0	393.216	MHz

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V_{SSP}	2	Ground
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FIN	4	18.432-MHz input, must be externally connected to XBUF
V_{DDL}	5	Power Supply for LCLK
LCLK	6	9.216-MHz output, FIN/2
V_{SSL}	7	Ground
V_{DDGS}	9, 13	Power Supply for GSCLK
V_{SSGS}	10, 12	Ground
GSCLK	11	53.946-MHz/54-MHz output, frequency selectable with SELGS pin
SELGS	14	GSCLK Select Input, Internal Pull-Down Resistor, Referenced to V_{DDCORE}
V_{DDCORE}	15	Power Supply for Core
V_{SSCORE}	16	Ground
XTALIN	17	Reference Crystal Input
XTALOUT	18	Reference Crystal Output
XBUF	20	Buffered Reference Output, must be externally connected to FIN
V_{DDR}	22, 27	Power Supply for RCLK and RCLKB
V_{SSR}	23, 26	Ground
RCLKB	24	Direct Rambus output (complement)
RCLK	25	Direct Rambus output
SELR	28	Direct Rambus PLL Multiplier Select Input, Internal Pull-Up Resistor, Referenced to V_{DDR}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +4.0V

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Storage Temperature ..... –65°C to +125°C

Static Discharge Voltage (per MIL-STD-883, Method 3015) 2000V

Latch up (per JEDEC 17) ..... ≥ ±200 mA

Operating Conditions[1]

Parameter	Description	Min.	Typ	Max.	Unit
V_{DDR}, V_{DDCORE}, V_{DDP}	Supply Voltage for Core, Crystal Oscillator, and 3.3V outputs	3.15	3.45	3.6	V
V_{DDGS}, V_{DDL}	Supply Voltage for 2.5V outputs	2.25	2.5	2.75	V
T_A	Operating Temperature, Ambient	0		+70	°C
C_{LOAD_OUT}	Max. Load Capacitance, CMOS outputs			15	pF
f_{REF}	External Reference Crystal		18.432		MHz

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
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	Output Low Current, 2.5V outputs[2]	V_{OL} = 0.5V, V_{DD} = 2.5V	8	16		mA
C_{XTAL}	Crystal Load Capacitance[2]	Total effective load of internal load caps		12.9		pF
C_{LOAD_IN}	Input Pin Capacitance[2]	Except crystal pins		7		pF
V_{IH}	HIGH-Level Input Voltage	CMOS levels,% of referenced power supply	70%			V_{DD}
V_{IL}	LOW-Level Input Voltage	CMOS levels,% of referenced power supply			30%	V_{DD}
R_{I_GS}	SELGS Input Resistor	Pull-down resistor on SELGS	80	100	135	kΩ
R_{I_R}	SELR Input Resistor	Pull-up resistor on SELR	10		100	kΩ
I_{DD}	Total Power Supply Current	Sum of all supply currents			120	mA

Direct Rambus Electrical Characteristics[2]

Parameter	Description	Min.	Max.	Unit.
V_{CM}	Differential output common-mode voltage	1.35	1.75	V
V_X	Differential output crossing-point voltage	1.25	1.85	V
V_{COS}	Output Voltage swing (p-p single-ended)[3]	0.4	0.7	V
V_{COH}	Output high voltage		2.1	V
V_{COL}	Output low voltage	1.0		V
r_{OUT}	Output dynamic resistance (at pins)[4]	12	50	Ω

Notes:

1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. Guaranteed by design, not 100% tested
3. V_{COS} = V_{OH} – V_{OL}.
4. r_{OUT} = Δ V_O/ Δ I_O. This is defined at the output pins, not at the measurement point of *Figure 12*.

Switching Characteristics[2]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
F_{PPM}	Frequency Error	Part to Part, does not include PCB variation[5]		±5	±10	PPM
		Over commercial temperature range[6]		±2	±5	PPM
DC	Output Duty Cycle	Duty cycle for all outputs, measured at $V_{DD}/2$	45%	50%	55%	
t_3	Rising Edge Slew Rate	CMOS clock rise time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_4	Falling Edge Slew Rate	CMOS clock fall time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_{CR}, t_{CF}	Rise and Fall times	RCLK rise and fall time, 20% to 80% of V_{DD}	160		400	ps
t_{CR-CF}	Rise and Fall difference[7]	RCLK rise and fall time difference, 20% to 80% of V_{DD}			100	ps
t_5	Lock Time	PLL Lock Time from Power-up		1.0	3	ms

Jitter Specifications[2]

Parameter	Description	Conditions	Typ.	Max.	Unit
t_{6_XBUF}	XBUF jitter[2]	Cycle-Cycle Jitter - 18.432 MHz		250	ps
t_{6_LCLK}	LCLK jitter[2]	Cycle-Cycle Jitter - 9.216 MHz		250	ps
t_{6_GSCLK}	GSCLK jitter[2]	Cycle-Cycle Jitter - 54 MHz, V_{DDGS} = 2.25V - 2.75V		250	ps
		Cycle-Cycle Jitter - 53.946 MHz, V_{DDGS} = 2.25V - 2.75V		250	ps
t_{7_XBUF}	XBUF 1000 cycle jitter[2]	1000 Cycle-Cycle Jitter - 18.432 MHz		250	ps
t_{7_LCLK}	LCLK 1000 cycle jitter[2]	1000 Cycle-Cycle Jitter - 9.216 MHz		250	ps
t_{7_GSCLK}	GSCLK 1000 cycle jitter[2,8]	1000 Cycle-Cycle Jitter - 54 MHz, V_{DDGS} = 2.25V - 2.75V		400	ps
		1000 Cycle-Cycle Jitter - 53.946 MHz, V_{DDGS} = 2.25V - 2.75V		400	ps
t_8	RCLK 1-6 cycle jitter[2,9]	Cycle-Cycle Jitter, 1-6 Cycles, 400 MHz		100	ps
		Cycle-Cycle Jitter, 1-6 Cycles, 300 MHz		140	ps
t_9	RCLK Long-term jitter[2,10]	Long-term Jitter, 400 MHz		300	ps
		Long-term Jitter, 300 MHz		400	ps
t_{10}	RCLK duty cycle error[2,11]	Cycle-Cycle Duty Cycle Error, 400 MHz		50	ps
		Cycle-Cycle Duty Cycle Error, 300 MHz		70	ps

Notes:

5. Tested across three lots on same board, PCB boards can vary more than ± 5 PPM.
6. Crystal should not be heated for this test, only IC.
7. Measured on same pin of a single device.
8. ± 4 Sigma, V_{DD} = 3.3V.
9. Output short-term jitter specification is peak-to-peak and defined in *Figure 13*.
10. RCLK Long Term jitter shown in *Figure 9*.
11. RCLK Duty Cycle Error shown in *Figure 10*.

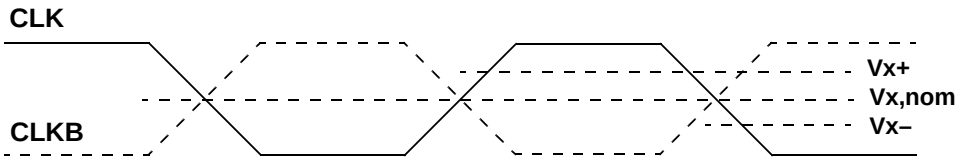


Figure 1. RCLK Crossing Point Voltage

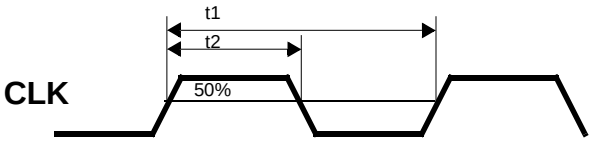
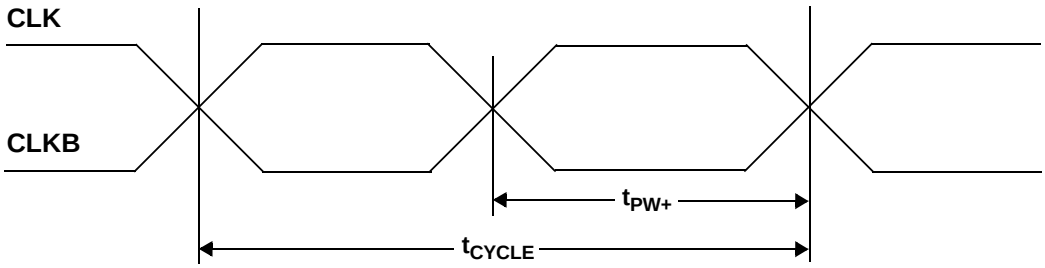


Figure 2. CMOS Duty Cycle Definition



$$DC = t_{PW+}/t_{CYCLE}$$

Figure 3. RCLK Duty Cycle Definition

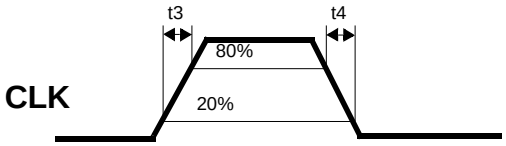


Figure 4. Output Rise and Fall Time Definitions

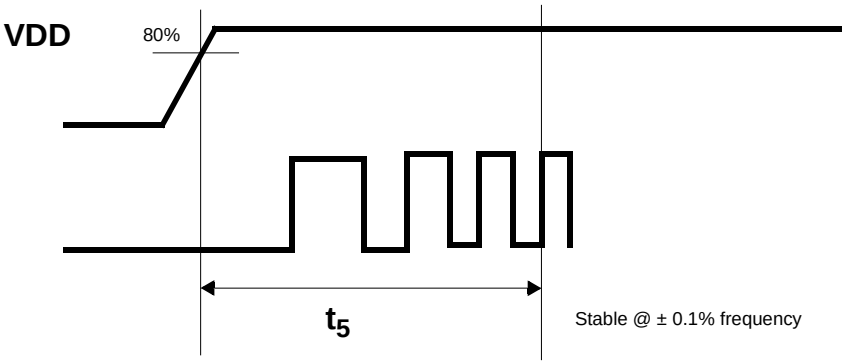


Figure 5. PLL Lock Time

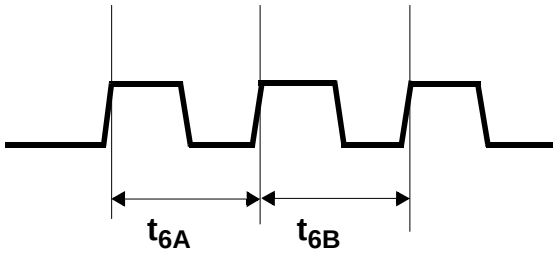


Figure 6. Cycle-to-Cycle Jitter

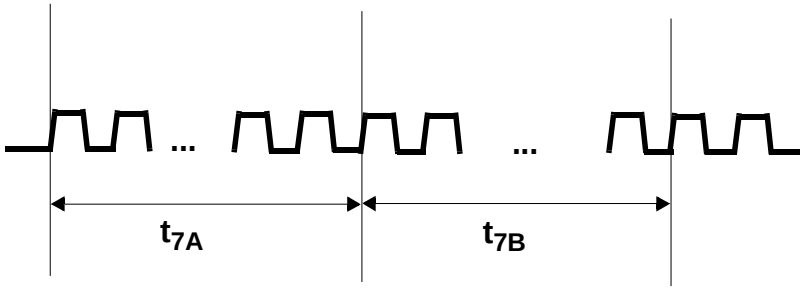
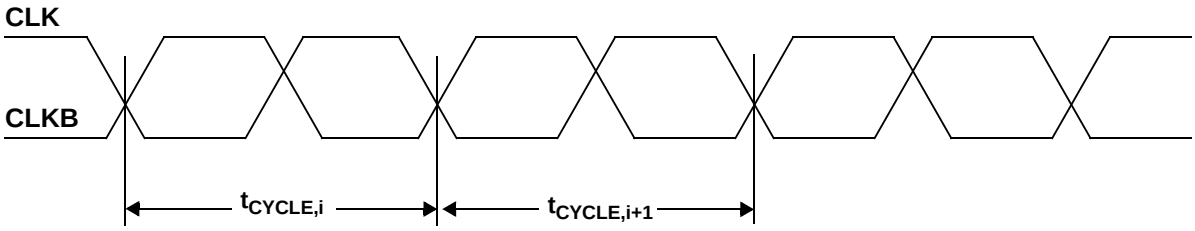
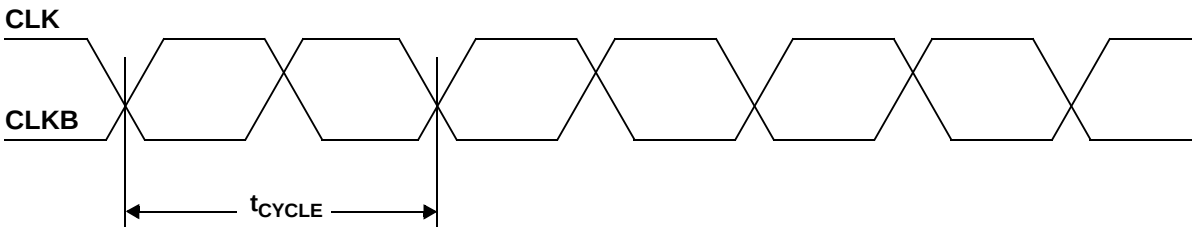


Figure 7. 1000 Cycle Jitter



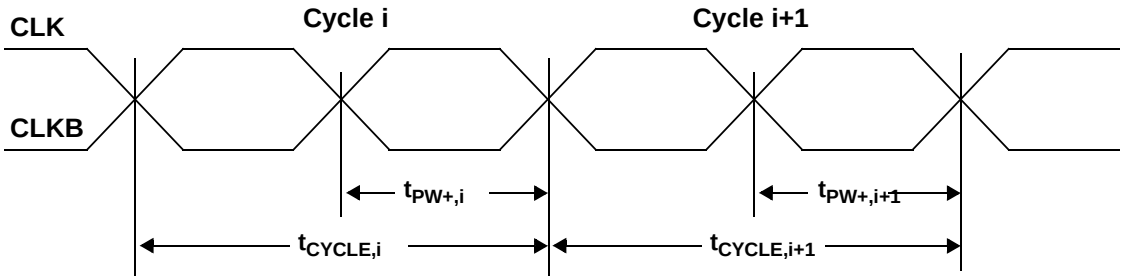
$t_8 = t_{CYLCE,i} - t_{CYCLE,i+1}$ **over 10000 consecutive cycles**

Figure 8. RCLK Cycle-to-Cycle Jitter



$t_9 = t_{CYCLE,max} - t_{CYCLE,min}$ **over 10000 cycles**

Figure 9. RCLK Long-term Jitter



$$t_{10} = t_{PW+,i} - t_{PW+,i+1}$$

Figure 10. RCLK Duty Cycle Error

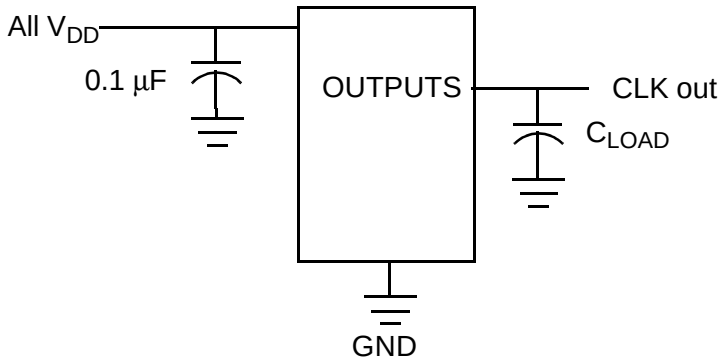


Figure 11. CMOS Output Test Circuits

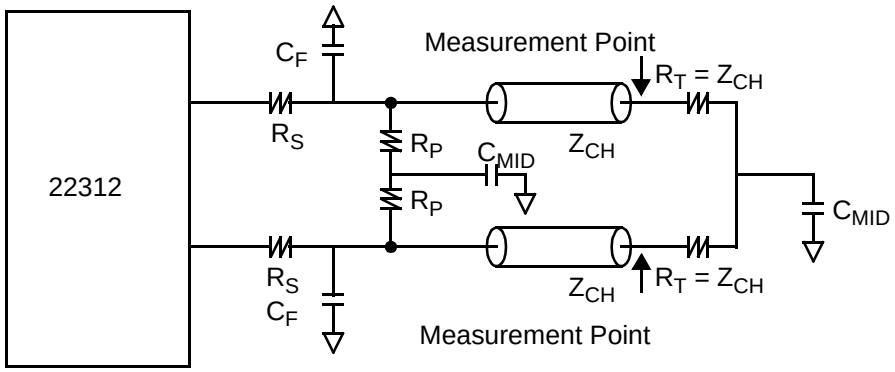
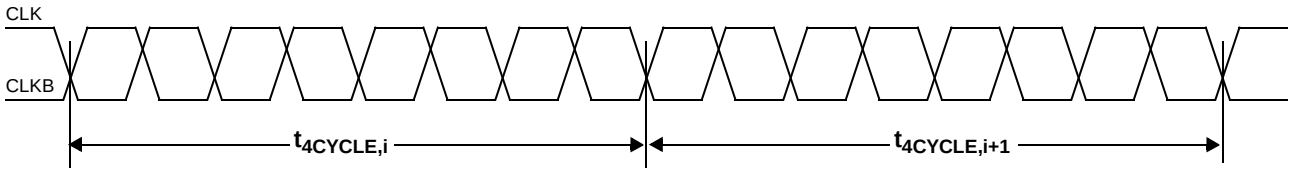


Figure 12. RCLK Test Circuit

Figure 13 shows the definition of 4-cycle short-term jitter. Short-term jitter is defined with respect to the falling edge of the CLK. 4-cycle short-term jitter is the difference between the cumulative cycle times of adjacent 4 cycles. Equal requirements apply for rising edges of the CLK signal. Equal requirements also apply for 2-cycle short-term jitter and 3-cycle short-term jitter, and for 5-cycle short-term jitter and 6-cycle short-term jitter. t_J is defined as the clock output short-term jitter over 2, 3, 4, 5, or 6 cycles.



$$t_J = t_{4CYCLE,i} - t_{4CYCLE,i+1 \text{ over 10000 consecutive cycles}}$$

Figure 13. Short Term Jitter

Table 1. RCLK Test Circuit Component Values

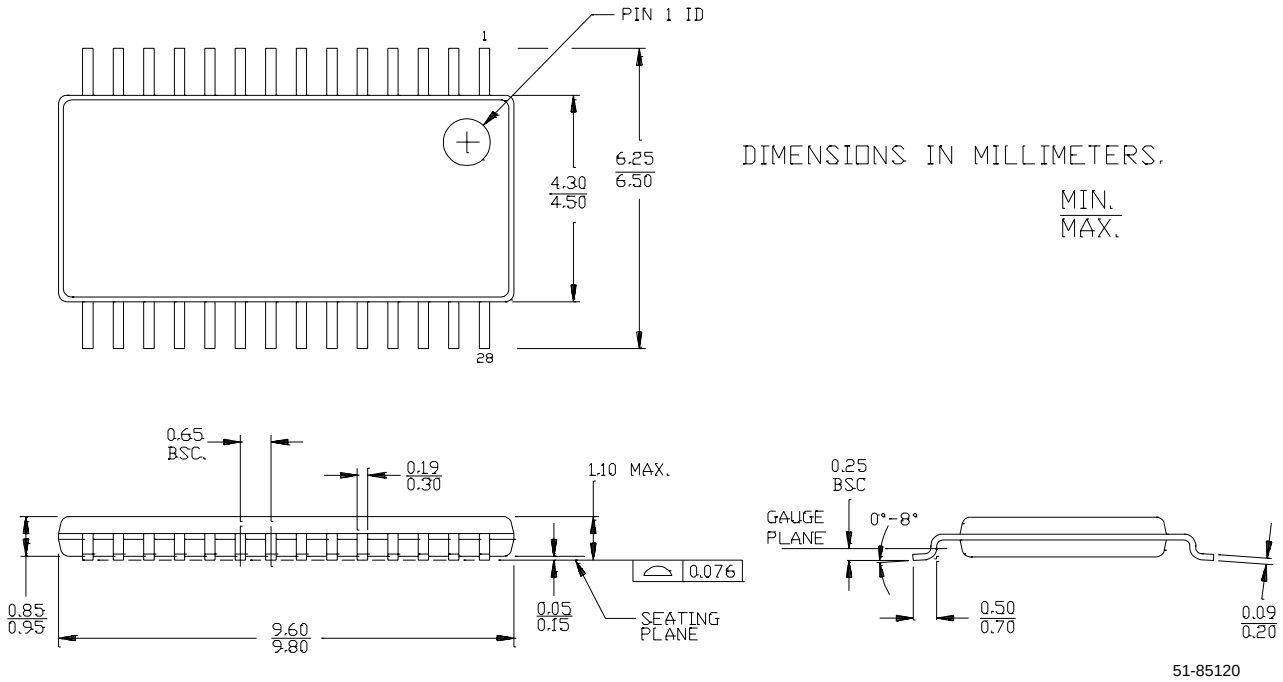
Symbol	Parameter	Value	Tolerance	Unit
R_S	Series Resistor	68	±5%	Ω
R_P	Parallel Resistor	39	±5%	Ω
C_{MID}	AC Ground Capacitor	0.01	±20%	µF

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltages
CY22312ZC	Z29	28-TSSOP	Commercial (T_A=0°C to 70°C)	3.3V

Package Diagram

28-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z29



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111465	03/01/02	JWK	New Data Sheet