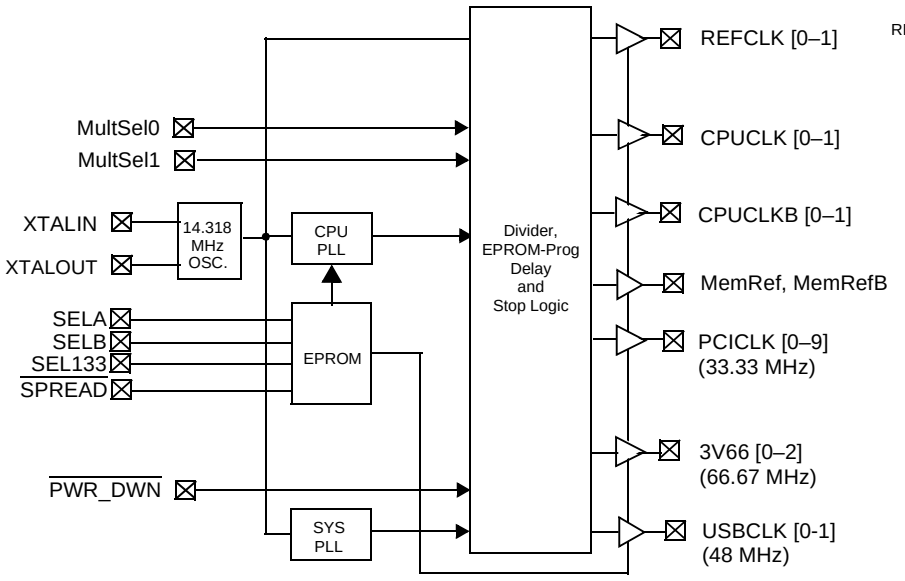
PRELIMINARY

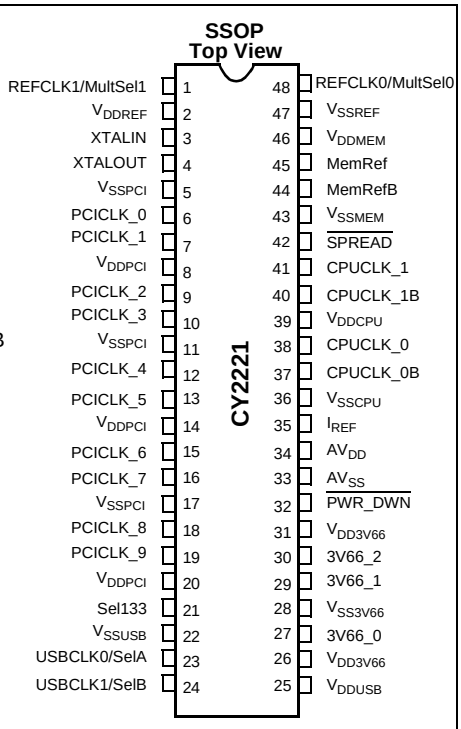
CY2221

133-MHz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs

Features	Benefits
• Compliant to Intel® CK00 Clock Synthesizer/Driver Specifications	Supports next generation Pentium® processors using differential clock drivers
• Multiple output clocks at different frequencies — Two pairs of differential CPU outputs, up to 133 MHz — Ten synchronous PCI clocks — Two MRef clocks, 180 degrees out of phase — Three AGP and Hub Link clocks at 66 MHz — Two 48-MHz clocks — Two reference clocks at 14.318 MHz	Motherboard clock generator — Optimized for single-CPU design — Support for PCI slots and chipset — Drives up to two Direct Rambus™ Clock Generators (DRCG) — Supports USB host controller and SuperI/O chip — Supports ISA slots and I/O chip
• Spread Spectrum clocking — 31 kHz modulation frequency — EPROM programmable percentage of spreading. Default is –0.6%, which is recommended by Intel	Enables reduction of EMI and overall system cost
• Power-down features	Enables ACPI compliant designs
• Three Select inputs	Supports up to eight CPU clock frequencies
• Low-skew and low-jitter outputs	Meets tight system timing requirements at high frequency
• OE and Test Mode support	Enables ATE and “bed of nails” testing
• 48-pin SSOP package	Widely available, standard package enables lower cost

Logic Block Diagram





Pin Summary

Name	Pins	Description
V_{SSREF}	47	3.3V Reference ground
V_{DDREF}	2	3.3V Reference voltage supply
V_{SSPCI}	5, 11, 17	3.3V PCI ground
V_{DDPCI}	8, 14, 20	3.3V PCI voltage supply
V_{SS3V66}	28	3.3V AGP and Hub Link ground
V_{DD3V66}	26, 31	3.3V AGP and Hub Link voltage supply
V_{SSUSB}	22	3.3V USB ground
V_{DDUSB}	25	3.3V USB voltage supply
V_{SSCPU}	36	3.3V CPU ground
V_{DDCPU}	39	3.3V CPU voltage supply
V_{SSMEM}	43	3.3V Memory ground
V_{DDMEM}	46	3.3V Memory voltage supply
AV_{SS}	33	Analog ground for PLL and Core
AV_{DD}	34	Analog voltage supply to PLL and Core
I_{REF}	35	Reference current for external biasing
XTALIN[1]	3	Reference crystal input
XTALOUT[1]	4	Reference crystal feedback
CPUCLK [0–1]	38, 41	CPU clock outputs
CPUCLK [0–1]B	37, 40	Inverse CPU clock outputs
PCICLK [0–9]	6, 7, 9, 10, 12, 13, 15, 16, 18, 19	PCI clock outputs, synchronously running at 33.33 MHz
MemRef	45	MemRef clock output, drives memory clock generator
MemRefB	44	MemRefB clock output 180 degrees out of phase with MemRef
3V66_ [0–2]	27, 29, 30	AGP and Hub Link clock outputs, running at 66 MHz
USBCLK [0–1]/Sel[A–B]	23, 24	Sel [A–B] inputs are sensed then internally latched on power-up before the pins are used for 48-MHz USB clock outputs
REFCLK[0–1]/MultSel[0–1]	1, 48	MultSel[0–1] inputs are sensed then internally latched on power-up before the pins are Reference clock outputs, 14.318 MHz
$\overline{\text{PWR\_DWN}}$	32	Active LOW input, powers down part when asserted
$\overline{\text{SPREAD}}$[2]	42	Active LOW input, enables spread spectrum when asserted
SEL133	21	CPU frequency select input (See Function Table)

Notes:

1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF. For crystals with different C_{LOAD}, please refer to the application note, “Crystal Oscillator Topics.”
2. After Crystal Oscillator starts and during low period of Xin, if three pulses come on $\overline{\text{SPREAD}}$ part will go into internal test mode.

Function Table[3]

SEL133	SELA	SELB	CPUCLK (MHz)	MemRef (MHz)	3V66CLK (MHz)	PCICLK (MHz)	USBCLK (MHz)	REFCLK (MHz)	Notes:
0	0	0	100	50	66	33	48	14.318	
0	0	1	N/A	N/A	N/A	N/A	N/A	N/A	
0	1	0	N/A	N/A	N/A	N/A	N/A	N/A	
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
1	0	0	133	66	66	33	48	14.318	
1	0	1	N/A	N/A	N/A	N/A	N/A	N/A	
1	1	0	N/A	N/A	N/A	N/A	N/A	N/A	
1	1	1	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	

Note:
3. TCLK is a test clock driven in on the XTALIN input in test mode.

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	100	TBD	TBD
CPUCLK	133	TBD	TBD
USBCLK	48	48.008	167

Swing Select Functions

MultSel0	MultSel1	Board Target	Reference R, I_{REF} =	Output Current	V_{OH} @ Z, Iref = 2.32mA
0	0	60Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 5*Iref	0.71 @ 60
0	0	50Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 5*Iref	0.59 @ 50
0	1	60Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 6*Iref	0.85 @ 60
0	1	50Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 6*Iref	0.71 @ 50
1	0	60Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 4*Iref	0.56 @ 60
1	0	50Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 4*Iref	0.47 @ 50
1	1	60Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 7*Iref	0.99 @ 60
1	1	50Ω	Rr = 475 ± 1%, Iref = 2.32mA	I_{OH} = 7*Iref	0.82 @ 50

Clock Driver Impedances

Buffer Name	V_{DD} Range	Buffer Type	Impedance		
			Minimum Ω	Typical Ω	Maximum Ω
CPUCLK, CPUCLKB		Type X1			
USB, REF	3.135–3.465	Type 3	20	40	60
PCI, 3V66	3.135–3.465	Type 5	12	30	55
MemRef, MemRefB	3.135–3.465	Type 5	12	30	55

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +7.0V

Input Voltage..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature..... +150°C

Package Power Dissipation..... 1W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DDREF}, V_{DDPCI}, AV_{DD}, V_{DD3V66}, V_{DDUSB}, V_{DDCPU}, V_{DDMEM}	3.3V Supply Voltages	3.135	3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_{in}	Input Pin Capacitance		5	pF
C_{XTAL}	XTAL Pin Capacitance		22.5	pF
C_L	Max. Capacitive Load on MemRef, USBCLK, REF PCICLK, 3V66		 20 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = V_{DD}/2		2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Pads			0.8	V
V_{OH}	High-level Output Voltage	MemRef, USB, REF, 3V66	I_{OH} = –1 mA	2.4		V
		PCI	I_{OH} = –1 mA	2.4		V
V_{OL}	Low-level Output Voltage	MemRef, USB, REF, 3V66	I_{OL} = 1 mA		0.4	V
		PCI	I_{OL} = 1 mA		0.55	V
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$		–5	5	µA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$		–5	5	µA
I_{OH}	High-level Output Current	CPU For I_{OH} =6*IRef Configuration	Type X1, V_{OH} = 0.65V	12.9		mA
			Type X1, V_{OH} = 0.74V		14.9	
		USB, REF	Type 3, V_{OH} = 1.00V	–29		
			Type 3, V_{OH} = 3.135V		–23	
		3V66, PCI, MemRef, MemRefB	Type 5, V_{OH} = 1.00V	–33		
			Type 5, V_{OH} = 3.135V		–33	
I_{OL}	Low-level Output Current					mA
		USB, REF	Type 3, V_{OL} = 1.95V	29		
			Type 3, V_{OL} = 0.4V		27	
		3V66, PCI, MemRef, MemRefB	Type 5, V_{OL} =1.95 V	30		
			Type 5, V_{OL} = 0.4V		38	
I_{OZ}	Output Leakage Current	Three-state			10	µA
I_{DD3}	3.3V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V, F_{CPU} = 133 MHz			250	mA
I_{DDPD3}	3.3V Shutdown Current	AV_{DD}/V_{DDQ3} = 3.465V, V_{DD25} = 2.625V			20	mA

Switching Characteristics[4] Over the Operating Range

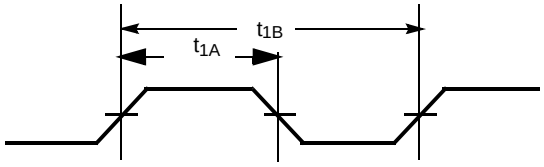
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_{1A}/(t_{1B})$	45	55	%
t_2	CPU	Rise Time	Measured at 20% to 80% of V_{oh}	175	700	ps
t_2	USB, REF	Rising Edge Rate	Between 0.4V and 2.4V	0.5	2.0	V/ns
t_2	PCI, 3V66, MemRef	Rising Edge Rate	Between 0.4V and 2.4V	1.0	4.0	V/ns
t_3	CPU	Fall Time	Measured at 80% to 20% of V_{oh}	175	700	ps
t_3	USB, REF	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	V/ns
t_3	PCI, 3V66, MemRef	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t_4	CPU	CPU-CPU Skew	Measured at Crossover		150	ps
t_5	3V66	3V66-3V66 Skew	Measured at 1.5V		250	ps
t_6	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_7	3V66,PCI	3V66-PCI Clock Skew	3V66 leads. Measured at 1.5V	1.5	3.5	ns
t_8	CPU	Cycle-Cycle Clock Jitter	Measured at Crossover $t_{8 =} t_{8A} – t_{8B}$ With all outputs running		200	ps
t_9	Mref	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		250	ps
t_9	3V66	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		300	ps
t_9	USB	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		350	ps
t_9	PCI	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		500	ps
t_9	REF	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_{9 =} t_{9A} – t_{9B}$		1000	ps
	CPU, PCI	Settle Time	CPU and PCI clock stabilization from power-up		3	ms
	CPU	Rise/Fall Matching	Measured with test loads[6, 7]		20%	
	CPU	Overshoot	Measured with test loads[7]		V_{oh} + 0.2	V
	CPU	Undershoot	Measured with test loads[7]	–0.2		V
V_{oh}	CPU	High-level Output Voltage	Measured with test loads[7]	0.65	0.74	V
V_{ol}	CPU	Low-level Output Voltage	Measured with test loads[7]	0.0	0.05	V
$V_{crossover}$	CPU	Crossover Voltage	Measured with test loads[7]	45% of 0.65	55% of 0.74	V

Notes:

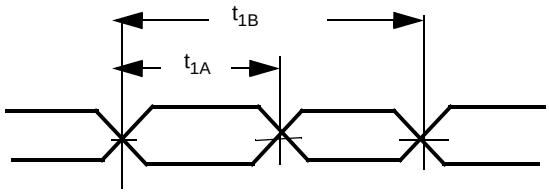
4. All parameters specified with loaded outputs.
5. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
6. Determined as a fraction of 2*(Trp –Trn)/(Trp +Trn) Where Trp is a rising edge and Trp is an intersecting falling edge.
7. The test load is R_s = 33.2Ω, R_p = 49.9Ω in test circuit.

Switching Waveforms

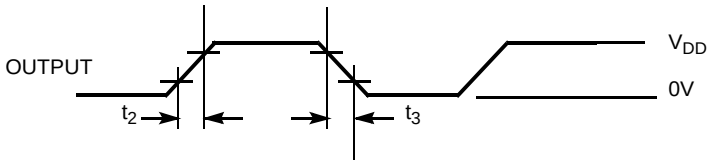
Duty Cycle Timing (Single Ended Output)



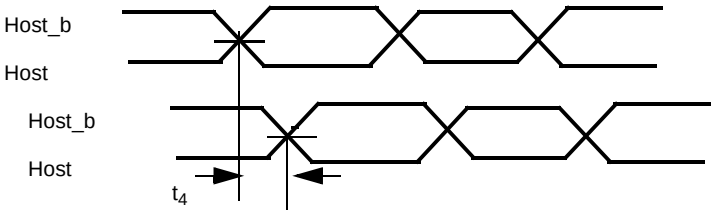
Duty Cycle Timing (CPU Differential Output)



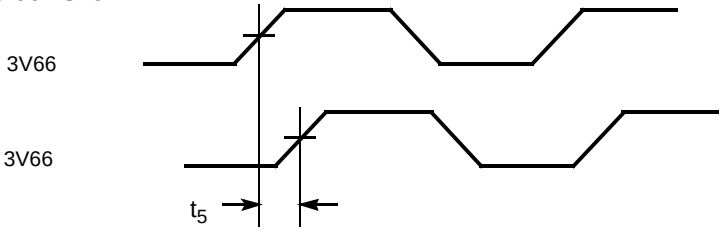
All Outputs Rise/Fall Time



CPU-CPU Clock Skew

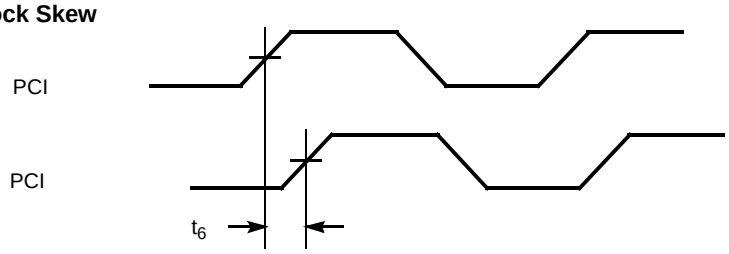


3V66-3V66 Clock Skew

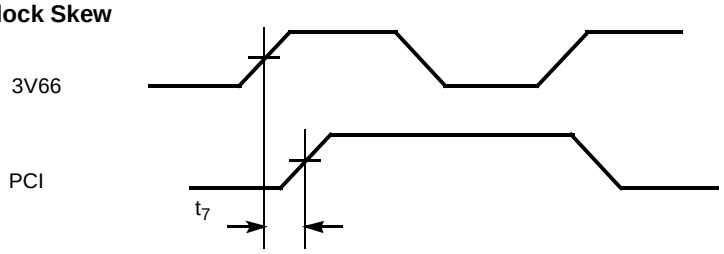


Switching Waveforms (continued)

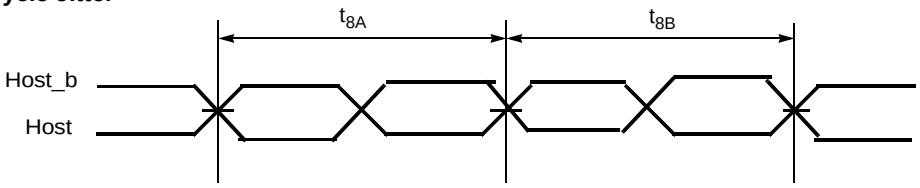
PCI-PCI Clock Skew



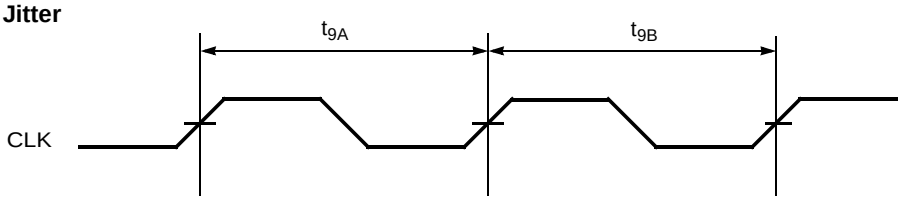
3V66-PCI Clock Skew



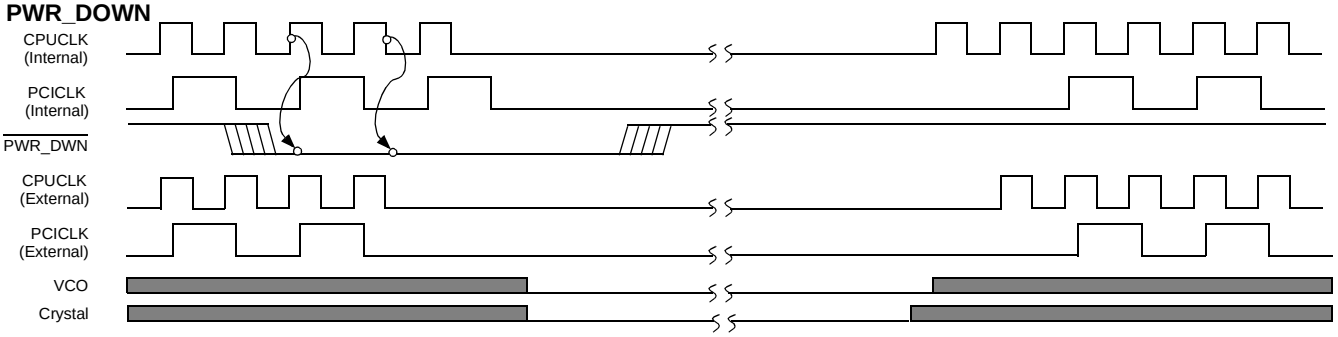
CPU Clock Cycle-Cycle Jitter



Cycle-Cycle Clock Jitter

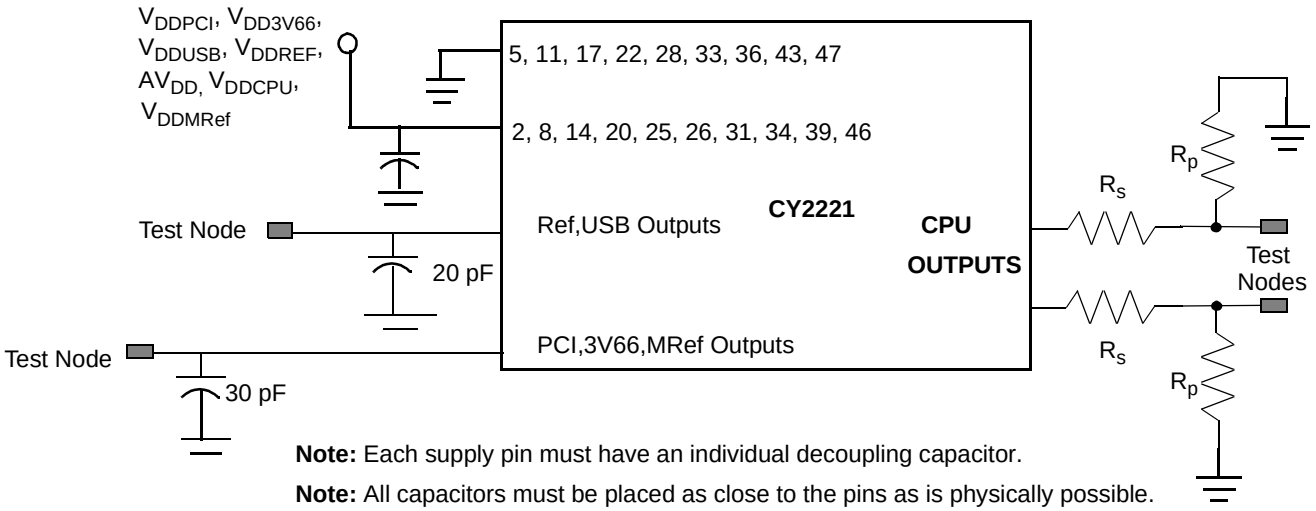


PWR_DOWN



Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Test Circuit



Note: Each supply pin must have an individual decoupling capacitor.

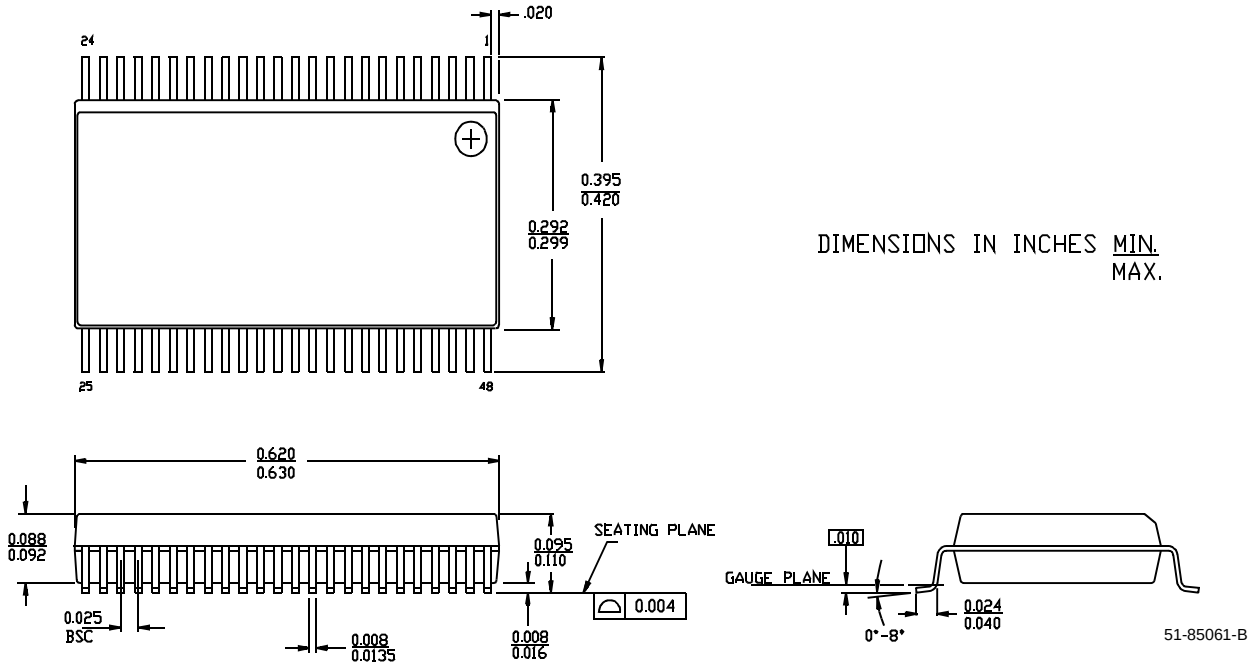
Note: All capacitors must be placed as close to the pins as is physically possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2221PVC–1	O48	48-Pin SSOP	Commercial

Package Diagram

48-Lead Shrunk Small Outline Package O48



Document Title: CY2221 133-Mhz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs Document Number: 38-07212				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110345	10/28/01	SZV	Change from Spec number: 38-00814 to 38-07212