



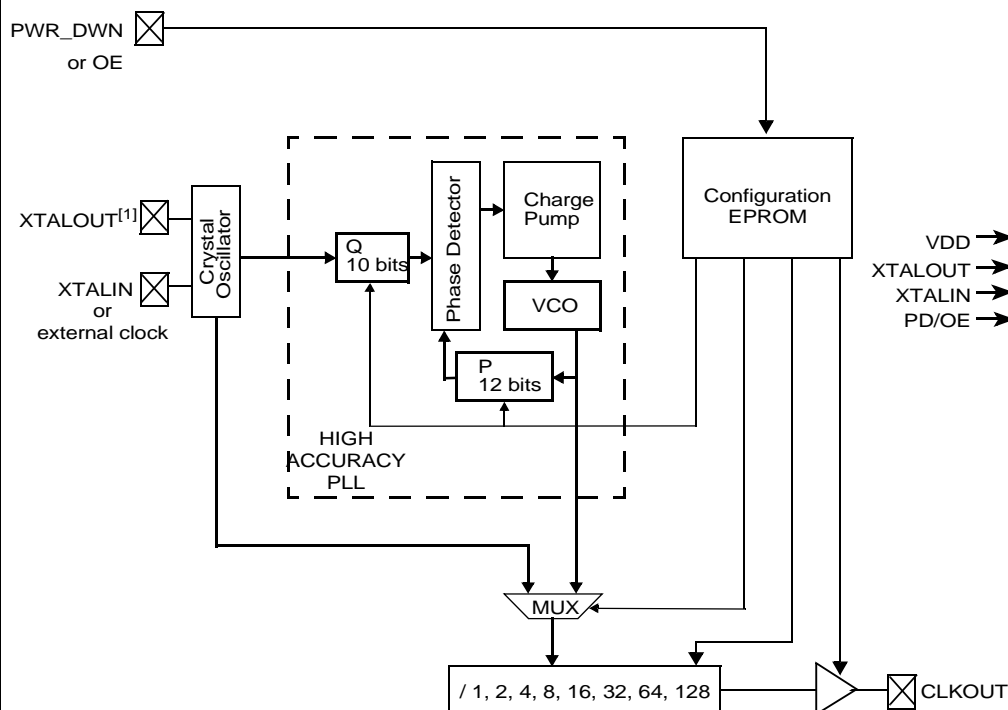
CYPRESS

CY2077

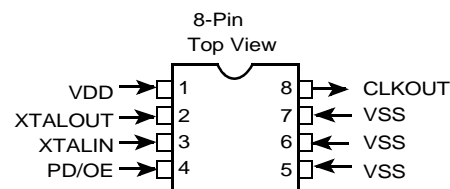
# High-Accuracy EPROM Programmable Single-PLL Clock Generator

Features	Benefits
• High-accuracy PLL with 12-bit multiplier and 10-bit divider	Enables synthesis of highly accurate and stable output clock frequencies with zero PPM
• EPROM-programmability	Enables quick turnaround of custom frequencies
• 3.3V or 5V operation	Supports industry standard design platforms
• Operating frequency — 390 kHz–133 MHz at 5V — 390 kHz–100 MHz at 3.3V	Services most PC, networking, and consumer applications
• Reference input from either a 10–30 MHz fundamental toned crystal or a 1–75 MHz external clock	Lowest cost of oscillator as PLL can be programmed to a high frequency using either a low-frequency, low-cost crystal, or an existing system clock
• EPROM-selectable TTL or CMOS duty-cycle levels	Duty cycle centered at 1.5V or $V_{DD}/2$ Provides flexibility to service most TTL or CMOS applications
• Sixteen selectable post-divide options, using either PLL or reference oscillator/external clock	Provides flexibility in output configurations and testing
• Programmable PWR_DWN or OE pin, with asynchronous or synchronous modes	Enables low-power operation or output enable function and flexibility for system applications, through selectable instantaneous or synchronous change in outputs
• Low jitter outputs typically — 80 ps at 3.3V/5V	Suitable for most PC, consumer, and networking applications
• Controlled rise and fall times and output slew rate	Has lower EMI than oscillators
• Available in both commercial and industrial temperature ranges	Suitable to fit most applications
• Factory-programmable device options	Easy customization and fast turnaround

## Logic Block Diagram



## Pin Configuration



### Note:

1. When using an external clock source, leave XTALOUT floating.

## Functional Description

The CY2077 is an EPROM-programmable, high-accuracy, general-purpose, PLL-based design for use in applications such as modems, disk drives, CD-ROM drives, video CD players, DVD players, games, set-top boxes, and data/telecommunications.

The CY2077 can generate a clock output up to 133 MHz at 5V or 100 MHz at 3.3V. It has been designed to give the customer a very accurate and stable clock frequency with little to zero PPM error. The CY2077 contains a 12-bit feedback counter divider and 10-bit reference counter divider to obtain a very high resolution to meet the needs of stringent design specifications. Furthermore, there are eight output divide options of /1, /2, /4, /8, /16, /32, /64, and /128. The output divider can select between the PLL and crystal oscillator output/external clock, providing a total of 16 different options to add more flexibility in designs. TTL or CMOS duty cycles can be selected.

Power management with the CY2077 is also very flexible. The user may choose either a PWR\_DWN or an OE feature with which both have integrated pull-up resistors. PWR\_DWN and OE signals can be programmed to have asynchronous and synchronous timing with respect to the output signal. There is a weak pull-down on the output that will pull CLKOUT LOW when either the PWR\_DWN or OE signal is active. This weak pull-down can easily be overridden by another clock signal in designs where multiple clock signals share a signal path.

Multiple options for output selection, better power distribution layout, and controlled rise and fall times enable the CY2077 to be used in applications that require low jitter and accurate reference frequencies.

## EPROM Configuration Block

Table 1 summarizes the features configurable by EPROM.

**Table 1. EPROM Adjustable Features**

EPROM Adjustable Features	
Adjust Freq.	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
Duty cycle levels (TTL or CMOS)	
Power management mode (OE or PWR_DWN)	
Power management timing (synchronous or asynchronous)	

## Pin Summary

Name	Pin	Description
V <sub>DD</sub>	1	Voltage supply.
V <sub>SS</sub>	5,6,7	Ground (all the pins have to be grounded).
X <sub>D</sub>	2	Crystal output (leave this pin floating when external reference is used).
X <sub>G</sub>	3	Crystal input or external input reference.
PWR_DWN / OE	4	EPROM programmable power-down or output enable pin. Weak pull-up.
CLKOUT	8	Clock output. Weak pull-down.

### Note:

- When using CyClocks, please note that the PLL frequency range is from 50 MHz to 250 MHz for 5V V<sub>DD</sub> supply, and 50 MHz to 180 MHz for 3V V<sub>DD</sub> supply. The output frequency is determined by the selected output divider.

## PLL Output Frequency

The CY2077 contains a high-resolution PLL with 12-bit multiplier and 10-bit divider.<sup>[2]</sup> The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \cdot (P + 5)}{(Q + 2)} \cdot F_{REF}$$

where P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

The calculation of P and Q values for a given PLL output frequency is handled by the CyClocks™ software. Refer to the "Custom Configuration Request Procedure" section for details.

## Power Management Features

PWR\_DWN and OE options are configurable by EPROM programming for the CY2077. In PWR\_DWN mode, all active circuits are powered down when the control pin is set LOW. When the control pin is set back HIGH, both the PLL and oscillator circuit must re-lock. In the case of OE, the output is three-stated and weakly pulled down when the control pin is set LOW. The oscillator and PLL are still active in this state, which leads to a quick clock output return when the control pin is set back HIGH.

Additionally, PWR\_DWN and OE can be configured to occur asynchronously or synchronously with respect to CLKOUT. In asynchronous mode, PWR\_DWN or OE disables CLKOUT immediately (allowing for logic delays), without respect to the current state of CLKOUT. Synchronous mode will prevent output glitches by waiting for the next falling edge of CLKOUT after PWR\_DWN or OE becomes asserted. In either asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of CLKOUT.

**Device Functionality: Output Frequencies**

Symbol	Description	Condition	Min.	Max.	Unit
Fo	Output frequency	$V_{DD} = 4.5 - 5.5V$	0.39	133	MHz
		$V_{DD} = 3.0 - 3.6V$	0.39	100	MHz

**Absolute Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... -0.5 to +7.0V

Input Voltage ..... -0.5V to  $V_{DD} + 0.5V$

Storage Temperature (Non-Condensing) ... -55°C to +150°C

Junction Temperature ..... 150°C

Static Discharge Voltage .....  $\geq 2000V$   
(per MIL-STD-883, Method 3015)

**Operating Conditions for Commercial Temperature Device**

Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage	3.0	5.5	V
$T_A$	Operating Temperature, Ambient	0	+70	°C
$C_{TTL}$	Max. Capacitive Load on outputs for TTL levels			
	$V_{DD} = 4.5 - 5.5V$ , Output frequency = 1 – 40 MHz		50	pF
	$V_{DD} = 4.5 - 5.5V$ , Output frequency = 40 – 125 MHz		25	pF
	$V_{DD} = 4.5 - 5.5V$ , Output frequency = 125 – 133 MHz		15	pF
$C_{CMOS}$	Max. Capacitive Load on outputs for CMOS levels			
	$V_{DD} = 4.5 - 5.5V$ , Output frequency = 1 – 40 MHz		50	pF
	$V_{DD} = 4.5 - 5.5V$ , Output frequency = 40 – 125 MHz		25	pF
	$V_{DD} = 4.5 - 5.5V$ , Output frequency = 125 – 133 MHz		15	pF
	$V_{DD} = 3.0 - 3.6V$ , Output frequency = 1 – 40 MHz		30	pF
	$V_{DD} = 3.0 - 3.6V$ , Output frequency = 40 – 100 MHz		15	pF
$X_{REF}$	Reference Frequency, input crystal with $C_{load} = 10$ pF	10	30	MHz
	Reference Frequency, external clock source	1	75	MHz

**Electrical Characteristics  $T_A = 0^\circ C$  to  $+70^\circ C$** 

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Low-level Input Voltage	$V_{DD} = 4.5 - 5.5V$ $V_{DD} = 3.0 - 3.6V$			0.8 $0.2V_{DD}$	V V
$V_{IH}$	High-level Input Voltage	$V_{DD} = 4.5 - 5.5V$ $V_{DD} = 3.0 - 3.6V$	2.0 $0.7V_{DD}$			V V
$V_{OL}$	Low-level Output Voltage	$V_{DD} = 4.5 - 5.5V$ , $I_{OL} = 16$ mA $V_{DD} = 3.0 - 3.6V$ , $I_{OL} = 8$ mA			0.4 0.4	V V
$V_{OHCMOS}$	High-level Output Voltage, CMOS levels	$V_{DD} = 4.5 - 5.5V$ , $I_{OH} = -16$ mA $V_{DD} = 3.0 - 3.6V$ , $I_{OH} = -8$ mA	$V_{DD} - 0.4$ $V_{DD} - 0.4$			V V
$V_{OHTTL}$	High-level Output Voltage, TTL levels	$V_{DD} = 4.5 - 5.5V$ , $I_{OH} = -8$ mA	2.4			V
$I_{IL}$	Input Low Current	$V_{IN} = 0V$			10	$\mu A$
$I_{IH}$	Input High Current	$V_{IN} = V_{DD}$			5	$\mu A$
$I_{DD}$	Power Supply Current, Unloaded	$V_{DD} = 4.5 - 5.5V$ , Output frequency $\leq 133$ MHz $V_{DD} = 3.0 - 3.6V$ , Output frequency $\leq 100$ MHz			45 25	mA mA
$I_{DDS}^{[3]}$	Stand-by current (PD = 0)	$V_{DD} = 4.5 - 5.5V$ $V_{DD} = 3.0 - 3.6V$		25 10	100 50	$\mu A$
$R_{UP}$	Input Pull-Up Resistor	$V_{DD} = 4.5 - 5.5V$ , $V_{IN} = 0V$ $V_{DD} = 4.5 - 5.5V$ , $V_{IN} = 0.7V_{DD}$	1.1 50	3.0 100	8.0 200	M $\Omega$ k $\Omega$
$I_{OE\_CLKOUT}$	CLKOUT Pulldown current	$V_{DD} = 5.0$		20		$\mu A$

**Note:**

3. If external reference is used, it is required to stop the reference (set reference to LOW) during power down.

**Output Clock Switching Characteristics Commercial** Over the Operating Range<sup>[4]</sup>

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$t_{1w}$	Output Duty Cycle at 1.4V, $V_{DD} = 4.5 - 5.5V$ $t_{1w} = t_{1A} \div t_{1B}$	1 – 40 MHz, $C_L \leq 50$ pF 40 – 125 MHz, $C_L \leq 25$ pF 125 – 133 MHz, $C_L \leq 15$ pF	45 45 45		55 55 55	% % %
$t_{1x}$	Output Duty Cycle at $V_{DD}/2$ , $V_{DD} = 4.5 - 5.5V$ $t_{1x} = t_{1A} \div t_{1B}$	1 – 40 MHz, $C_L \leq 50$ pF 40 – 125 MHz, $C_L \leq 25$ pF 125 – 133 MHz, $C_L \leq 15$ pF	45 45 45		55 55 55	% % %
$t_{1y}$	Output Duty Cycle at $V_{DD}/2$ , $V_{DD} = 3.0 - 3.6V$ $t_{1y} = t_{1A} \div t_{1B}$	1 – 40 MHz, $C_L \leq 30$ pF 40 – 100 MHz, $C_L \leq 15$ pF	45 40		55 60	% %
$t_2$	Output Clock Rise Time	Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 50$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 25$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 15$ pF Between 0.2V <sub>DD</sub> – 0.8V <sub>DD</sub> , $V_{DD} = 4.5V - 5.5V$ , $C_L = 50$ pF Between 0.2V <sub>DD</sub> – 0.8V <sub>DD</sub> , $V_{DD} = 3.0V - 3.6V$ , $C_L = 30$ pF Between 0.2V <sub>DD</sub> – 0.8V <sub>DD</sub> , $V_{DD} = 3.0V - 3.6V$ , $C_L = 15$ pF			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
$t_3$	Output Clock Fall Time	Between 0.8V – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 50$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 25$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 15$ pF Between 0.2V <sub>DD</sub> – 0.8V <sub>DD</sub> , $V_{DD} = 4.5V - 5.5V$ , $C_L = 50$ pF Between 0.2V <sub>DD</sub> – 0.8V <sub>DD</sub> , $V_{DD} = 3.0V - 3.6V$ , $C_L = 30$ pF Between 0.2V <sub>DD</sub> – 0.8V <sub>DD</sub> , $V_{DD} = 3.0V - 3.6V$ , $C_L = 15$ pF			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
$t_4$	Start-Up Time Out of Power-Down	PWR_DWN pin LOW to HIGH <sup>[5]</sup>		1	2	ms
$t_{5a}$	Power-Down Delay Time (synchronous setting)	PWR_DWN pin LOW to output LOW (T= period of output CLK)		T/2	T + 10	ns
$t_{5b}$	Power-Down Delay Time (asynchronous setting)	PWR_DWN pin LOW to output LOW		10	15	ns
$t_6$	Power-Up Time	From power-on <sup>[5]</sup>		1	2	ms
$t_{7a}$	Output Disable Time (synchronous setting)	OE pin LOW to output high-Z (T= period of output clk)		T/2	T + 10	ns
$t_{7b}$	Output Disable Time (asynchronous setting)	OE pin LOW to output high-Z		10	15	ns
$t_8$	Output Enable Time (always synchronous enable)	OE pin LOW to HIGH (T= period of output clk)		T	1.5T + 25ns	ns
$t_9$	Peak-to-Peak Period Jitter	$V_{DD} = 3.0V - 3.6V$ , $4.5V - 5.5V$ , $F_o > 33$ MHz, $V_{CO} > 100$ MHz $V_{DD} = 3.0V - 5.5V$ , $F_o < 33$ MHz		80 0.3%	150 1%	ps % of $F_o$

**Notes:**

4. Not all parameters measured in production testing.
5. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70Ω.

**Operating Conditions for Industrial Temperature Device**

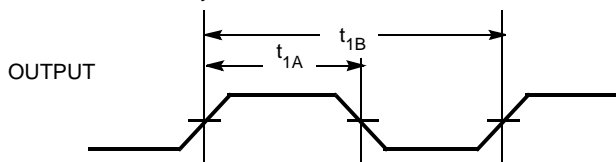
Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage	3.0	5.5	V
$T_A$	Operating Temperature, Ambient	-40	+85	°C
$C_{TTL}$	Max. Capacitive Load on outputs for TTL levels $V_{DD} = 4.5 - 5.5V$ , Output frequency = 1 – 40 MHz $V_{DD} = 4.5 - 5.5V$ , Output frequency = 40 – 125 MHz $V_{DD} = 4.5 - 5.5V$ , Output frequency = 125 – 133 MHz		35 15 10	pF pF pF
$C_{CMOS}$	Max. Capacitive Load on outputs for CMOS levels $V_{DD} = 4.5 - 5.5V$ , Output frequency = 1 – 40 MHz $V_{DD} = 4.5 - 5.5V$ , Output frequency = 40 – 125 MHz $V_{DD} = 4.5 - 5.5V$ , Output frequency = 125 – 133 MHz $V_{DD} = 3.0 - 3.6V$ , Output frequency = 1 – 40 MHz $V_{DD} = 3.0 - 3.6V$ , Output frequency = 40 – 100 MHz		35 15 10 20 10	pF pF pF pF pF
$X_{REF}$	Reference Frequency, input crystal with $C_{load} = 10$ pF	10	30	MHz
	Reference Frequency, external clock source	1	75	MHz

**Electrical Characteristics  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$** 

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Low-level Input Voltage	$V_{DD} = 4.5 - 5.5V$ $V_{DD} = 3.0 - 3.6V$			0.8 $0.2V_{DD}$	V V
$V_{IH}$	High-level Input Voltage	$V_{DD} = 4.5 - 5.5V$ $V_{DD} = 3.0 - 3.6V$	2.0 $0.7V_{DD}$			V V
$V_{OL}$	Low-level Output Voltage	$V_{DD} = 4.5 - 5.5V$ , $I_{OL} = 16$ mA $V_{DD} = 3.0 - 3.6V$ , $I_{OL} = 8$ mA			0.4 0.4	V V
$V_{OHCMOS}$	High-level Output Voltage, CMOS levels	$V_{DD} = 4.5 - 5.5V$ , $I_{OH} = -16$ mA $V_{DD} = 3.0 - 3.6V$ , $I_{OH} = -8$ mA	$V_{DD} - 0.4$ $V_{DD} - 0.4$			V V
$V_{OHTTL}$	High-level Output Voltage, TTL levels	$V_{DD} = 4.5 - 5.5V$ , $I_{OH} = -8$ mA	2.4			V
$I_{IL}$	Input Low Current	$V_{IN} = 0V$			10	$\mu A$
$I_{IH}$	Input High Current	$V_{IN} = V_{DD}$			5	$\mu A$
$I_{DD}$	Power Supply Current, Unloaded	$V_{DD} = 4.5 - 5.5V$ , Output frequency $\leq 133$ MHz $V_{DD} = 3.0 - 3.6V$ , Output frequency $\leq 100$ MHz			45 25	mA mA
$I_{DDS}^{[3]}$	Stand-by current (PD = 0)	$V_{DD} = 4.5 - 5.5V$ $V_{DD} = 3.0 - 3.6V$		25 10	100 50	$\mu A$
$R_{UP}$	Input Pull-Up Resistor	$V_{DD} = 4.5 - 5.5V$ , $V_{IN} = 0V$ $V_{DD} = 4.5 - 5.5V$ , $V_{IN} = 0.7V_{DD}$	1.1 50	3.0 100	8.0 200	M $\Omega$ k $\Omega$
$I_{OE\_CLKOUT}$	CLKOUT Pull-down current	$V_{DD} = 5.0$		20		$\mu A$

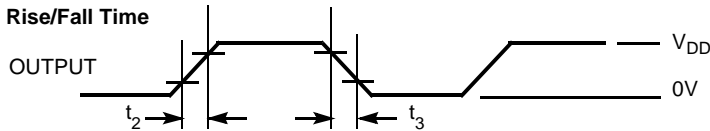
**Output Clock Switching Characteristics Industrial** Over the Operating Range<sup>[4]</sup>

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$t_{1w}$	Output Duty Cycle at 1.4V, $V_{DD} = 4.5 - 5.5V$ $t_{1w} = t_{1A} \div t_{1B}$	1 – 40 MHz, $C_L \leq 35$ pF 40 – 125 MHz, $C_L \leq 15$ pF 125 – 133 MHz, $C_L \leq 10$ pF	45 45 45		55 55 55	% % %
$t_{1x}$	Output Duty Cycle at $V_{DD}/2$ , $V_{DD} = 4.5 - 5.5V$ $t_{1x} = t_{1A} \div t_{1B}$	1 – 40 MHz, $C_L \leq 35$ pF 40 – 125 MHz, $C_L \leq 15$ pF 125 – 133 MHz, $C_L \leq 10$ pF	45 45 45		55 55 55	% % %
$t_{1y}$	Output Duty Cycle at $V_{DD}/2$ , $V_{DD} = 3.0 - 3.6V$ $t_{1y} = t_{1A} \div t_{1B}$	1 – 40 MHz, $C_L \leq 20$ pF 40 – 100 MHz, $C_L \leq 10$ pF	45 40		55 60	% %
$t_2$	Output Clock Rise Time	Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 35$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 15$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 10$ pF Between 0.2 $V_{DD}$ – 0.8 $V_{DD}$ , $V_{DD} = 4.5V - 5.5V$ , $C_L = 35$ pF Between 0.2 $V_{DD}$ – 0.8 $V_{DD}$ , $V_{DD} = 3.0V - 3.6V$ , $C_L = 20$ pF Between 0.2 $V_{DD}$ – 0.8 $V_{DD}$ , $V_{DD} = 3.0V - 3.6V$ , $C_L = 10$ pF			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
$t_3$	Output Clock Fall Time	Between 0.8V – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 35$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 15$ pF Between 0.8 – 2.0V, $V_{DD} = 4.5V - 5.5V$ , $C_L = 10$ pF Between 0.2 $V_{DD}$ – 0.8 $V_{DD}$ , $V_{DD} = 4.5V - 5.5V$ , $C_L = 35$ pF Between 0.2 $V_{DD}$ – 0.8 $V_{DD}$ , $V_{DD} = 3.0V - 3.6V$ , $C_L = 20$ pF Between 0.2 $V_{DD}$ – 0.8 $V_{DD}$ , $V_{DD} = 3.0V - 3.6V$ , $C_L = 10$ pF			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
$t_4$	Start-Up Time Out of Power-Down	PWR_DWN pin LOW to HIGH <sup>[5]</sup>		1	2	ms
$t_{5a}$	Power-Down Delay Time (synchronous setting)	PWR_DWN pin LOW to output LOW (T = period of output clk)		T/2	T+10	ns
$t_{5b}$	Power-Down Delay Time (asynchronous setting)	PWR_DWN pin LOW to output LOW		10	15	ns
$t_6$	Power-Up Time	From power on <sup>[5]</sup>		1	2	ms
$t_{7a}$	Output Disable Time (synchronous setting)	OE pin LOW to output high-Z (T = period of output clk)		T/2	T + 10	ns
$t_{7b}$	Output Disable Time (asynchronous setting)	OE pin LOW to output high-Z		10	15	ns
$t_8$	Output Enable Time (always synchronous enable)	OE pin LOW to HIGH (T = period of output clk)		T	1.5T + 25ns	ns
$t_9$	Peak-to-Peak Period Jitter	$V_{DD} = 3.0V - 3.6V$ , $4.5V - 5.5V$ , $F_o > 33$ MHz, $V_{CO} > 100$ MHz $V_{DD} = 3.0V - 5.5V$ , $F_o < 33$ MHz		80 0.3%	150 1%	ps % of $F_o$

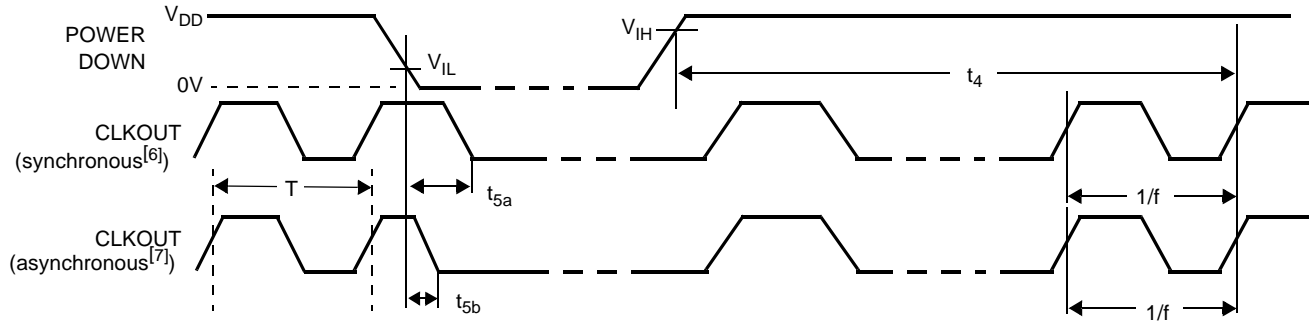
**Switching Waveforms**
**Duty Cycle Timing ( $t_{1w}$ ,  $t_{1x}$ ,  $t_{1y}$ )**


## Switching Waveforms (continued)

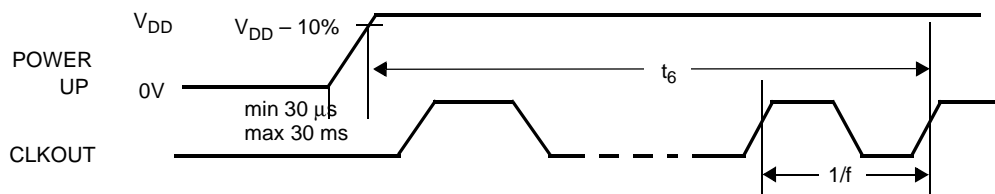
### Output Rise/Fall Time



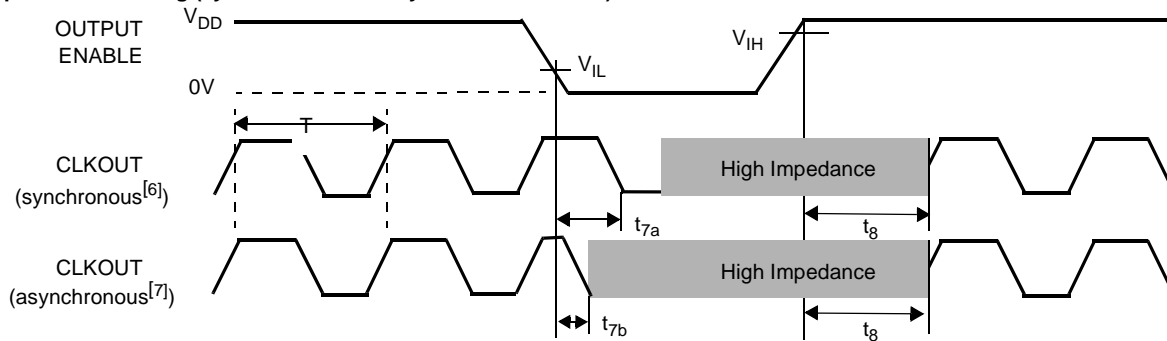
### Power-Down Timing (synchronous and asynchronous modes)



### Power-Up Timing



### Output Enable Timing (synchronous and asynchronous modes)



## Custom Configuration Request Procedure

The CY2077 is an EPROM-programmable device that is configured in the factory. The output frequencies requested will be matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress Field Application Engineer (FAE) or sales representative. The method to use to request custom configurations is: Use CyClocks software of version 3.65 or greater. This software automatically calculates the output frequencies that can be generated by the CY2077 devices and provides a print-out

of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative. The CyClocks software is available free of charge from the Cypress website (<http://www.cypress.com>) or from your local sales representative.

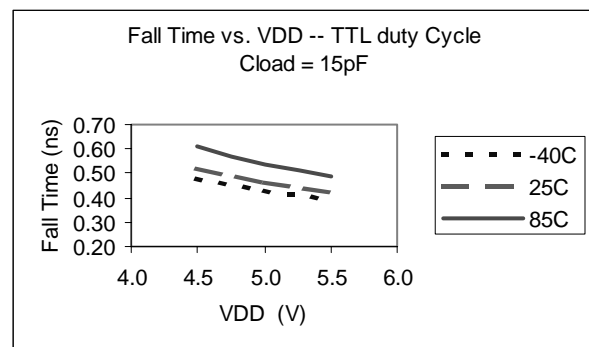
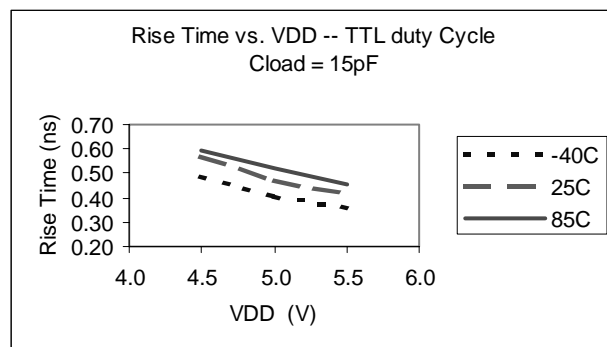
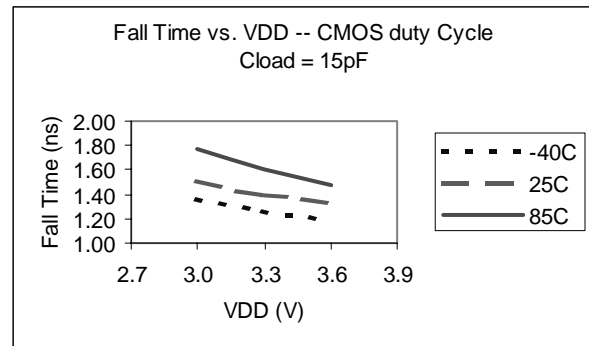
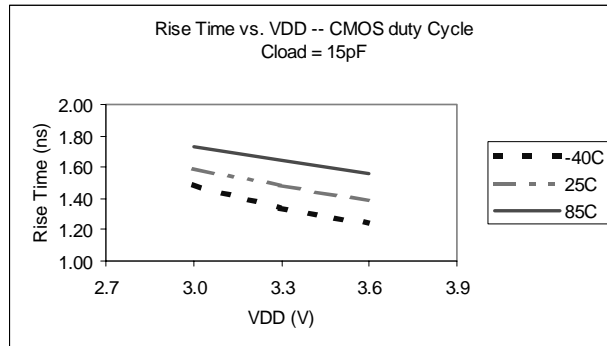
Once the custom request has been processed you will receive a part number with a 3-digit extension (e.g., CY2077SC-103) specific to the frequencies and pinout of your device. This will be the part number used for samples requests and production orders.

### Notes:

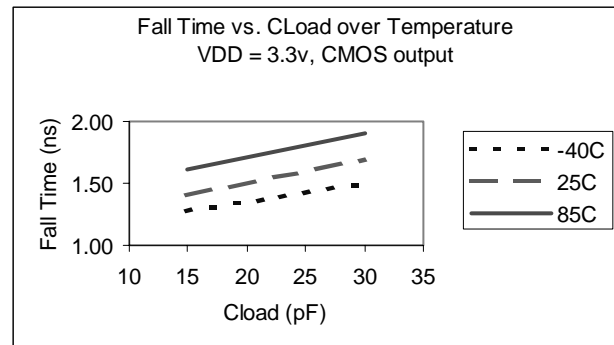
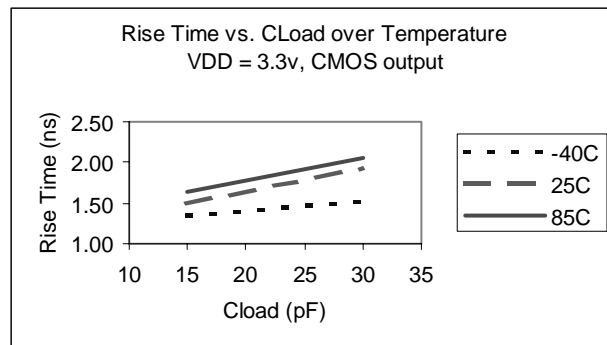
6. In synchronous mode the power-down or output three-state is not initiated until the next falling edge of the output clock.
7. In asynchronous mode the power-down or output three-state occurs within 25 ns irrespective of position in the output clock cycle.

### Typical Rise Time<sup>[8]</sup> and Fall Time<sup>[8]</sup> Trends for CY2077

Rise/Fall Time vs.  $V_{DD}$  over Temperatures



Rise/Fall Time vs. Output Loads over Temperatures



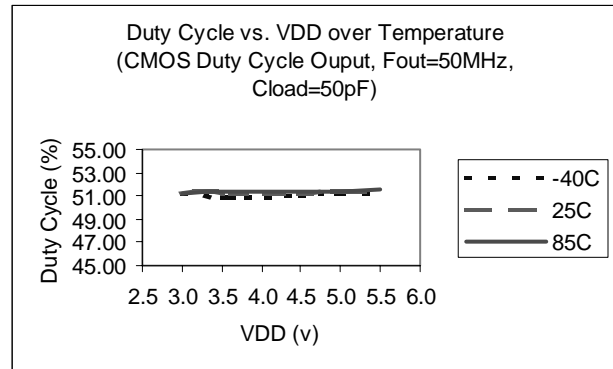
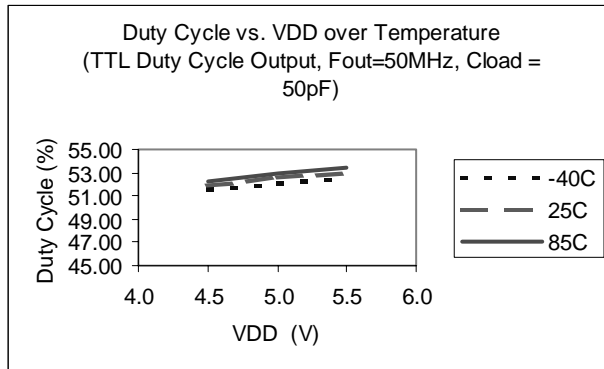
**Note:**

8. Rise/Fall Time for CMOS output is measured between  $1.2 V_{DD}$  and  $0.8 V_{DD}$ . Rise/Fall Time for TTL output is measured between 0.8V and 2.0V.

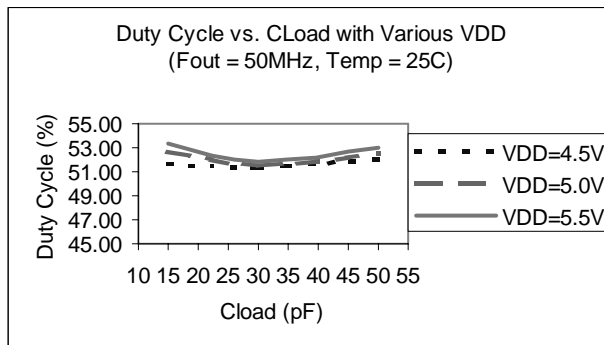


### Typical Duty Cycle<sup>[9]</sup> Trends for CY2077

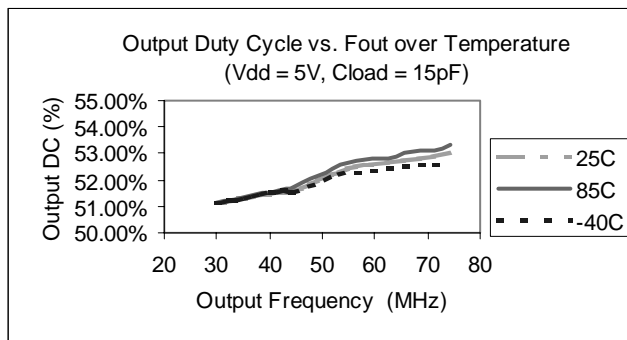
Duty Cycle vs.  $V_{DD}$  over Temperatures



Duty Cycle vs. Output Load



Duty Cycle vs. Output Frequency over Temperatures

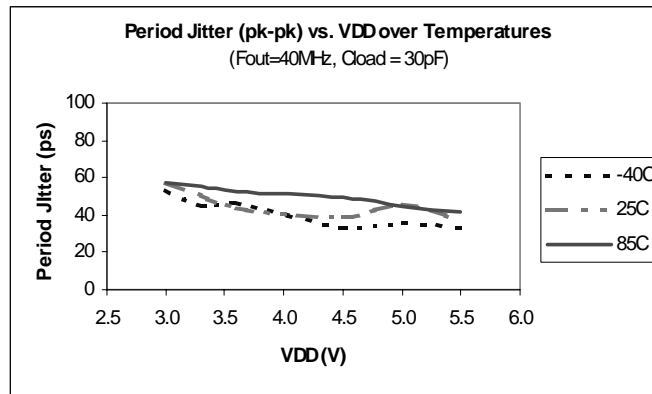


**Note:**

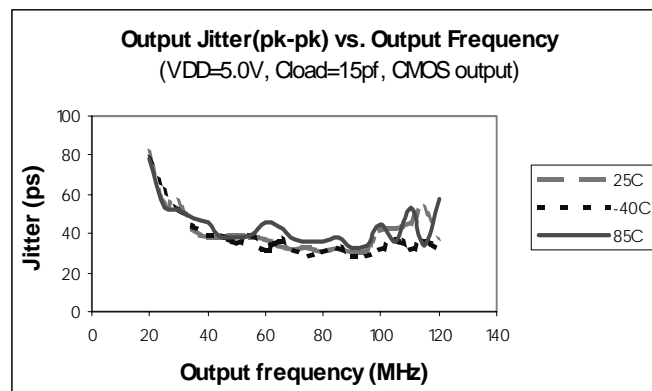
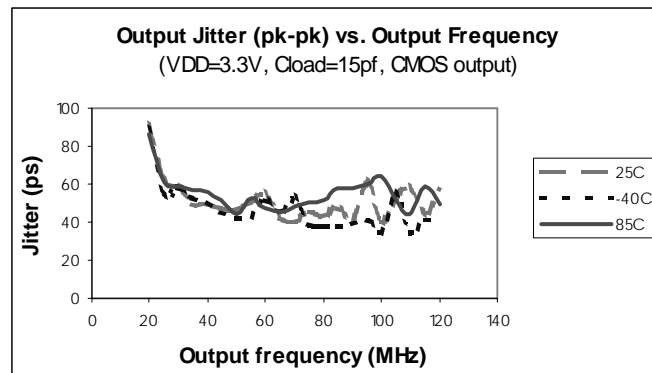
9. Duty cycle is measured at 1.4V for TTL output and 0.5  $V_{DD}$  for CMOS output.

### Typical Jitter Trends for CY2077

Period Jitter (pk-pk) vs.  $V_{DD}$  over Temperatures

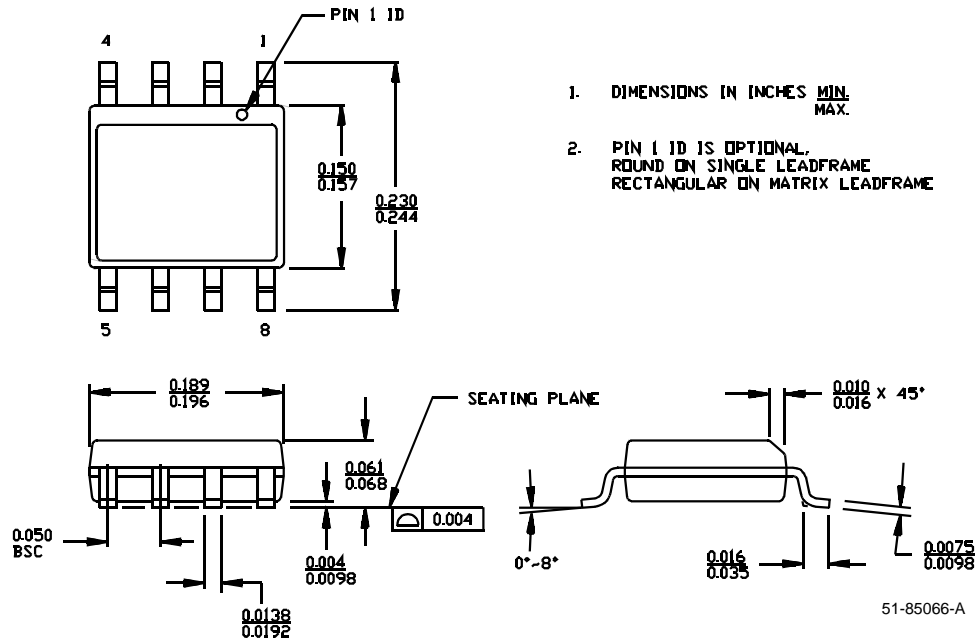


### Period Jitter (pk-pk) vs. Output Frequency over Temperatures

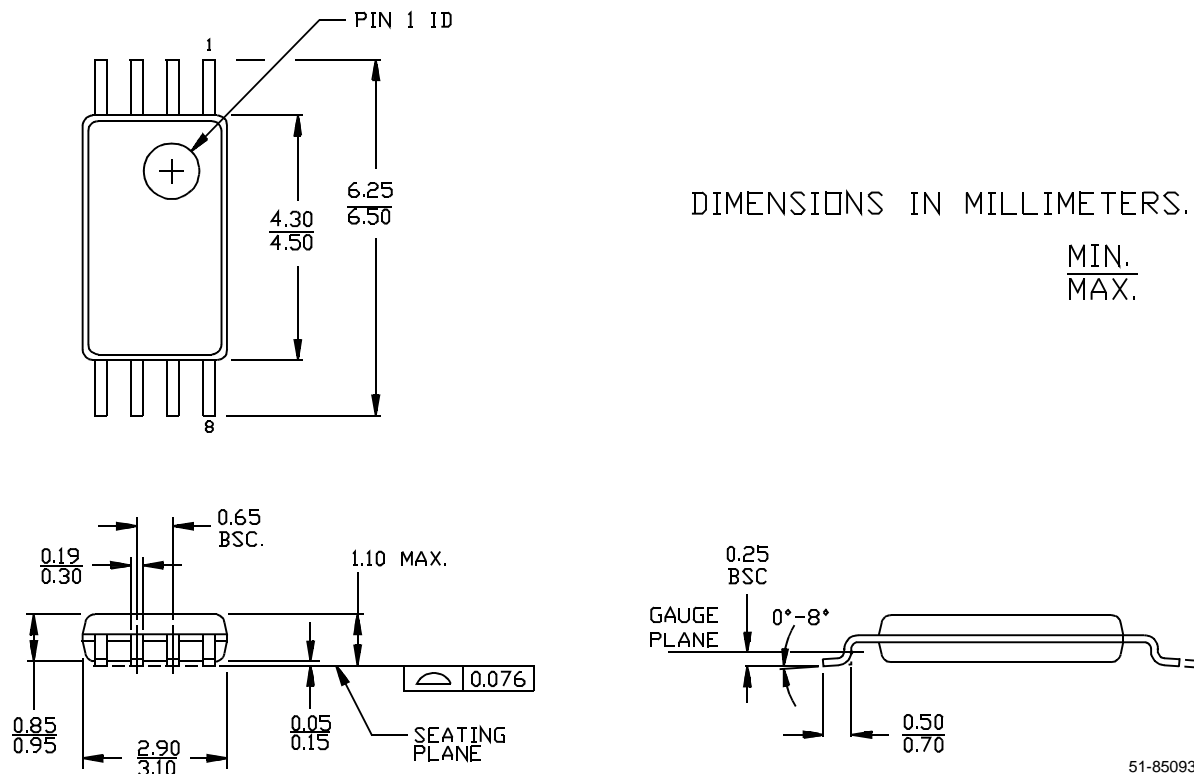


## Package Diagrams

**8-Lead (150-Mil) SOIC S8**



**8-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z8**



CyClocks is a trademark of Cypress Semiconductor. All product or company names mentioned in this document are the trademarks of their respective holders.

**Revision History**

<b>Document Title: CY2077 High-Accuracy EPROM Programmable Single-PLL Clock Generator</b> <b>Document Number: 38-07210</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	111727	02/07/02	DSG	Convert from Spec number: 38-01009 to 38-07210