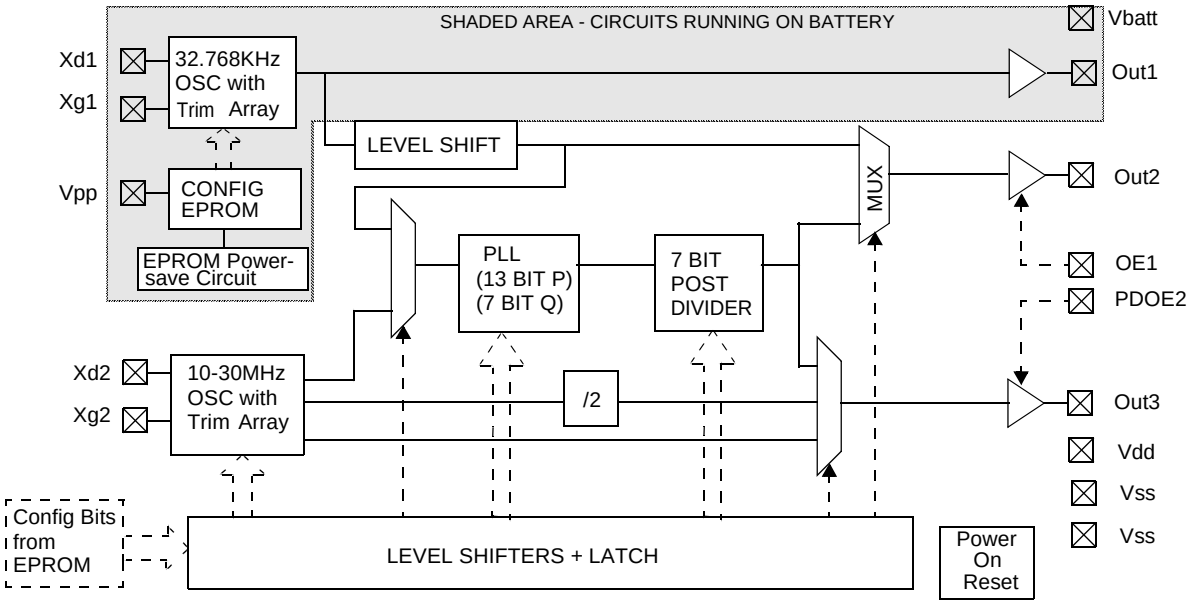
Programmable Clock Die With Precision 32-kHz Input

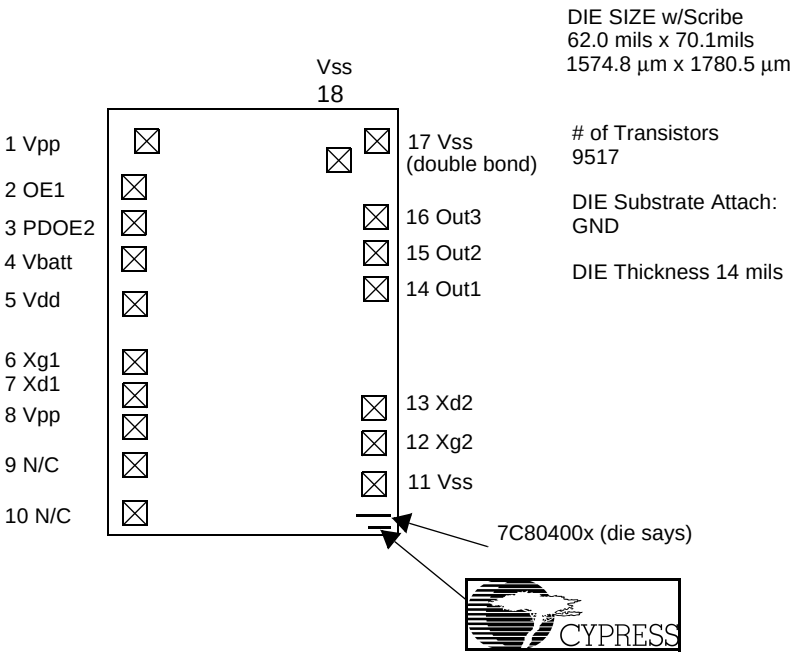
Features	Benefits
• **3 Clock outputs**	Maximize value
• **32.768 kHz**	Precision RTC; CPU clock (powerdown mode), DRAM refresh
• **1 MHz–66 MHz output**	User selectable output frequency
• **Two Control inputs**	Output Enables for Out2 and Out3

Logic Block Diagram



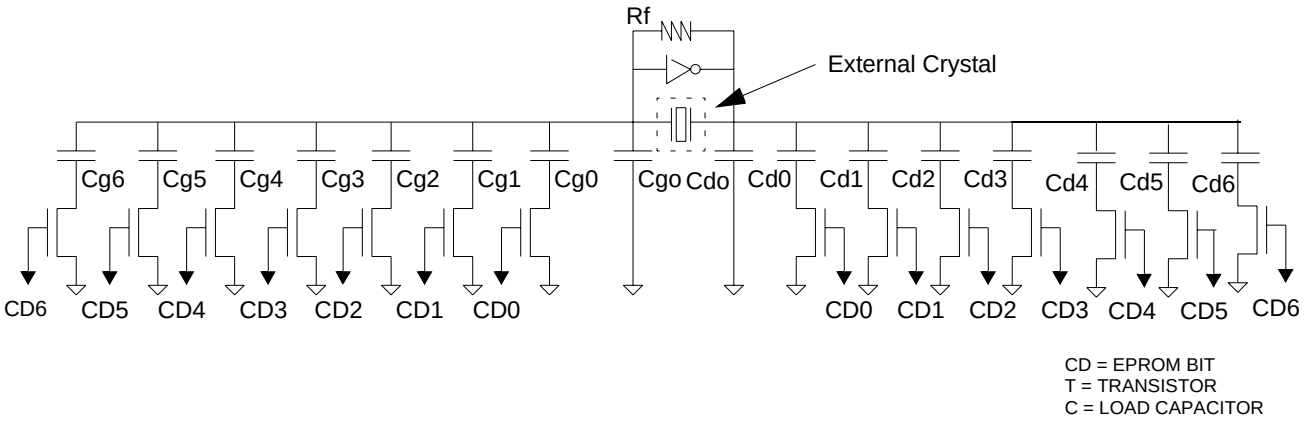
PAD Configurations

CY2040WAF



PAD	I/O	Description
1	Vpp	Vpp for programming, NC when in normal operating mode, Pad 1 and 8 are shorted on die
2	OE1	Out2 Control Pin - Out2 is disabled (HiZ) when LOW
3	PDOE2	EPROM Programmable Powerdown OR Output enable Pin - Out3 is disabled (HiZ) when LOW (OE function). Part is powered down when LOW (PD function)
4	Vbatt	Battery supply or backup power source (2.5V to 3.6V)
5	Vdd	Main VDD (2.7V–5.5V) (Vbatt has to be present when main Vdd is present)
6	Xg1	32.768-kHz Xtal Pin
7	Xd1	32.768-kHz Xtal Out Pin
8	Vpp	Vpp for programming, NC when in normal operating mode. Pins 1 and 8 are shorted on die
9	NC	No Connect
10	NC	No Connect
11	Vss	Ground
12	Xg2	10–30 MHz Xtal Pin
13	Xd2	10–30 MHz Xtal Out Pin
14	Out1 Programming	32-kHz output Three-state input when used for programming
15	Out2	32-kHz output OR 1 MHz–66 MHz output from PLL post divider
16	Out3	10–30 MHz Xtal output OR 5–15 MHz Xtal output (with divide-by-2 option) OR PLL post divider output (1 MHz–66 MHz). Output programmable by user
17,18	Vss	Ground (Pad 17 and 18 have to be bonded out to one pin)

32-kHz and 10–30 MHz Crystal Oscillator Tuning Circuits



CD = EPROM BIT
T = TRANSISTOR
C = LOAD CAPACITOR

32-kHz Oscillator Circuit

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
R_F	Feedback Resistor (32-kHz oscillator)	Vbatt = 2.5V to 3.6V, 32-kHz oscillator	15	30	100	MΩ
	Capacitors have ±20% Tolerance					
C_{G0}	Gate Capacitor (32-kHz oscillator)	Include stray capacitance		8		pF
C_{D0}	Drain Capacitor (32-kHz oscillator)	Include stray capacitance		8		pF
$C_{G0,}C_{D0}$	Tuning Cap (32-kHz oscillator)			0.094		pF
$C_{G1,}C_{D1}$	Tuning Cap (32-kHz oscillator)			0.187		pF
$C_{G2,}C_{D2}$	Tuning Cap (32-kHz oscillator)			0.375		pF
$C_{G3,}C_{D3}$	Tuning Cap (32-kHz oscillator)			0.75		pF
$C_{G4,}C_{D4}$	Tuning Cap (32-kHz oscillator)			1.5		pF
$C_{G5,}C_{D5}$	Tuning Cap (32-kHz oscillator)			3		pF
$C_{G6,}C_{D6}$	Tuning Cap (32-kHz oscillator)			6		pF

10–30 MHz Oscillator Circuit

Symbol	Description	Condition	Min.	Typ.	Ma.x	Unit
R_F	Feedback Resistor (10–30 MHz oscillator)	Vdd = 4.5V to 5.5V Vdd = 2.7V to 3.6V, 10–30 MHz oscillator	0.32 0.61	0.62 1.35	1.45 6.1	MΩ MΩ
	Capacitors have ±20% Tolerance					
C_{G0}	Gate capacitor (10–30 MHz oscillator)	Include stray capacitance		13		pF
C_{D0}	Drain Capacitor (10–30 MHz oscillator)	Include stray capacitance		9		pF
C_{G0} C_{D0}	Tuning Cap (10–30 MHz oscillator)			0.27 N/A		pF pF
C_{G1} C_{D1}	Tuning Cap (10–30 MHz oscillator)			0.52 N/A		pF pF
C_{G2} C_{D2}	Tuning Cap (10–30 MHz oscillator)			1.00 N/A		pF pF
C_{G3} C_{D3}	Tuning Cap (10–30 MHz oscillator)			0.7 0.45		pF pF
C_{G4} C_{D4}	Tuning Cap (10–30 MHz oscillator)			1.4 0.85		pF pF
C_{G5} C_{D5}	Tuning Cap (10–30 MHz oscillator)			2.6 1.7		pF pF
C_{G6} C_{D6}	Tuning Cap (10–30 MHz oscillator)			5.0 3.3		pF pF

Device Functionality: Output Frequencies

Parameter	Description	Condition	Min.	Max.	Unit
F_{out1}	Output frequency	Vbatt = 2.5V–3.6V	32.768	32.768	kHz
F_{out2}	Output frequency	Vdd = 2.7V–5.5V	32.768	32.768	kHz
		Vdd = 2.7V–5.5V	1	66	MHz
F_{out3}	Output frequency	Vdd = 2.7V–5.5V	1	66	MHz

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
Vbatt	Supply voltage (Battery or backup supply)	Relative to V_{SS}	–0.5	7.0	V
Vdd	Supply voltage	Relative to V_{SS}	–0.5	7.0	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	Vdd+0.5	V
T_{STOR}	Storage temperature		–55	150	°C
T_J	Junction temperature			150	°C
ESD	Static Discharge voltage	Per MIL-STD-883, Method 3105	2000		V

Operating Conditions (T_J = –10°C to 100°C unless otherwise noted)

Parameter	Description	Condition	Min.	Max.	Unit
Vbatt	Supply voltage (Battery or backup supply)	Relative to V_{SS} For crystal startup, min. voltage = 3.0V	2.5	3.6	V
Vdd	Supply voltage	Relative to V_{SS}	2.7	5.5	V
C_L	Load capacitance	Max. Capacitive Load on out1, out2, and out3		15	pF

DC Characteristics (Vbatt = 2.5V to 3.6V, Vdd = 2.7V to 5.5V, T_J = –10°C to 100°C unless otherwise noted)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage OE Pins	Vdd = 4.5V to 5.5V			0.8	V
		Vdd = 2.7V to 3.6V			0.2 Vdd	
V_{IH}	Input high voltage OE pins	Vdd = 2.7V to 5.5V	2.0			V
I_{IL}	Input low current OE Pins	V_{IN} = 0V		<1	10	µA
I_{IH}	Input high current OE Pins	V_{IN} = Vdd		<1	5	µA
Out1 (Vbatt 2.5V–3.6V)						
V_{OL}	Output low voltage (out1)	Vbatt = 2.5V to 3.6V, I_{OL}= 8 mA			0.4	V
V_{OHC} (CMOS)	Output high voltage CMOS level	Vbatt = 2.5V to 3.6V, I_{OH}= - 8 mA	Vbatt – 0.4			
Out2, Out3 (Vdd 2.7V–5.5V)						
V_{OL}	Output low voltage	Vdd = 4.5V to 5.5V, I_{OL}= 16 mA			0.4	V
		Vdd = 2.7V to 3.6V, I_{OL}= 8 mA			0.4	
V_{OHC} (CMOS)	Output high voltage CMOS level	Vdd = 4.5V to 5.5V, I_{OH}= –16 mA	Vdd – 0.4			V
		Vdd = 2.7V to 3.6V, I_{OH}= –8 mA	Vdd – 0.4			
V_{OHT} (TTL)	Output high voltage, TTL levels	Vdd = 4.5V to 5.5V, I_{OH}= –16 mA	2.4			V
I_{OZ}	Output leakage current (Out2, Out3)	Vdd = 2.7 to 5.5V, with output disabled		1	50	µA
I_{OP_Vdd}	Supply current on Vdd (No load)	Vdd = 4.5 to 5.5V, fout3 = 66 MHz, fout2 = 32.768 kHz			45	mA
		Vdd = 2.7 to 3.6V, fout3 = 66 MHz, fout2 = 32.768 kHz			25	
I_{OP_Vbatt}	Supply current on Vbatt (15-pF load)	Vbatt = 3.3V, T = 25C, Vdd = 0V		5		µA
		Vbatt = 3.6V, T = –10 to 100 C, Vdd = 0 V			10	
R_{UPH}	Pull-up Resistor	OE1, OE2; Vdd = 4.5V to 5.5V, measured V_{IN} = 0.7 Vdd	15	100	200	kΩ
R_{UPL}	Pull-up Resistor	OE1, OE2; Vdd = 4.5V to 5.5V, measured V_{IN} = 0.0V	1.1	3.0	8.0	MΩ
R_{PON}	Parallel equivalent static on resistance	T0–T6	10			kΩ

AC Characteristics (T_J= –10°C to 100°C unless otherwise noted)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Out1 AC Characteristics						
tr1	Out1 Rise time	20% to 80% Vbatt			6.0	ns
tf1	Out1 Fall time	80% to 20% Vbatt			6.0	ns
dc1	Out1 Duty Cycle	32.768 kHz, C_{LT} = 15 pF, measured at Vbatt/2	40		60	%
tj1	Period jitter	32.768 kHz output directly from oscillator			±25	ns
Out2 AC Characteristics						
tr2	Out2 Rise time	Vdd = 4.5V to 5.5V; (0.8V to 2.0V)			2.0	ns
		Vdd = 4.5V to 5.5V; 20% to 80% Vdd			4.0	ns
		Vdd = 2.7V to 3.6V; 20% to 80% Vdd			4.0	ns
tf2	Out2 Fall Time	Vdd = 4.5V to 5.5V; (2.0V to 0.8V),			2.0	ns
		Vdd = 4.5V to 5.5V; 80% to 20% Vdd			4.0	ns
		Vdd = 2.7V to 3.6V; 80% to 20% Vdd			4.0	ns
dc2	Out2 Duty cycle	32.768 kHz, C_{LT} = 15 pF; measured at 1.4 V Vdd = 4.5V to 5.5V	40		60	%
		32.768 kHz, C_{LT} = 15 pF; measured at Vdd/2 Vdd = 4.5V to 5.5V				
		32.768 kHz, C_{LT} = 15 pF; measured at Vdd/2 Vdd = 2.7V to 3.6V				
dc2	Out2 Duty cycle	1 MHz to 66 MHz, C_{LT} = 15 pF; measured at 1.4V; Vdd = 4.5V to 5.5V	45		55	%
		1 MHz to 66 MHz, C_{LT} = 15 pF; measured at Vdd/2; Vdd = 4.5V to 5.5V				
		1 MHz to 66 MHz, C_{LT} = 15 pF; measured at Vdd/2; Vdd = 2.7V to 3.6V	40		60	%
tj2	Period Jitter (32kHz output)	32.768 kHz output directly from oscillator			±25	ns
	Period Jitter (PLL output)	Vdd = 4.5V to 5.5V, Fo > 33 MHz, Fvco>100 MHz, 10–30 MHz input[1]		±75	±125	ps
		Vdd = 2.7V to 3.6V, Fo > 33 MHz, Fvco>100 MHz, 10–30 MHz input[1]		±100	±200	ps
		Vdd = 2.7V to 5.5V, 16 MHz < Fo < 33 MHz 10–30 MHz input[1]			±300	ps
		Vdd = 2.7V to 5.5V, 1 MHz < Fo < 16 MHz 10–30 MHz input[1]			±500	ps
Out3 AC Characteristics						
tr3	Out3 Rise time	Vdd = 4.5V to 5.5V; (0.8V to 2.0V)			2.0	ns
		Vdd = 4.5V to 5.5V; 20% to 80% Vdd			4.0	ns
		Vdd = 2.7V to 3.6V; 20% to 80% Vdd			4.0	ns
tf3	Out3 Fall Time	Vdd = 4.5V to 5.5V; (2.0V to 0.8V),			2.0	ns
		Vdd = 4.5V to 5.5V; 80% to 20% Vdd			4.0	ns
		Vdd = 2.7V to 3.6V; 80% to 20% Vdd			4.0	ns
dc3	Out3 Duty cycle	1 MHz to 66 MHz, C_{LT} = 15 pF; measured at 1.4V; Vdd = 4.5V to 5.5V	45		55	%
		1 MHz to 66 MHz, C_{LT} = 15 pF; measured at Vdd/2; Vdd = 4.5V to 5.5V				
		1 MHz to 66 MHz, C_{LT} = 15 pF; measured at Vdd/2; Vdd = 2.7V to 3.6V	40		60	%

AC Characteristics (T_J= –10°C to 100°C unless otherwise noted) (continued)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
tj3	Period Jitter (Osc. output)	10–30 MHz output directly from oscillator			±125	ps
	Period Jitter (PLL output)	Vdd = 4.5V to 5.5V, Fo > 33 MHz, Fvco > 100 MHz, 10–30MHz input[1]		±75	±125	ps
		Vdd = 2.7V to 3.6V, Fo > 33 MHz, Fvco > 100 MHz, 10–30 MHz input[1]		±100	±200	ps
		Vdd = 2.7V to 5.5V, 16 MHz < Fo < 33 MHz 10–30 MHz input[1]			±300	ps
		Vdd = 2.7V to 5.5V, 1 MHz < Fo < 16 MHz 10–30 MHz input[1]			±500	ps
Other AC Characteristics						
t_{STP}	Power-down delay time; ASYNC	OE pin HIGH to LOW (T = output clock period)		10	25	ns
	Power-down delay time; SYNC	OE pin HIGH to LOW (T = output clock period)		T/2	T+25	ns
t_{PU}	Power-up time (Osc start-up time)	From power-on (min. Vbatt = 3.0V). Decided by 32.768-kHz crystal startup			3	sec
t_{PXZ}	Output disable time; SYNC	OE pin HIGH to LOW (T = output clock period)		T/2	T+25	ns
	Output disable time; ASYNC	OE pin HIGH to LOW		10	25	ns
T_{PZX}	Output enable time; SYNC (always SYNC)	OE pin LOW to HIGH (T = output clock period)		T	1.5T+25	ns
f_O	Output frequency	Out1 (Vbatt = 2.5V to 3.6V)	32.768kHz			Hz
		Out2 (Vdd = 2.7V to 5.5V)	32.768kHz			
		Out3 (Vdd = 2.7V to 5.5V)	1M		66M	
F_{PLL}	PLL frequency	Vdd = 2.7V to 5.5V	60		133	MHz
Crystal oscillator 1 (32.768 kHz)						
F_C	Crystal frequency	Out1		32.768		kHz
D_L	Crystal drive level	At 32.768 kHz, with ESR <= 55 kΩ		0.1	0.5	µW
–R	Negative resistance	At 32.768 kHz		–200		KΩ
Crystal oscillator 2 (10–30 MHz)						
F_C	Crystal frequency	Out2, Out3	10		30	MHz
D_L	Crystal drive level	At 28 MHz, with ESR <= 20 Ω			150	µW
–R	Negative resistance	At 10–30 MHz		–300		Ω

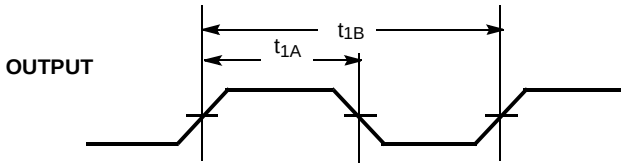
Output Modes (Programmable)[2]

Mode	Out2	Out3
1	32.768 kHz (Level Shifted)	10–30 MHz crystal output
2	32.768 kHz (Level Shifted)	10–30 MHz crystal output divided by 2
3	32.768 kHz (Level Shifted)	PLL
4	PLL	PLL
5	PLL	10–30 MHz crystal output
6	PLL	10–30 MHz crystal output divided by 2

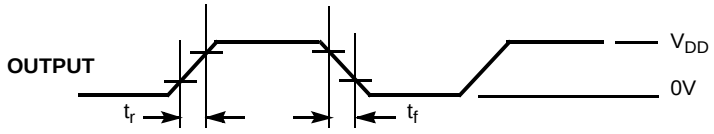
Note:
1. Out2 and Out3 must be at the same frequency for jitter specs to be valid.
2. Refer to the “7C80400 Programming Specification” for details.

Switching Waveforms

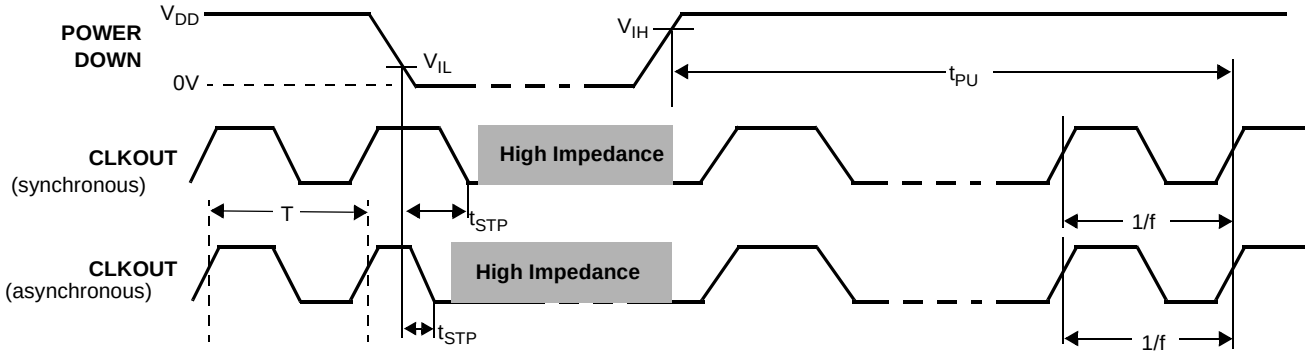
Duty Cycle Timing (dc1, dc2, dc3)



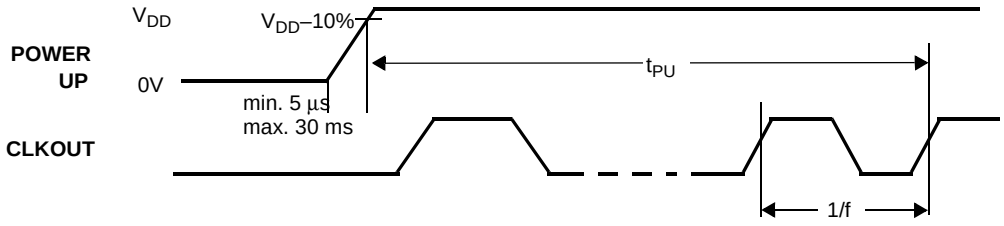
Output Rise/Fall Time



Power Down Timing (synchronous and asynchronous modes)

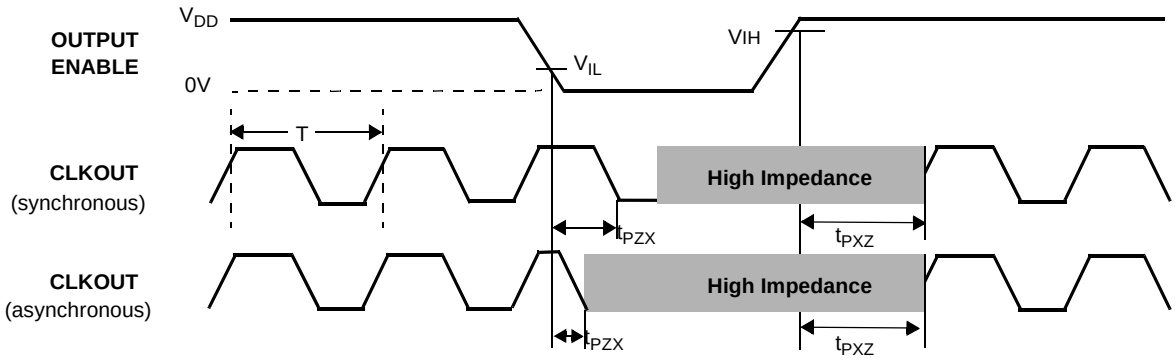


Power Up Timing



Switching Waveforms (continued)

Output Enable Timing (synchronous and asynchronous modes)



Ordering Code	Type	Operating Range
CY2040WAF	Wafer	–10°C to 100°C

Revision History

Document Title: CY2040WAF Programmable Clock Die With Precision 32-kHz Input Document Number: 38-07234				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113051	05/07/02	CKN	New data sheet