B9847

DDR Clock Distribution Buffer/Driver

Features

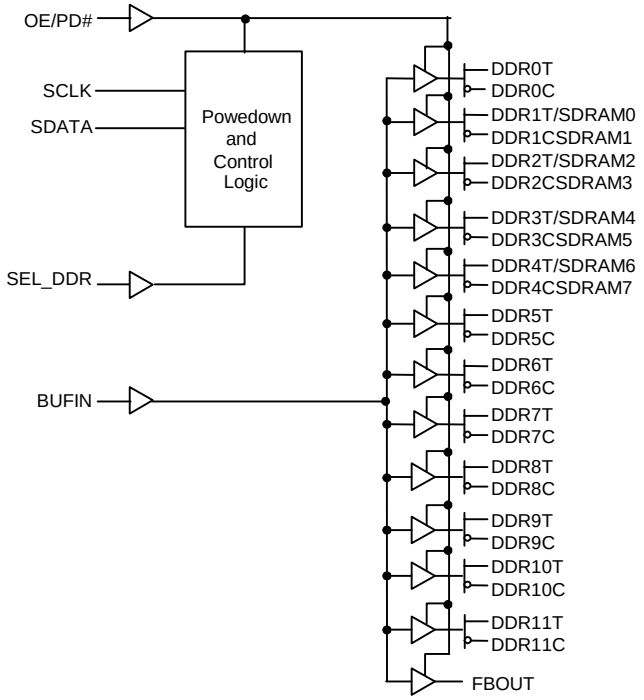
- **Supports 266-MHz DDR SDRAM**
- **Supports VIA Pro 266, PM266, and KT266 Chipsets**
- **Operating Frequency: 60 MHz to 170 MHz**
- **12 Differential or 6 Differential 8 single-ended outputs**
- **Configurable Outputs: Drive 4 DDR DIIMS or 2 DDR DIMMS and 2 SDRAM DIMMS**
- **Spread Spectrum Compatible**
- **Low Jitter (cycle-to-cycle): < 75 ps**
- **Very Low Skew: < 100 ps**
- **Power Management via I^2C Interface and OE#/PD**
- **2.5V and 3.3V Power Supplies**
- **48-Pin SSOP**

Description

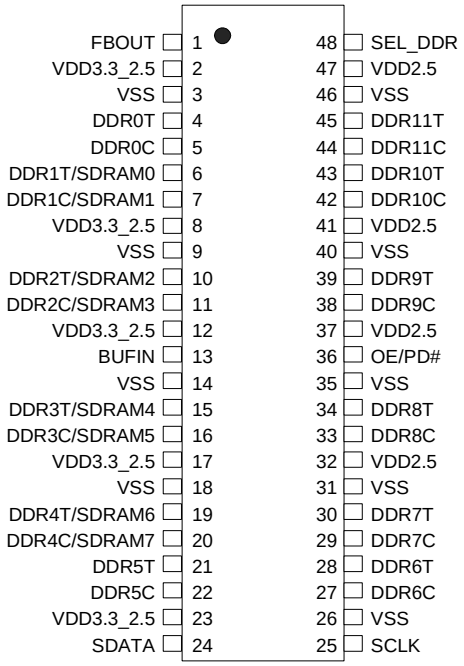
The B9847 is a high-performance, low-skew, low-jitter buffer designed to distribute differential clocks in high-speed applications. The B9847 generates twelve differential pair clock outputs or six differential and eight single-ended clock outputs from one single-ended clock input. The B9847 outputs are configurable to drive four DDR DIMMS or two DDR DIMMS and two SDRAM DIMMS. In addition, the B9847 features a feedback clock output, FBOUT. This output is for the chipset or other B9847 devices and/or one of Cypress's zero-delay buffers. The B9847 is used with C9846 clock synthesizer for the VIA Pro 266 chipset.

The I2C interface enables/disables differential pair outputs. This feature allows flexibility in system power management. The B9847 can also be shut down when PD# is asserted LOW, which drives the outputs LOW.

Block Diagram



Pin Configuration



Pin Description

Pin	Name	PWR	I/O[1]	Description
13	BUFIN		I	Clock Input. 2.5V for DDR-ONLY mode. 3.3V input for standard SDRAM mode.
28, 30, 34, 39, 43, 45	DDR(6:11)T	VDD2.5	O	DDR Clock Outputs
27, 29, 33, 38, 42, 44	DDR(6:11)C	VDD2.5	O	DDR Clock Outputs
4, 6, 10, 15, 19, 21	DDR(0:5)T / SDRAM(0,2,4,6,8, 10)	VDD3.3_2.5	O	DDR/SDRAM Clock Outputs
5, 7,11,16,20, 22	DDR(0:5)C / SDRAM(1,3,5,7,9, 11)	VDD3.3_2.5	O	DDR/SDRAM Clock Outputs
1	FBOUT	VDD3.3_2.5	O	Feedback Clock Output. This clock is for the chipset.
48	SEL_DDR		I, PU	DDR Select Input. When asserted HIGH, DDR-ONLY mode, pins 4, 5, 6, 7, 10, 11, 15, 16, 19, 20, 21, 22, 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44, and 45 are DDR outputs. When set LOW, STANDARD SDRAM mode, pins 6, 7, 10, 11, 15, 16, 19, and 20 are SDRAM outputs. Pins 4, 5, 21, 22, 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44, and 45 are low (off).
36	OE/PD#		I, PU	This is a dual-function pin. If during power-up OE is LOW, then the outputs are three-stated. When OE goes HIGH the outputs are enabled. Once HIGH, this pin becomes a Power Down control (PD#). When PD# is then driven LOW, the outputs will be driven LOW.
25	SCLK		I, PU	Serial Clock Input. Clocks data at SDATA into the internal register.
24	SDATA		I/O, PU	Serial Data Input. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.
2, 8, 12, 17, 23	VDD3.3_2.5			2.5V Power Supply for DDR_ONLY mode. Connect to 3.3V Power Supply.
32, 37, 41, 47	VDD2.5			2.5V Power Supply
3, 9, 14, 18, 26, 31, 35, 40, 46	VSS			Common Ground

Note:
1. PU = Internal Pull-up, typical value of 640KΩ.

A bypass capacitor (0.1 µF) should be placed as close as possible to each positive power pin (<0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Power Management

The individual output enable/disable control of the B9847 allows the user to implement unique power management schemes into the design. Outputs are three-stated when disabled through the I^2C interface as individual bits are set low in Byte6 and Byte7 registers. The enabling and disabling of individual outputs is done in such a manner as to eliminate the possibility of partial “runt” clocks.

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

1. **“Command Code”** byte, and
2. **“Byte Count”** byte.
3. **Byte(0:5) are dummy bytes and are reserved. These bytes should be sent as don’t care.**

See our application note (AN0022) for more details on using the I^2C interface.

Byte 6: Output Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	1	1	FBOUT
3	1	45, 44	DDR11T, DDR11C
2	1	43, 42	DDR10T, DDR10C
1	1	39, 38	DDR9T, DDR9C
0	1	34, 33	DDR8T, DDR8C

Byte 7: Output Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	30, 29	DDR7T, DDR7C
6	1	28, 27	DDR6T, DDR6C
5	1	21, 22	DDR5T DDR5C
4	1	19, 20	DDR4T/SDRAM6, DDR4C/SDRAM7
3	1	15, 16	DDR3T/SDRAM4, DDR3C/SDRAM5
2	1	10, 11	DDR2T/SDRAM2, DDR2C/SDRAM3
1	1	6, 7	DDR1T/SDRAM0, DDR1C/SDRAM1
0	1	4, 5	DDR0T DDR0C

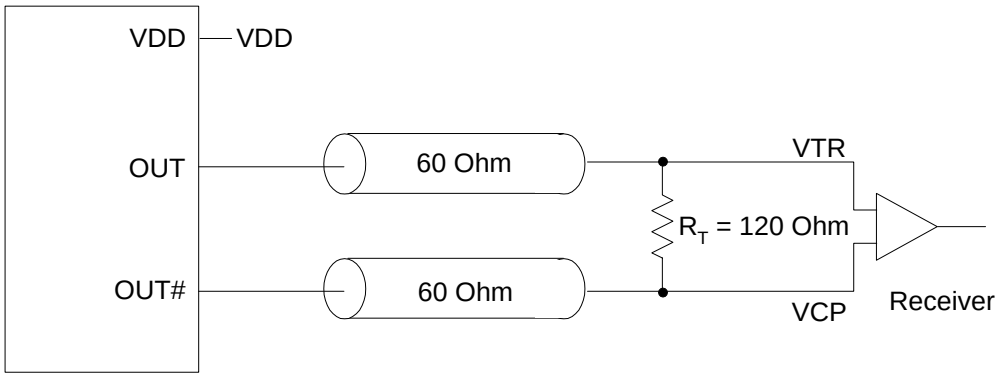


Figure 1. Differential Signal Using Direct Termination Resistor

Maximum Ratings

Input Voltage Relative to V_{SS}:.....V_{SS} – 0.3V

Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to +150°C

Operating Temperature:.....0°C to +70°C

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters[2]: $V_{DD2.5}$ = 2.5V + 5%, $V_{DD3.3\_2.5}$ = 3.3V + 5% or 2.5V + 5%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	SDATA, SCLK		-	1.0	V
V_{IH}	Input High Voltage		2.2	-		V
V_{IL1}	Input Low Voltage	BUFIN, PD#			1.0	
V_{IH1}	Input High Voltage		2.0			
I_{IH}	Input High Current	$V_{IN} = V_{DD}$, BUFIN, PD#			10	µA
I_{IL}	Input Low Current				TBD	µA
I_{OL}	Output Low Current	V_{DD} = 2.375V, V_{OUT} = 1.2V	26	35		mA
I_{OH}	Output High Current	V_{DD} = 2.375V, V_{OUT} = 1V	–18	-32		mA
V_{OL}	Output Low Voltage	V_{DD} = 2.375V, I_{OL} = 12 mA			0.6	V
V_{OH}	Output High Voltage	V_{DD} = 2.375V, I_{OH} = –12 mA	1.7			V
V_{OUT}	Output Voltage Swing[5]		0.7		V_{DD}+0.6	V
V_{OX}	Output Crossing Voltage[6]		(V_{DD}/2) – 0.2	V_{DD}/2	(V_{DD}/2) + 0.2	V
I_{OZ}	High-Impedance Output Current	V_O = GND or V_O=V_{DD}	–10		10	µA
I_{DD}	Dynamic Supply Current[7]	DDR mode, V_{DD} = 2.65 volts, F_O = 133 MHz		187	210	mA
I_{DDS}	Shutdown Supply Current	All V_{DD}				mA
C_{in}	Input Pin Capacitance			5	-	pF

Notes:

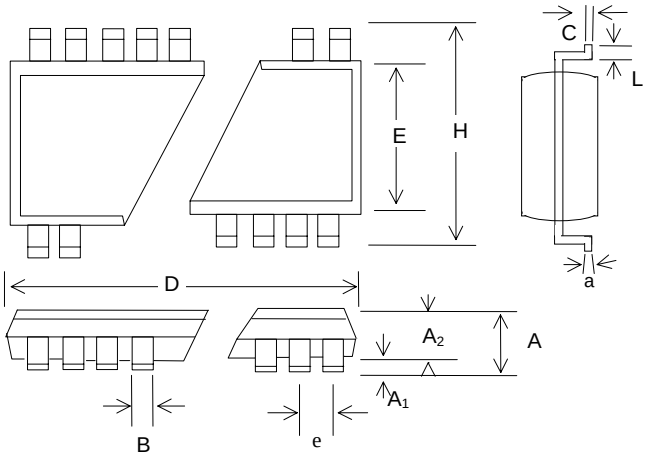
2. Unused inputs must be held high or low to prevent them from floating.
3. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level. See *Figure 1*.
4. Differential cross-point input voltage is expected to track V_{DD} and is the voltage at which the differential signals must be crossing.
5. For load conditions see *Figure 1*.
6. The value of VOC is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120Ω resistor. See *Figure 1*.
7. All outputs switching loaded with 16 pF in 60Ω environment. See *Figure 1*.

AC Parameters[8]**:** $V_{DD2.5}$ = 2.5V + 5%, $V_{DD3.3\_2.5}$ = 3.3V + 5% or 2.5V + 5%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
fCLK	Operating Clock Frequency		60		170	MHz
tDC	Input Clock Duty Cycle		48		52	%
Tr/Tf	DDR Output Clocks Rise/Fall edge rate	20% to 80%	1.0		4.0	V/ns
tDC	Output Duty Cycle	Measured at 1.5V for 3.3V outputs. Measured at 1.25V for VDD/2V outputs	INDC – 2%		INDC + 2%	%
Tr/Tf	SDRAMs Rise/Fall edge rate	0.4V to 2.4V	1.0		4.0	V/ns
	SDRAM Propagation Delay SDRAM Input to SDRAM output		TBD		TBD	ns
tpZL, tpZH	Output Enable Time[9] (all outputs)			3		ns
tpLZ, tpHZ	Output Disable Time[9] (all outputs)			3		ns
tPLH	Low-to-High Propagation Delay, BUFIN to Output		1.5	3.5	6	ns
tPHL	High-to-Low Propagation Delay, BUFIN to Output		1.5	3.5	6	ns
tSKEW	Any Output to Any Output Skew[10]	Note 11			100	ps

Notes:

8. Parameters are guaranteed by design and characterization. Not 100% tested in production.
9. Refers to transition of non-inverting output.
10. All differential input and output terminals are terminated with 120Ω/16 pF as shown in *Figure 1*.
11. This measurement is applicable to outputs of similar function. SDRAM to SDRAM skew is measured at 1.5V. DDRT/C to DDRT/C skew is measure at crossing point (VOC). SDRAM to FBOUT skew is measured at 1.5V. DDRT/C to FBOUT skew is measured at 50% (for FBOUT) and at crossing point (VOC) for DDRT/C.



48-Pin SSOP Outline Dimensions

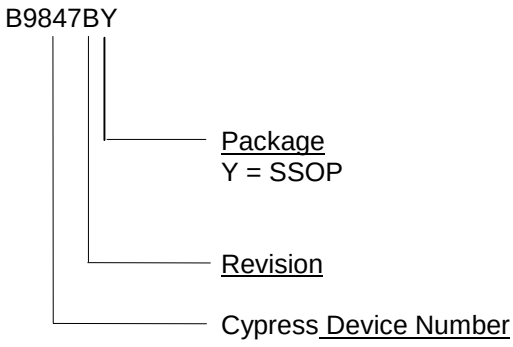
Symbol	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
IMIB9847BY	48-Pin SSOP	Commercial, 0°C to +70°C
IMIB9847BYT	48-Pin SSOP - Tape and Reel	Commercial, 0°C to +70°C

Note:The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
B9847BY
Date Code, Lot #



Revision History

Document Title: B9847 DDR Clock Distribution Buffer/Driver Document Number: 38-07197				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111340	12/16/01	DMG	New data sheet