2-DIMM DDR Clock Distribution Buffer/Driver

Features

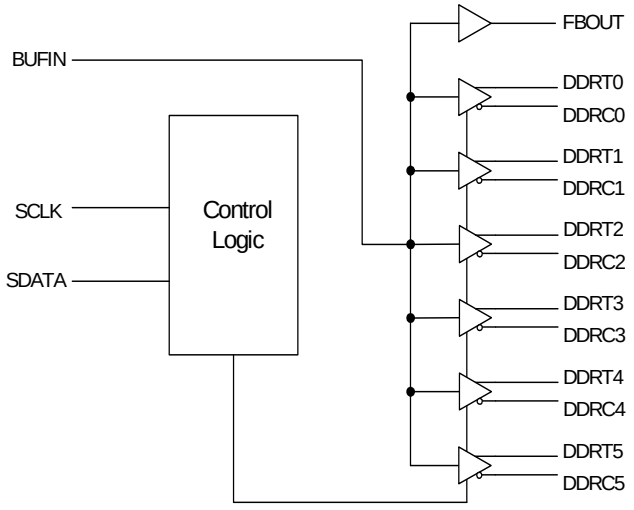
- **Supports 266 MHz DDR SDRAM**
- **Supports VIA Pro 266, PM266, and KT266 chipsets**
- **Operating frequency: 60 MHz – 170 MHz**
- **6 differential pairs**
- **Spread-spectrum-compatible**
- **Low jitter (cycle-to-cycle): < 75 ps**
- **Very low skew: < 100 ps**
- **Fast propagation delay: < 4.5nS**
- **50% duty cycle**
- **Power management via I^2C interface**
- **2.5V power supply**
- **28-pin SSOP**

Description

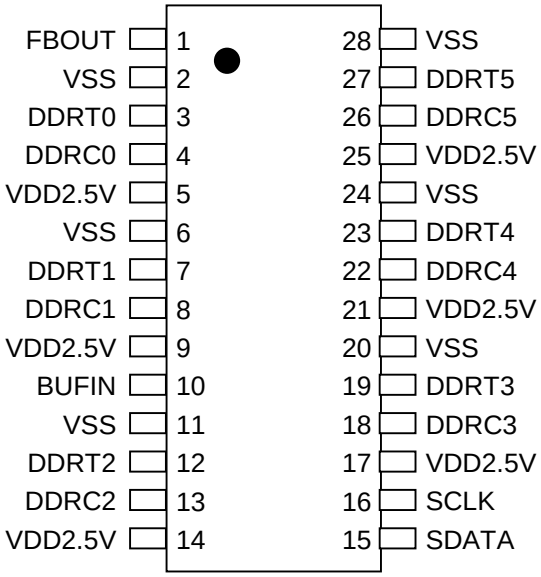
The B9846 is a high performance, low-skew, low jitter buffer designed to distribute differential clocks in high-speed applications. The B9846 generates six differential pair clock outputs to support two DDR Dimms. In addition, the B9846 features a feedback clock output, FBOUT. This output is for the chipset or other B9846 devices and/or one of Cypress's zero-delay buffers. Typically, The B9846 is used with C9846 clock synthesizer for the VIA Pro 266 chipset, and with the C9854 clock synthesizer for the VIA KT266 chipset.

The I^2C interface enables/disables differential pair outputs. This feature allows flexibility in system power management.

Block Diagram



Pin Configuration



Pin Description

Pin No.	Pin Name	PWR	I/O	Description
10	BUFIN	VDD2.5V	I	**Clock Input**. 2.5V for DDR-ONLY.
3,7,12,19,23,27	DDR(0:5)T	VDD2.5V	O	**True DDR Clock Outputs**. Buffered copy of the signal applied at BUFIN.
4,8,13,18,22,26	DDR(0:5)C	VDD2.5V	O	**Complementary DDR Clock Outputs**. Inverted copy of the signal applied at BUFIN.
1	FBOUT	VDD2.5V	O	**Feedback Clock Output**. Single ended buffered copy of the signal applied at BUFIN. This clock is in phase with the True DDR clock outputs. It is generally used to drive the DCLKI of chipset memory controller.
16	SCLK		I, PU[1]	**Serial Clock Input**. Clocks data at SDATA into the internal register.
15	SDATA		I/O, PU	**Serial Data Input**. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.
5,9,14,17,21,25	VDD2.5			2.5V power supply
2,6,11,20,24,28	VSS			Common ground

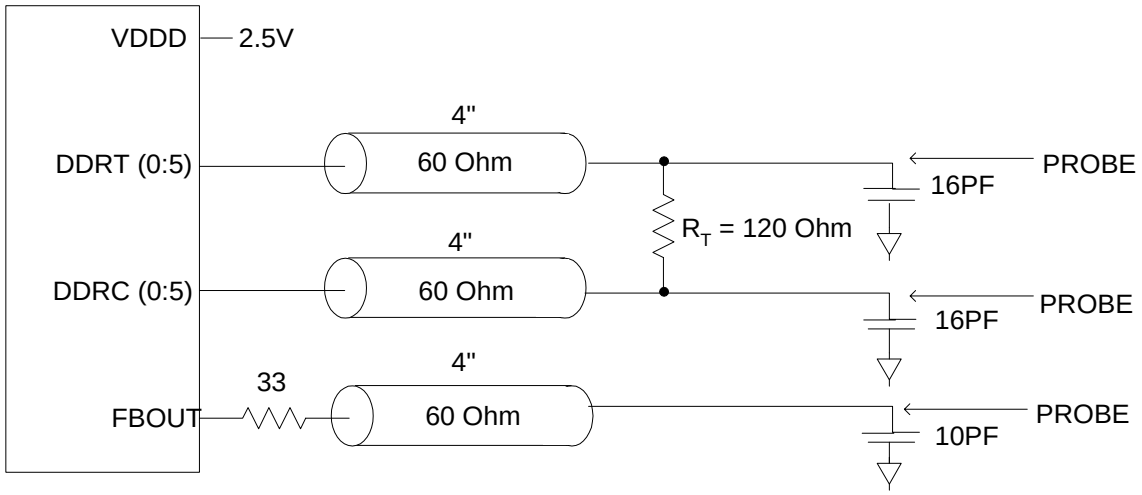


Figure 1. Differential Signal Using Direct Termination Resistor

A bypass capacitor (0.1 µF) should be placed as close as possible to each positive power pin (< 0.2”). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Note:
1. PU = Internal pull-up, typical value of 640KΩ.

Serial Control Registers

Following the acknowledge of the Address byte, two additional bytes must be sent:

1. Command code
2. Byte count.

Byte(0:5) are dummy bytes and are reserved. These bytes will be ignored and acknowledged. For more details on the use of the I^2C interface, see our application note entitled *2-Wire I2C Control Interface* (AN0022).

Byte 6: Output Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin No.	Description
7	0	–	Reserved
6	0	–	Reserved
5	0	–	Reserved
4	1	1	FBOUT
3	1	–	Reserved
2	1	26,27	DDRT/C5
1	1	22,23	DDRT/C4
0	1	18,19	DDRT/C3

Byte 7: Output Register (1 = Enable, 0 = Disable)

Bit	@Pup	Pin No.	Description
7	1	–	Reserved
6	1	–	Reserved
5	1	–	Reserved
4	1	12,13	DDRT/C2
3	1	–	Reserved8
2	1	7, 8	DDRT/C1
1	1	–	Reserved
0	1	3, 4	DDRT/C0

Maximum Ratings

Input Voltage Relative to V_{SS} ..... V_{SS} – 0.3V
Input Voltage Relative to V_{DD} ..... V_{DD} + 0.3V
Storage Temperature .....–65°C to +150°C
Operating Temperature .....0°C to +70°C
Maximum Power Supply 5.5V

This device contains circuitry to protect the inputs against damage due to high-static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters VDD2.5V = 2.5V + 5%, T_A = 0°C to +70°C [2]

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage	SDATA , SCLK		–	1.0	V
V_{IH}	Input High Voltage		2.2	–		V
V_{IL1}	Input Low Voltage	BUFIN			1.0	
V_{IH1}	Input High Voltage		2.0			
I_{IH}	Input High Current	$V_{IN} = V_{DD}$, BUFIN, PD#			10	µA
I_{IL}	Input Low Current				–TBD	µA
I_{OL}	Output Low Current	V_{DD} = 2.375V, V_{OUT} = 1.2V	26	35		mA
I_{OH}	Output High Current	V_{DD} = 2.375V, V_{OUT} = 1V	–18	–32		mA
V_{OL}	Output Low Voltage	V_{DD} = 2.375V, I_{OL} = 12 mA			0.6	V
V_{OH}	Output High Voltage	V_{DD} = 2.375V, I_{OH} = –12 mA	1.7			V
V_{OUT}	Output Voltage Swing[5]		0.7		V_{DD}+0.6	V
V_{OX}	Output Crossing Voltage[6]		(V_{DD}/2) – 0.2	V_{DD}/2	(V_{DD}/2) + 0.2	V
I_{OZ}	High-Impedance Output Current	V_O = GND or $V_O = V_{DD}$	–10		10	µA
I_{DD}	Dynamic Supply Current[7]	All V_{DD}, FO = 133 MHz	–	TBD	TBD	mA
I_{DDS}	Shutdown Supply Current	All V_{DD}		–	TBD	mA
C_{IN}	Input Pin Capacitance		–	5	–	pF

Notes:

2. Unused inputs must be held high or low to prevent them from floating.
3. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level. See *Figure 1*. **AUTHOR: NO CORRESPONDING FOOTNOTE IN THE TEXT.**
4. Differential cross-point input voltage is expected to track V_{DD} and is the voltage at which the differential signals must be crossing. **AUTHOR: NO CORRESPONDING FOOTNOTE IN THE TEXT.**
5. For load conditions, see *Figure 1*.
6. The value of VOC is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120Ω resistor. See *Figure 1*.
7. All outputs switching loaded with 16 pF in 60Ω environment. See *Figure 1*.

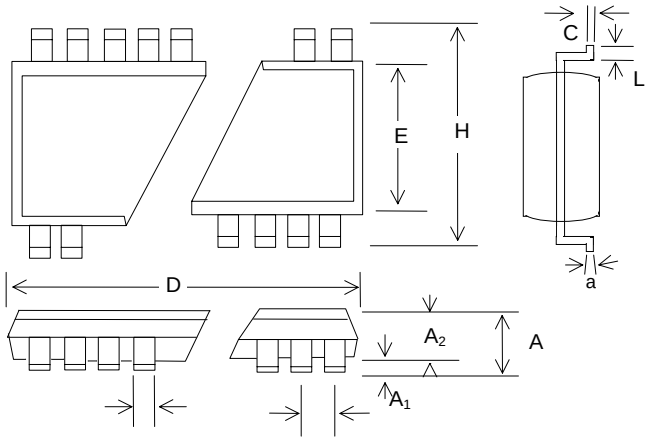
AC Parameters VDD2.5V = 2.5V + 5%, T_A = 0°C to +70°C [2]

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
fCLK	Operating Clock Frequency		60		170	MHz
tDC	Input Clock Duty Cycle		48		52	%
Tr / Tf	DDR Output Clocks Rise/Fall Edge Rate	20% to 80%	1.0		3.0	V/ns
tDC	Output Duty Cycle[3] Single ended output	Measured at 1.4V for 3.3V outputs. Measured at V_{DD}/2 for 2.5V outputs	INDC – 2%	–	INDC + 2%	%
tHCS	Half-period jitter	Note 8	–100		100	ps
tPLH	Low-to-High Propagation Delay, BUFIN to Output		1.5	3.5	6	ns
tPHL	High-to-Low Propagation Delay, BUFIN to Output		1.5	3.5	6	ns
tSKEW	Any-Output-to-Any-Output Skew	Note 8			150	ps

Notes:

8. Measured at crossing point (VOC). DDRT/C to FBOUT skew is measured at 50% (for FBOUT) and at crossing point (VOC) for DDRT/C.
9. Parameters are guaranteed by design and characterization. Not 100% tested in production. **AUTHOR: NO CORRESPONDING FOOTNOTE IN THE TEXT.**

Package Diagram



28-pin SSOP Outline Dimensions

Parameter	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	–	–	0.079	–	–	2.0
A_1	0.002	–	0.006	0.05	–	0.15
A2	0.065	0.069	0.073	1.65	1.75	1.85
B	0.009	–	0.015	0.22	–	0.38
C	0.004	–	0.010	0.09	–	0.25
D	0.390	0.402	0.413	9.90	10.20	10.50
E	0.197	0.209	0.220	5.00	5.30	5.60
e	0.026 BSC			0.65 BSC		
H	0.291	0.307	0.323	7.40	7.80	8.20
L	0.022	0.030	0.037	0.55	0.75	0.95
a	0º	–	8º	0º	–	8º

Ordering Information

Part Number	Package Type	Production Flow
B9846AY	28 PIN SSOP	Commercial, 0°C to +70°C
B9846AYT	28 PIN SSOP – Tape and Reel	Commercial, 0°C to +70°C

The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below. Purchase of I^2C components from Cypress, or one of its sublicensed Associated Companies, conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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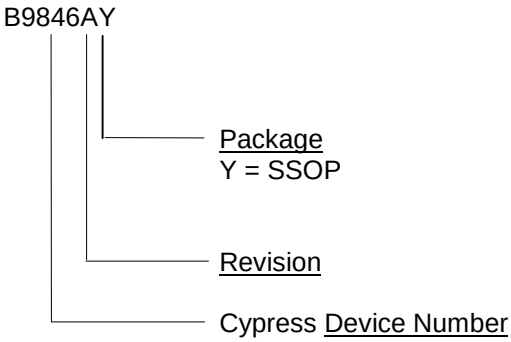
Marking: Example: Date Code
B9846AY
Lot #



Document Title: B9846 2-DIMM DDR Clock Distribution Buffer/Driver Document Number: 38-07299				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111302	12/16/01	DMG	New Data Sheet