zeroskew: 5/01
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Zero-Skew Backplane Using the RoboClock II™

Overview

This article discusses the use of Cypress' RoboClock II ™ Phase Locked Loop (PLL)-based, skew-defeating clock buffer, in designing and implementing a zero-skew backplane.

Unlike traditional clock buffers, RoboClock® and RoboClock II™ enjoy the advantages of an internal, multi-tapped PLL. This offers designers three principal advantages: zero propagation delay, configurable phase control relative to the reference clock, and a wide array of multiply and divide capabilities.

Zero propagation delay is achieved through the presence of the internal PLL. Because of the properties of it's PLL, RoboClock II™ is able to synchronize itself to an incoming reference clock, allowing the buffered outputs to be coincident(having zero delay) with the reference input. Configurable phase control allows the designer to overcome the effects of clock skew and effectively move it's outputs in or out in time relative to the reference. Divide capabilities on the output pins and the presence of an external feedback allow designers to effectively create multiply and divide variations on outputs of RoboClock II not previously possible with PLL based clock distribution devices.

It is assumed that the reader has a working understanding of RoboClock and RoboClock II. If not, "Related Documents" shown below are recommended.

Using RoboClock II's abilities to eliminate propagation delay, it's multiply capabilities to increase the reference clock frequency, and taking advantage of RoboClock II's robust programmable skew functions this note will describe a 16 board chassis, where the clock is presented to each board in the chassis phase-aligned with the input reference clock and multiplied up from the input reference clock frequency.

Related Documents

For a more complete description of RoboClock as well as its internal PLL, the reader is encouraged to consult the following documents for additional information:

"CY7B993/4V High Speed Multi-Phase Clock Buffer Data Sheet"

http://www.cypress.com/cypress/prodgate/timi/cy7b993v_994v.html

"Frequently Asked Questions About the RoboClock II Family"

http://www.cypress.com/clock/appnotes.html

"RoboClock II Test Mode"

http://www.cypress.com/clock/appnotes.html

"Frequently Asked Questions About the RoboClock Family"

http://www.cypress.com/clock/appnotes.html

16-Slot Chassis Clock Tree Design

For this example, the reference clock being used is 25 MHz. RoboClock II will be used to multiply the reference clock up to 100 MHz and distribute this to the 16 chassis slots. The design will use all 4 clock outputs from each of the 4 banks (16 total), and combined with the programmable skew settings and 4 groups of matched trace lengths, will deliver the clocks to the 16 boards at 100 MHz and phase aligned to the reference input.

Multiplying 25 MHz up to 100 MHz

Programming the Feedback Bank outputs to give a /4 output on QFA0 and QFA1 and using one of these as the input to the feedback bank (FBKA or FBKB) of the RoboClock II causes the internal RoboClock II PLL to run at 4x the input frequency. Using a 25-MHz reference input allows a 100 MHz output for all of the outputs on Banks 1–4. *Table 1* shows the Output divider functions for the feedback pins and the Bank 1–4 outputs.

Table 1. Output Divider Functions

Function Selects		Output Divider Function				
[1:4]DS1 and FBDS1	[1:4]DS0 and FBDS0	Bank 1	Bank 2	Bank 3	Bank 4	Feedback Bank
LOW	LOW	/1	/1	/1	/1	/1
LOW	MID	/2	/2	/2	/2	/2
LOW	HIGH	/3	/3	/3	/3	/3
MID	LOW	/4	/4	/4	/4	/4
MID	MID	/5	/5	/5	/5	/5
MID	HIGH	/6	/6	/6	/6	/6
HIGH	LOW	/8	/8	/8	/8	/8
HIGH	MID	/10	/10	/10	/10	/10
HIGH	HIGH	/12	/12	/12	/12	/12

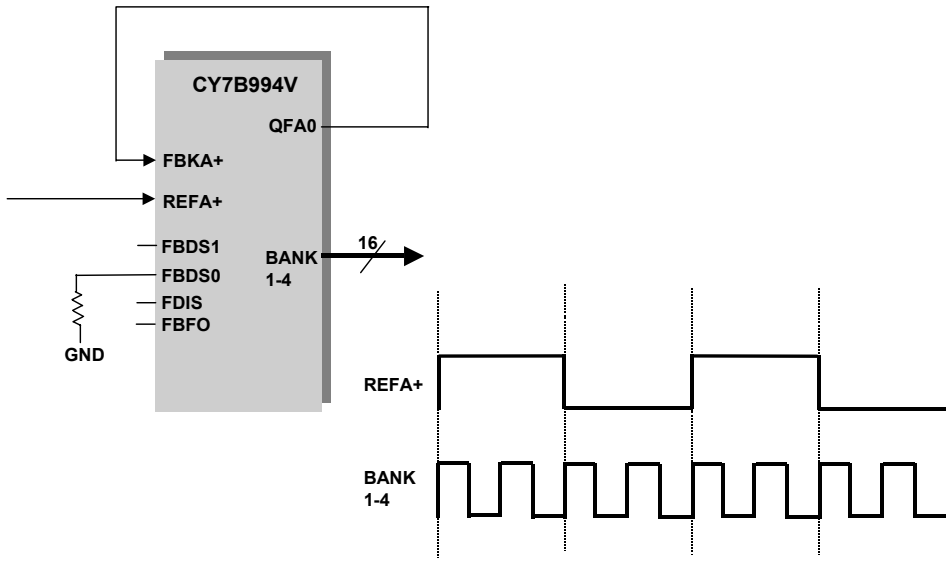

Figure 1. x4 Multiply

Figure 1 shows the RoboClock II configuration creating a x4 output for all outputs on Banks 1–4. The divide by 4 function on the Feedback output pins (QFA0, QFA1) is created by pulling input FBDS0 low and leaving FBDS1 at the MID setting.

Matching Skews Across the Backplane

Prior to RoboClock and RoboClock II designers would be required to match all clock output trace lengths from the clocking source to each load to create a zero skew clock tree. However, using this technique on a backplane was only effective when the backplane was relatively small (i.e., few chassis slots). The reason for this is that the longest trace length required to reach the furthest chassis slot was the trace length or loading that needed to be duplicated for all clock outputs (If reaching the furthest chassis slot required a trace of 30", all trace lengths for outputs from the clock distribution device needed to be matched at this same length of 30"). Because of the lack of space and the complexity involved in adding additional length to traces, this was often times difficult or impossible to do.

With the outputs of the RoboClock II device running at 100 MHz, the 16 chassis slots will be broken into 4 discreet regions. Using the programmable skew settings on the RoboClock II, 4 different skew offsets—1 from each output bank— will be used to supply clocks to the 4 chassis regions defined. Using these 4 discreet skew offset zones the design will match trace lengths within these 4 zones, creating a zero skew clock distribution and minimizing the required trace lengths. *Figure 2* shows the RoboClock II settings required to create 4 discreet skew zones, each offset by 2 Time Units (t_U):

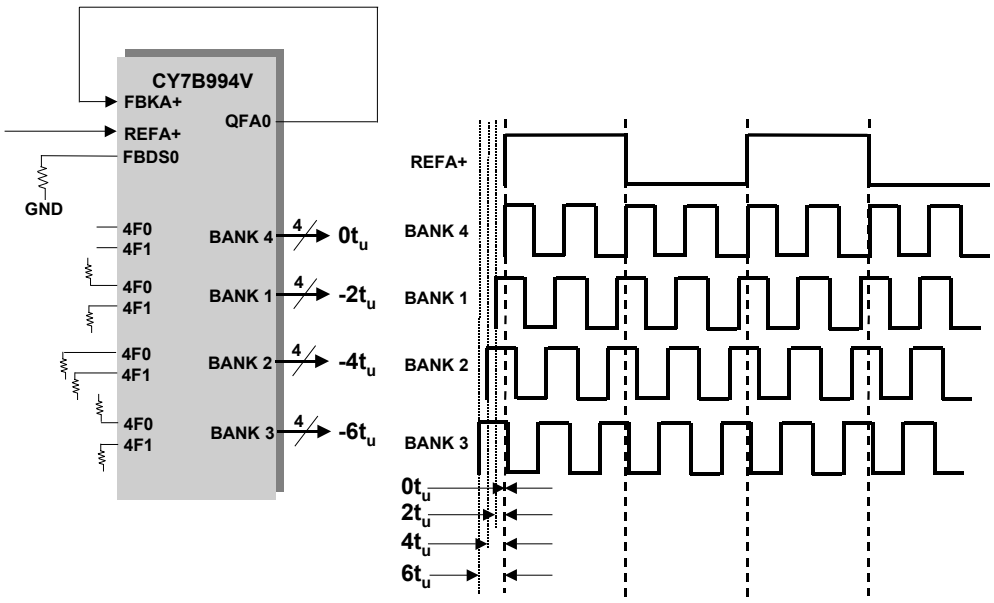

Figure 2. Bank Skew Settings

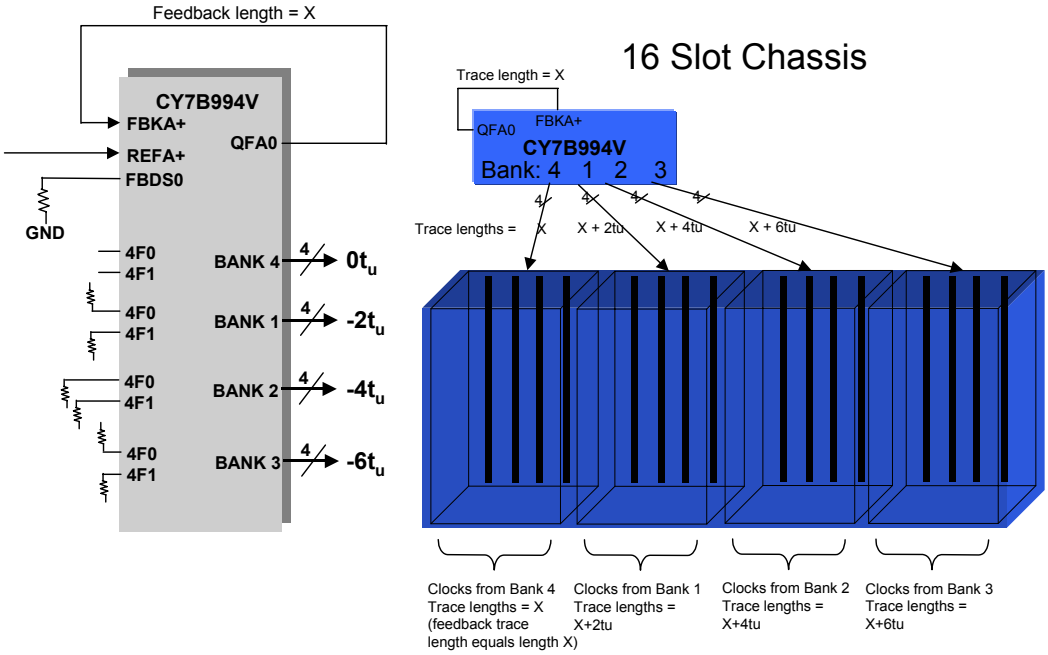

Figure 3. Backplane Layout

Actual trace length delays are dependent upon the materials used for both the backplane and the traces. Consult the board/backplane manufacturers for specifications on the materials used and the associated delay/unit measure resulting from these.

For this example, we will assume a delay of 179 ps/inch. Using the CY7B994V with FS set to Mid and Fnom = 100 MHz, the Time Unit or t_u = 0.625 ns. For a $2t_u$ Skew this translates into 1.25 ns or, 6.983 inches in effective trace length. The backplane layout is shown in *Figure 3*.

For the first skew zone receiving the 0 t_u clock outputs from Bank 4, all of the output clock traces must be matched in length. To insure that the reference clock and the bank 4 outputs are aligned, the feedback trace length must be matched to the bank 4 clock trace lengths. By matching the trace length on the feedback path to bank 4's output clock traces, you are effectively zeroing out the delays associated with the trace lengths from these clock outputs to their respective loads. This trace length is referred to as length X and is shown in *Figure 3*. Each Bank's clock output's trace lengths must now be matched to each other and to the specified length in *Figure 3*. For the Bank 4 outputs, all 4 outputs must have a trace length of X. For the Bank 1 outputs, all 4 clock outputs must be matched and they must be X + 2 t_u in length, or as in this example- X + 6.983 inches. For Bank 2 outputs, the length to be matched is X + 4 t_u. And, for Bank 3 the outputs must be X + 6 t_u.

Designers may note that the lengths designated in this example are unsatisfactory for their design needs—either being too short or prohibitively long. There are many ways in which the designer can get around this. There are several ways to increase the overall lengths supported: (1) increase the length of X, (2) use a larger multiple of the t_u skew offset value ($6t_u$,$7t_u$,$8t_u$) and increase the trace lengths correspondingly. There are also ways to decrease the lengths: (1) reduce the length of X as much as possible, (2) use smaller multiples of $t_u$increments, (3) make the effective t_u time smaller by changing fNOM of the RoboClock II or by changing the FS setting, (4) put the $0t_u$ based skew zone closer to the center of the chassis and limit the clock runs as shown in *Figure 4*.

The example shown in *Figure 4* takes a slightly different approach. Bank 3 was selected to imitate the skew selections for Bank 2. Bank 2 is set up for a $+1t_u$ skew offset. By moving the $0t_u$ skew settings (Bank 4 outputs) toward the middle of the chassis, and offsetting the Bank 2 and 3 outputs ***forward*** in time relative to the reference clock (and Bank 4), the length of the clock traces driven by Bank 3 and Bank 2 outputs now need to be $1t_u$ shorter than the X length required on the Bank 4 clock traces.

Summary

This application note described several methods of using RoboClock II to generate a zero skew backplane. The examples given show several methods for taking advantage of the programmable skew and the multiply and divide capabilities of the device. Because of the flexibility of the RoboClock II, the number of design options is essentially limitless. RoboClock II meets the challenges of implementing today's high speed clock distribution designs.

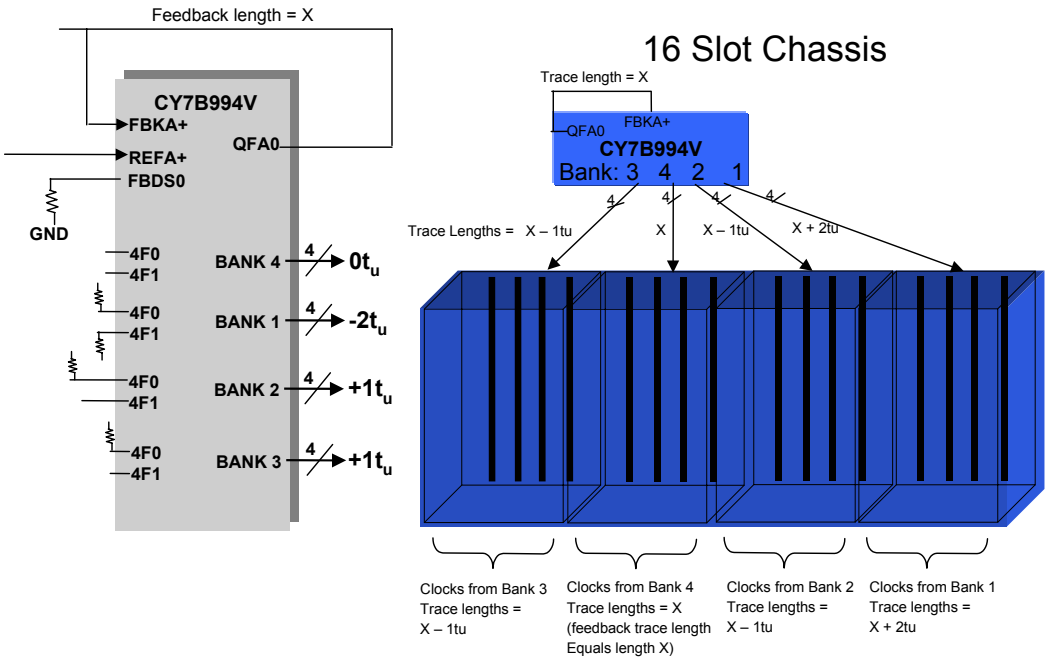

Figure 4. Backplane Layout—Another Option