DATA SHEET

PZ3960C/PZ3960N
960 macrocell SRAM CPLD

Product specification
Supersedes data of 1998 Sep 01
IC27 Data Handbook

1998 Sep 28

Philips
Semiconductors

PHILIPS

FEATURES

- Industry's largest CPLD—960 macrocells
- Industry's first SRAM-based CPLD
- Multiple configuration modes
  - Master serial
  - Slave serial
  - Master parallel-up
  - Slave parallel
  - Synchronous peripheral
- Configuration times of under 1.0 second
- IEEE 1149.1 compliant JTAG testing capability
  - 5 pin JTAG interface
  - IEEE 1149.1 TAP controller
- 3.3 volt device
- Innovative XPLA2 Architecture combines extreme flexibility and high speeds
- 8 synchronous clock networks with programmable polarity at every macrocell
- Up to 96 asynchronous clocks support complex clocking needs
- Innovative XOR structure at every macrocell provides excellent logic reduction capability
- Logic expandable to 36 product terms on a single macrocell
- PCI compliant
- Advanced 0.35µ SRAM process
- Design entry and verification using industry standard and Philips CAE tools
- Innovative Control Term structure provides either sum terms of product terms in each logic block for:
  - 3-State buffer control
  - Asynchronous macrocell register reset/preset
- Global 3-State pin facilitates 'bed of nails' testing without sacrificing logic resources
- Programmable slew rate control
- Small form factor 492 pin PBGA package provides 384 I/O pins
- Available in commercial and industrial temperature ranges

Table 1. PZ3960C/PZ3960N Features

	PZ3960C/PZ3960N
Usable gates	30,000
Maximum inputs	384
Maximum I/Os	384
Number of macrocells	960
Propagation delay (ns)	7.5
Package	492-pin PBGA

DESCRIPTION

The PZ3960 device is a member of the CoolRunner™ family of high-density SRAM-based CPLDs (Complex Programmable Logic Device) from Philips Semiconductors. This device combines high speed and deterministic pin-to-pin timing with high density. The PZ3960 uses the patented Fast Zero Power (FZP) design technique that combines high speed and low power for the first time ever in a CPLD. FZP allows the PZ3960 to have true pin-to-pin timing delays of 7.5ns, and standby currents of 100 microamps without the need for 'turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used since the bipolar era) with a cascaded chain of pure CMOS gates, both standby and dynamic power are dramatically reduced when compared to other CPLDs. The FZP design technique is also what allows Philips to offer a true CPLD architecture in a high density device. Competitors offer CPLDs that are approximately half the density of the PZ3960, and yet consume over two times the power.

The Philips PZ3960C/PZ3960N devices use the new patent-pending XPLA2™ (eXtended Programmable Logic Array) architecture. This architecture combines the best features of both PAL- and PLA-type logic structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA2™ architecture is constructed from 80 macrocell Fast Modules that are connected together by an interconnect array. Within each Fast Module are four Logic Blocks of 20 macrocells each. Each Logic Block contains a PAL structure with four dedicated product terms for each macrocell. In addition, each Logic Block has 32 additional product terms in a PLA structure that can be shared through a fully programmable OR array to any of the 20 macrocells. This combination efficiently allocates logic throughout the Logic Block, which increases device density and allows for design changes without re-defining the pinout or changing the system timing. The PZ3960 offers pin-to-pin propagation delays of 7.5ns through the PAL array of a Fast Module; and if the PLA array is used, an additional 1.5ns is added to the delay, no matter how many PLA product terms are used. If the interconnect array between Fast Modules is used, there is a second fixed addition to the propagation delay of 4.0ns. This means that the worst case pin-to-pin propagation delay within a fast module is 7.5 + 1.5 = 9.0 ns, and the delay from any pin to any other pin across the entire chip is 7.5 + 4.0 = 11.5ns if only the PAL array is used, and 7.5 + 1.5 + 4.0 = 13.0ns if the PLA array is used. This deterministic timing allows you to establish system timing before the logic design is even started.

Each macrocell also has a two input XOR gate with the dedicated PAL product terms on one input and the PLA product terms on the other input. This patent-pending Versatile XOR structure allows for very efficient logic optimization compared to competing XOR structures that have only one product term as the second input to the XOR gate. The Versatile XOR allows an 8 bit XOR function to be implemented in only 20 product terms, compared to 65 product terms for the traditional XOR approach.

The PZ3960 is SRAM-based, which means that it is configured at power up by one of many different methods. The device may be reconfigured any number of times. See the configuration section of this data sheet for more information. The device supports the full JTAG specification (IEEE 1149.1) through an industry standard JTAG interface.

Software support for the PZ3960 is through industry standard CAE tools (Cadence, Mentor, Synopsys, Synario, Viewlogic, MINC, Exemplar Logic, and Orcad) as well as Philips' own XPLA Designer. Entry methods include both text (ABEL, PHDL, VHDL, Verilog) and/or schematic. Design verification uses industry standard simulators for functional and timing simulation, and development tools are supported on personal computer, SPARC, and HP Workstation platforms. Device fitting uses either MINC or Philips Semiconductors developed tools.

ORDERING INFORMATION

ORDER CODE	PACKAGE, PROPAGATION DELAY	DESCRIPTION	DRAWING NUMBER
PZ3960C7EB	492-pin PBGA, 7.5ns t_{PD}	Commercial temp. range, 3.3 volt power supply ± 10%	SOT514–1
PZ3960N8EB	492-pin PBGA, 8.0ns t_{PD}	Industrial temp. range, 3.3 volt power supply ± 10%	SOT514–1

XPLA2 ARCHITECTURE

Figure 1 shows a high level block diagram of the PZ3960 implementing the XPLA2 architecture. The XPLA2 architecture is a multi-level, modular hierarchy that consists of Fast Modules interconnected by a Global Zero Power Interconnect Array (GZIA). The GZIA is a virtual crosspoint switch that connects the Fast Modules together. Each Fast Module accepts 64 bits from the GZIA and outputs 64 bits to the GZIA. Each Fast Module is essentially an 80 macrocell CPLD with four logic blocks of 20 macrocells each inside. There are eight dedicated, low-skew, global clocks for the device; and each Fast Module has access to any two of these clocks (there are additional asynchronous clocks available in the Fast Modules, see Figure 3). There are also Global 3-state (gts) and Global Reset (rstn) pins that are common to all Fast Modules. When gts is pulled high, all output buffers in the device will be disabled, causing all I/O pins to be tri-stated. When rstn is pulled low, all flip-flops of the device will be reset.

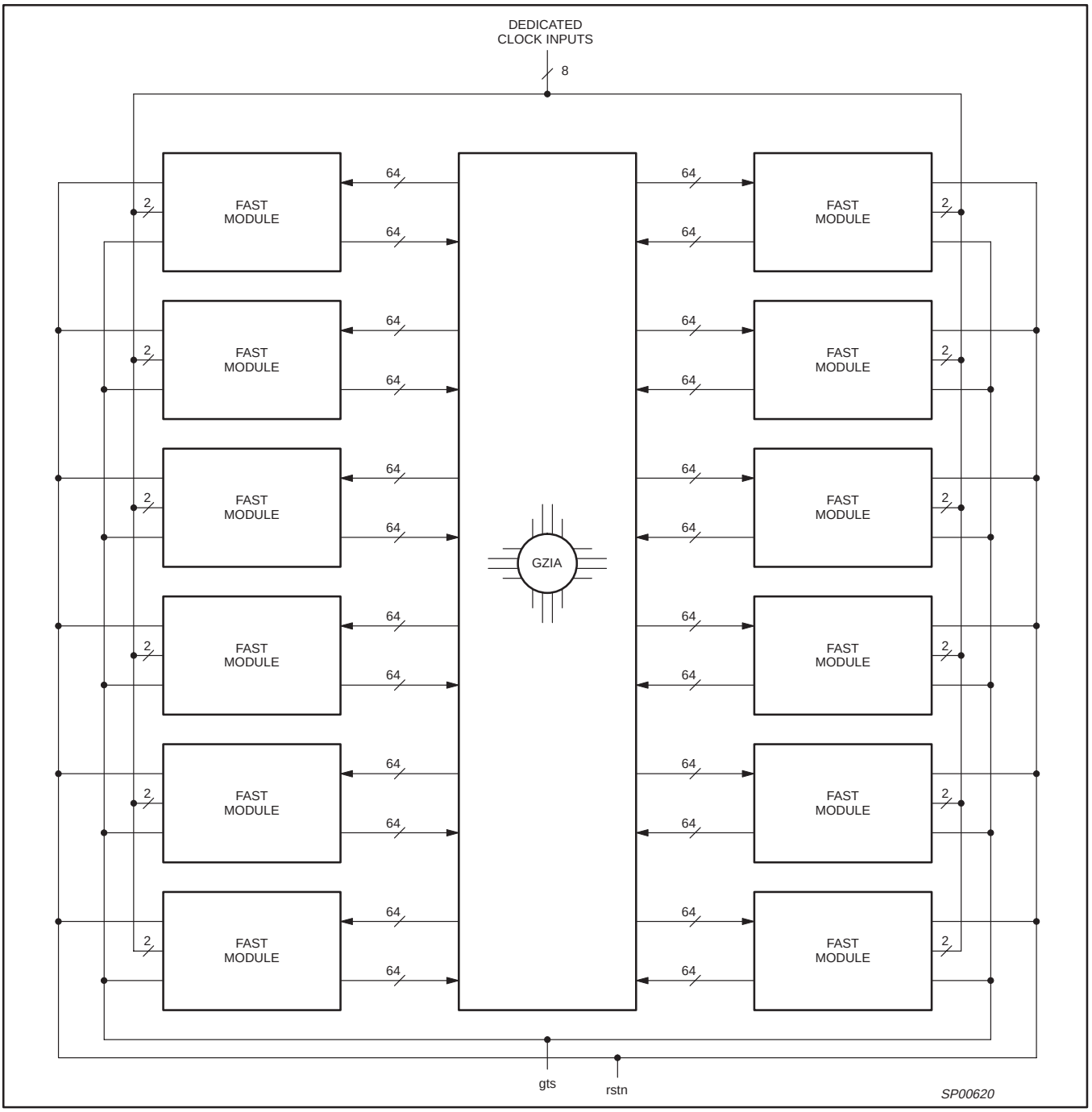


Figure 1. Philips XPLA2 CPLD Architecture

XPLA2 Fast Module

Each Fast Module consists of four Logic Blocks of 20 macrocells each. Eight of the 20 macrocells in each Logic Block are connected to I/O pins and the remaining 12 can be used as buried nodes. These four Logic Blocks are connected together by the Local Zero Power Interconnect Array (LZIA). The LZIA is a virtual crosspoint switch that connects the Logic Blocks to each other and to the GZIA. The feedback from all 80 macrocells, input from the I/O pins, and the 64 bit input bus from the GZIA are input into the LZIA. The LZIA outputs 36 signals into each Logic Block and 64 signals into the GZIA.

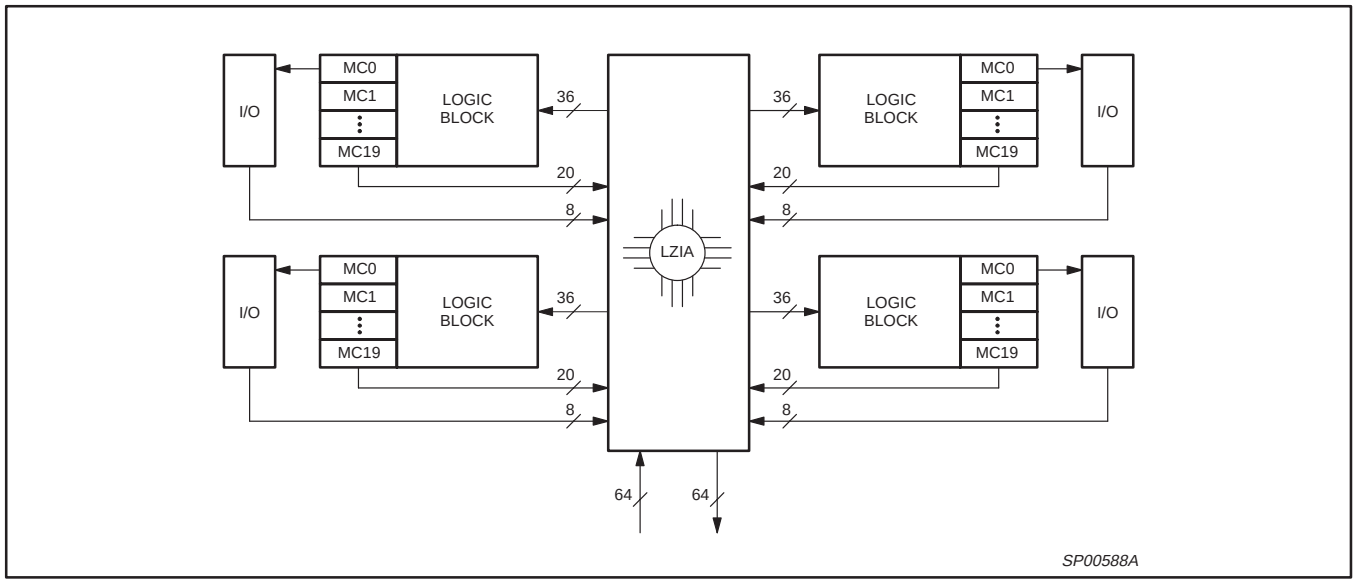


Figure 2. Philips XPLA2 Fast Module

XPLA2 Logic Block Architecture

Figure 3 illustrates the XPLA2 Logic Block architecture. Each Logic Block contains 8 control terms, a PAL array, a PLA array, and 20 macrocells. The 36 inputs from the LZIA are available to all control terms and to each product term in both the PAL and the PLA array. The 8 control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the asynchronous preset and reset functions of the macrocell registers, the output enables of the 20 macrocells, and for asynchronous clocking. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array.

Each macrocell has 4 dedicated product terms from the PAL array. When additional logic is required, each macrocell takes the extra product terms from the PLA array. The PLA array consists of 32 extra product terms that are shared between the 20 macrocells of the Logic Block. The PAL product terms can be connected to the PLA product terms through either an OR gate or an XOR gate. One input to the XOR gate can be connected to all the PLA terms, which provides for extremely efficient logic synthesis. An eight bit XOR function can be implemented in only 20 product terms. Each macrocell can use the output from the OR gate or the XOR gate in either normal or inverted state.

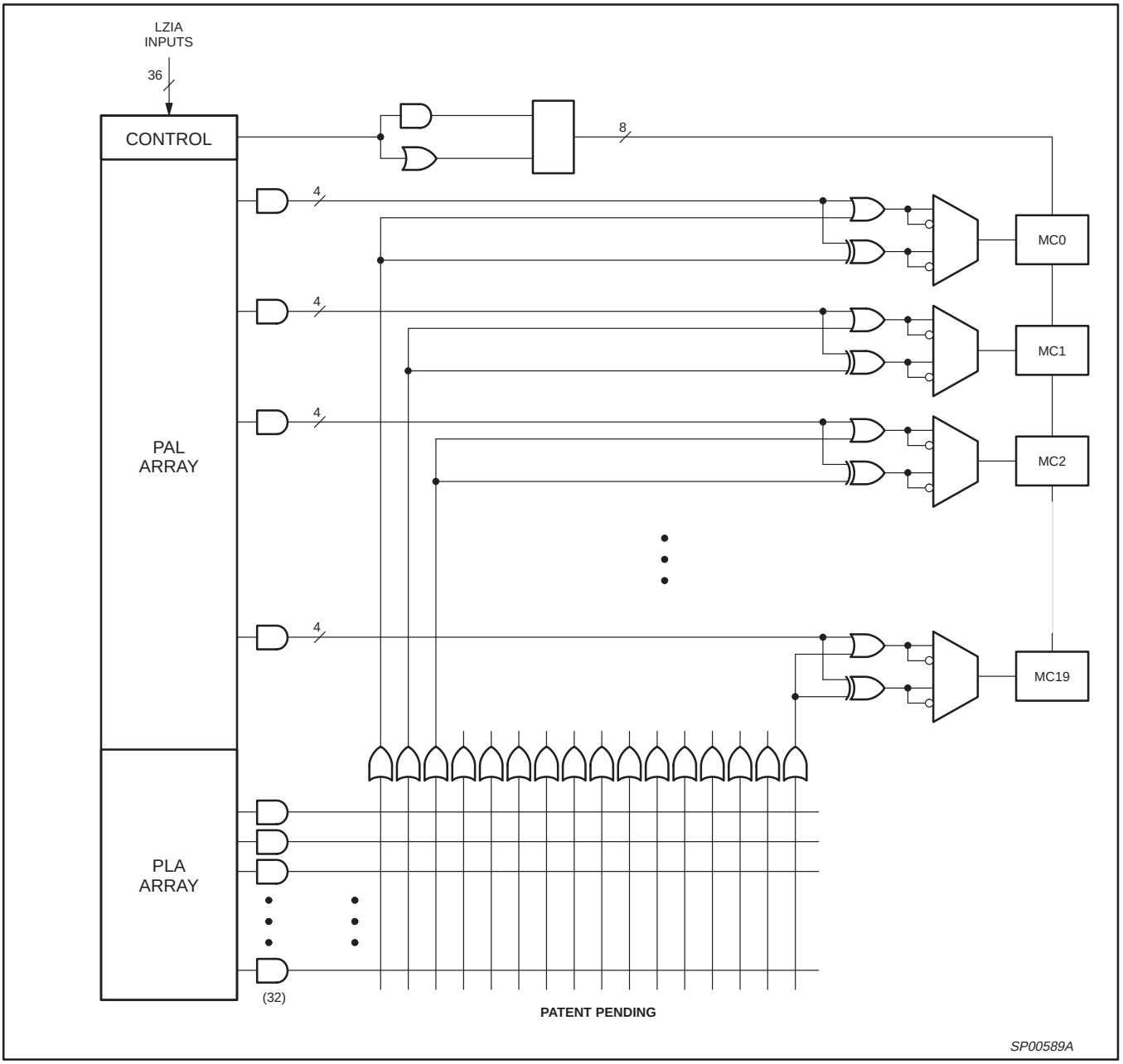


Figure 3. Philips XPLA2 Logic Block Architecture

XPLA2 Macrocell Architecture

Figure 4 shows the XPLA2 macrocell architecture used in the PZ3960. The macrocell can be configured as either a D- or T-type flip-flop or a combinatorial logic function. A D-type flip-flop is generally more useful for implementing state machines and data buffering while a T-type flip-flop is generally more useful in implementing counters. Each of these flip-flops can be clocked from any one of four sources. Two of the clock sources (CLK0 and CLK1) are from the eight dedicated, low-skew, global clock networks designed to preserve the integrity of the clock signal by reducing skew between rising and falling edges. These clocks are designated as a "synchronous" clocks and must be driven by an external source. Both CLK0 and CLK1 can clock the macrocell flip-flops on either the rising edge or the falling edge of the clock signal. The other clock sources are designated as "asynchronous" and are connected to two of the eight control terms (CT6 and CT7) provided in each logic block. These clocks can be individually configured as any PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. Thus, in each Logic Block, there are up to four possible clocks; and in each Fast Module, there are up to 10 possible clocks. Throughout the entire device, there are up to 104 possible clocks—eight from the dedicated, low-skew, global clocks, and two for each of the 48 logic blocks.

The remaining six control terms of each logic block (CT0–CT5) are used to control the asynchronous preset/reset of the flip-flops and the enable/disable of the output buffers in each macrocell. Control terms CT0 and CT1 are used to control the asynchronous preset/reset of the macrocell's flip-flop. Note that the power-on reset leaves all macrocells in the "zero" state when power is properly applied, and that the preset/reset feature for each macrocell can also be disabled. Each macrocell can choose between an asynchronous reset or an asynchronous preset function, but both cannot be simultaneously used on the same register. The global rstn function can always be used, regardless of whether or not asynchronous reset or preset control terms are enabled. Control terms CT2, CT3, CT4 and CT5 are used to enable or disable the macrocell's output buffer. Having four dedicated output enable control terms ensures that the CoolRunner™ devices are PCI compliant. The output buffers can also be always enabled or always disabled. All CoolRunner™ devices also provide a Global 3-State (gts) pin, which, when pulled high, will 3-State all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails" testing used during manufacturing.

For the macrocells in the Logic Block that are associated with I/O pins, there are two feedback paths to the LZIA: one from the macrocell, and one from the I/O pin. The LZIA feedback path before the output buffer is the macrocell feedback path, while the LZIA feedback path after the output buffer is the I/O pin feedback path. When these macrocells are used as outputs, the output buffer is enabled, and either feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pins are used as inputs, the output buffer of these macrocells will be 3-Stated and the input signal will be fed into the LZIA via the I/O feedback path. In this case the logic functions implemented in the buried macrocell can be fed back into the LZIA via the macrocell feedback path. For macrocells that are not associated with I/O pins, there is one feedback path to the LZIA. Logic functions implemented in these buried macrocells are fed back into the LZIA via this path. All unused inputs and I/O pins should be properly terminated. Please refer to the section on terminations.

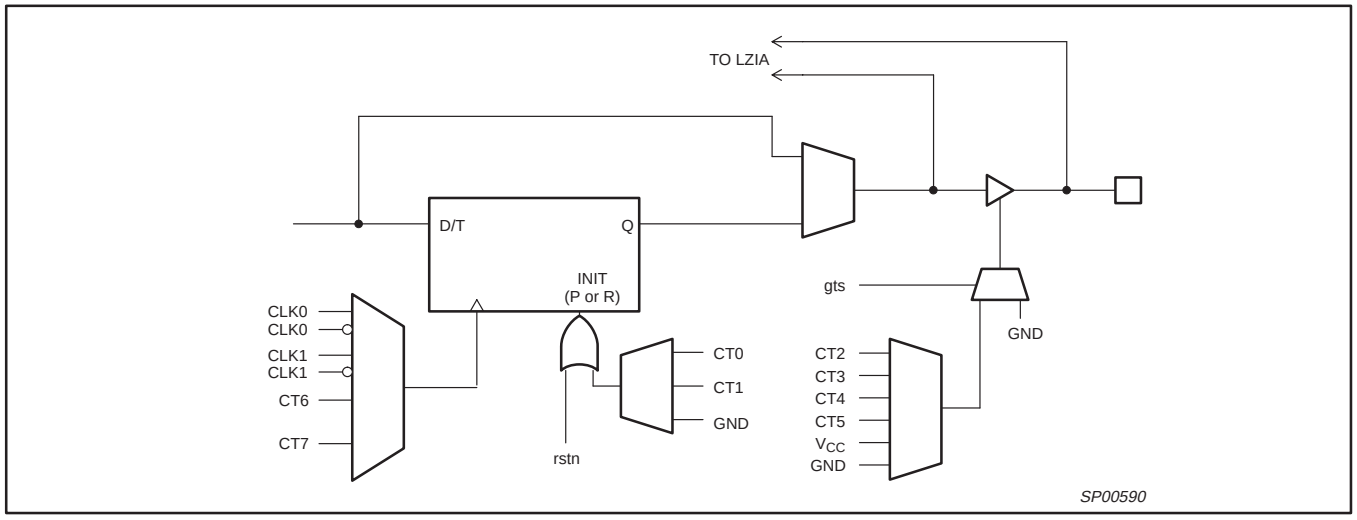


Figure 4. PZ3960 Macrocell Architecture

Simple Timing Model

Figure 5 shows the PZ3960 timing model. The PZ3960 timing model is very simple compared to the models of competing architectures. There are three main timing parameters: the pin-to-pin delay for combinatorial logic functions (t_{PD}), the input pin to register set up time (t_{SU}), and the register clock to valid output time (t_{CO}). As the model shows, timing is only dependent on whether or not you use the PLA array, and whether or not the logic function is created within a single Fast Module or uses the GZIA. The timing starts with a set time for t_{PD} and t_{SU} through the PAL array in a Fast Module, and there are fixed delays added for use of the PLA array or the GZIA. The t_{CO} timing specification never changes. For example, a combinatorial logic function of four or fewer product terms constructed from inputs within the same logic block would have a t_{PD} delay of 7.5ns. If the logic function were more than four product terms wide, the delay would be t_{PD} plus the fixed PLA delay, or 7.5 + 1.5 = 9.0ns. A function that used the PAL array and inputs from a different Fast Module would have a propagation delay of t_{PD} plus the fixed GZIA delay, or 7.5 + 4.0 = 11.5ns.

This simple timing model allows designers to determine whether or not the device will meet system timing specifications up front. In competing devices, the user is unable to determine if the design will meet system timing requirements until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, the fan-out of a signal, the varying number of X and Y routing channels used, etc. The simplicity of the PZ3960 timing model gives you pin-to-pin delay information before the design is set. Further, the timing in the PZ3960 device will not vary with place and route iterations caused by design changes. This allows the PZ3960 device to meet your timing requirements even when you make changes to the design.

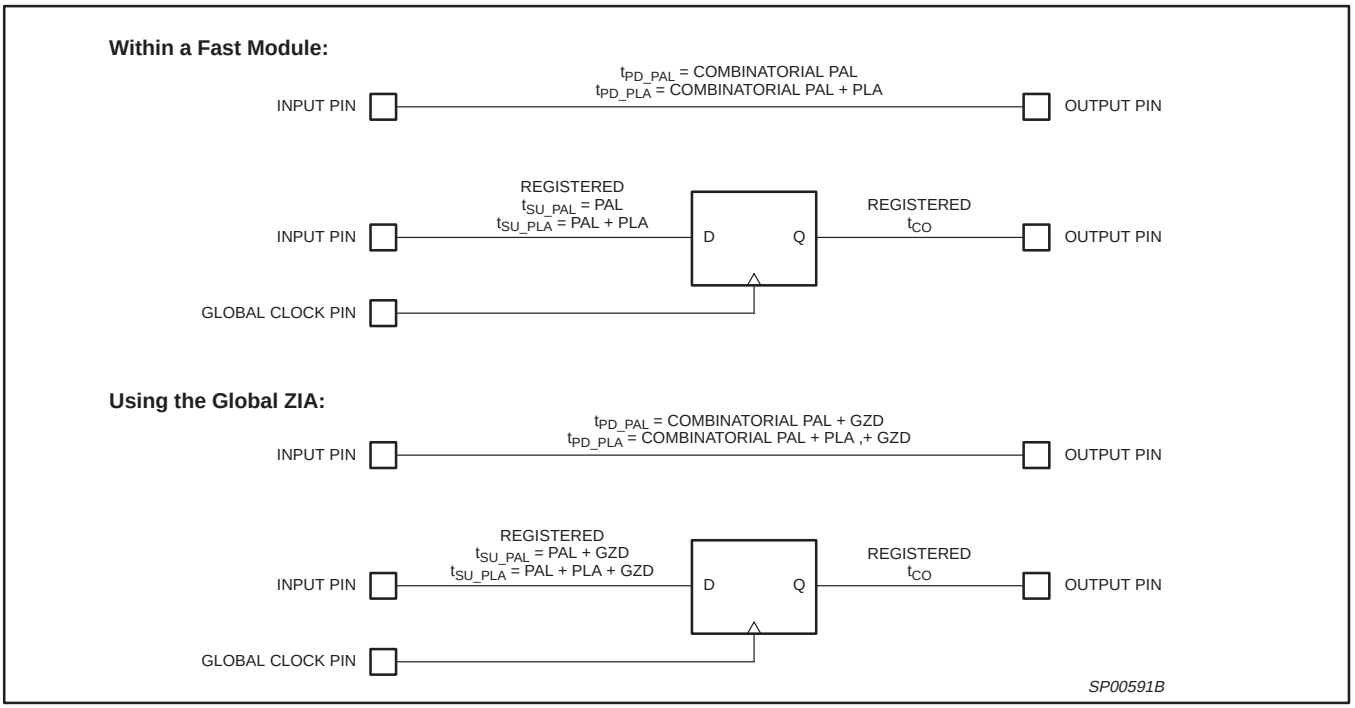


Figure 5. PZ3960 Timing Model

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ CPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its product terms instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. This also makes it possible to manufacture high density CPLDs like the PZ3960 that consume a fraction of the power of competing devices. Refer to Figure 6 and Table 2 showing the I_{DD} vs. Frequency of the PZ3960 TotalCMOS™ CPLD (data taken with 60 16-bit counters @ 3.3V, 25°C).

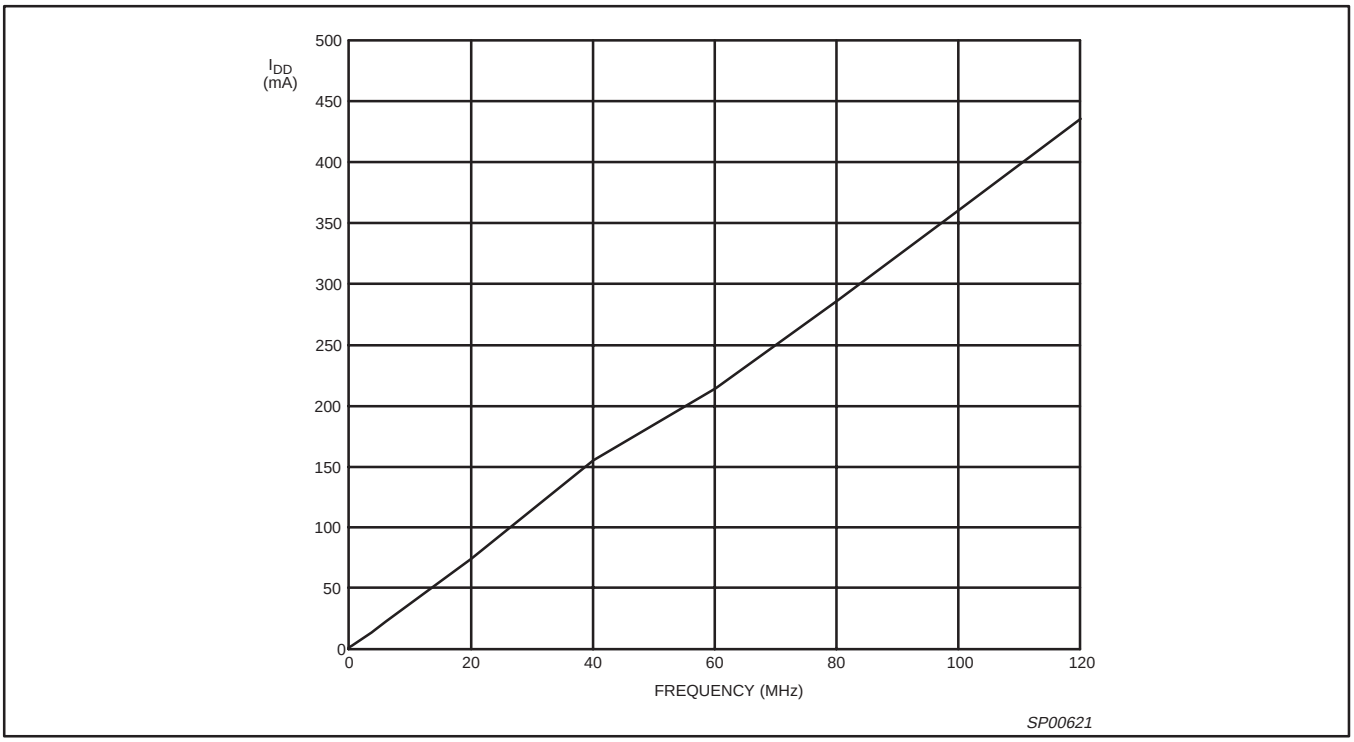


Figure 6. I_{DD} vs. Frequency @ V_{DD} = 3.3V, 25°C

Table 2. I_{DD} vs. Frequency

V_{DD} = 3.3V

FREQUENCY (MHz)	0	1	20	40	60	80	100	120
Typical I_{DD} (mA)	0.1	4.1	76.7	150.1	222.2	294.6	364	441.6

Terminations

The CoolRunner™ PZ3960C/PZ3960N CPLDs are TotalCMOS™ devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. It can also cause the voltage on a configuration pin to float to an unwanted voltage level, interrupting device operation.

The PZ3960C/PZ3960N CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-down resistors are only available for unused I/O pins, and are automatically activated by the fitter software. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. We recommend that any unused I/O pins on the PZ3960C/PZ3960N device be left unconnected.

There are no on-chip pull-down structures associated with dedicated pins used for device configuration or special device functions like global reset and global 3-state. Philips recommends that these pins be terminated consistent with the description given in Table 15. Philips recommends the use of weak pull-up and pull-down resistors for terminating these pins. These pins can be directly connected to V_{CC} or GND, but using the external pull-up resistors maintains maximum design flexibility.

When using the JTAG Boundary Scan functions, it is recommended that 10k pull-up resistors be used on the tdi, tdo, tck, and trstn pins. The tdo signal pin can be left floating unless it is connected to the tdi of another device. Letting these signals float can cause the voltage on tms to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times.

CONFIGURATION INTRODUCTION

The Philips CoolRunner™ series are available in technologies which use non-volatile (EEPROM-based) and volatile (SRAM based) configuration memory. The functionality of the XPLA2 family of the CoolRunner™ series is defined by on-chip SRAM. The devices are configured in a manner similar to that of most FPGAs. This section describes the configuration of the PZ3960, and applies to all similarly configured devices to be produced by Philips.

Either the Philips or Minc fitter, XPLA Designer and PL-Designer, respectively, is used to generate a JEDEC file. The JEDEC file contains the configuration data, which is loaded into the PZ3960 configuration memory to control the PZ3960 functionality. This is done at power-up and/or with configure command. This section provides some of the trade-offs in selecting a configuration mode, and provides debug hints for configuration problems.

There are several different methods of configuring the PZ3960. The mode used is selected using the mode select pins. There are three basic configuration methods: master, slave, and peripheral. The configuration data can be transmitted to the PZ3960 serially or in parallel bytes. As a master, the PZ3960 generates the clock and control signals to strobe configuration data into the PZ3960. As a slave device, a clock is generated externally, and provided into the PZ3960's cclk pin. In the peripheral mode, the PZ3960 interfaces as a microprocessor peripheral. Table 3 lists the configuration modes.

Design Flow Overview

Figure 7 is a diagram of the steps used in configuring the PZ3960. The development system is used to generate configuration data in the JEDEC file. Using the <design>.jed file, there are two general methods of configuring the PZ3960. The utility **download** can load the configuration data from a PC or workstation hard disk into the PZ3960. Alternately, the PZ3960 can be loaded from non-volatile ICs such as serial or parallel EEPROMs, after converting the JEDEC file to an MCS file using the jed2mcs utility.

Table 3. Configuration Modes

M2	M1	M0	cclk	CONFIGURATION MODE	DATA FORMAT
0	0	0	Output	Master serial	Serial
0	0	1	Input	Slave parallel	Parallel
0	1	0	Reserved		
0	1	1	Input	Synchronous peripheral	Parallel
1	0	0	Output	Master parallel – up	Parallel
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Input	Slave serial	Serial

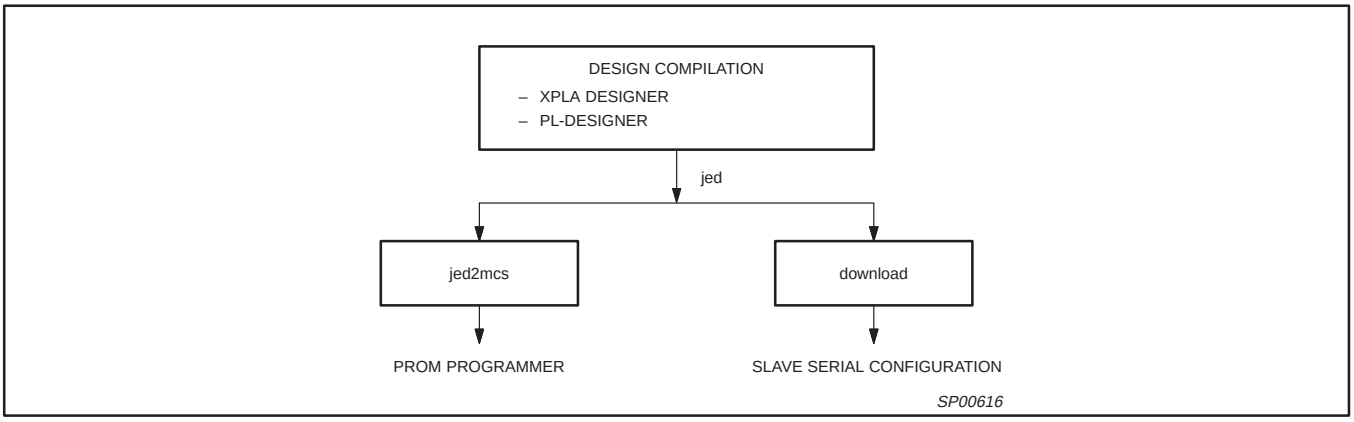


Figure 7. Design flow

PZ3960 STATES OF OPERATION

Prior to becoming operational, the PZ3960 goes through a sequence of states, including initialization, configuration, and start-up. This section discusses these three states. In the master configuration modes, the PZ3960 is the source of configuration clock (cclk).

When configuration is initiated, a counter in the PZ3960 is set to 0 and begins to count configuration clock cycles applied to the PZ3960. As each configuration data frame is supplied to the PZ3960, it is internally assembled into data words. Each data word is loaded into the internal configuration memory. The configuration loading process is complete when the internal length count equals the loaded length count in the length count field, and the required end of configuration frame is written.

All configuration I/Os used as inputs operate with TTL-level input thresholds during configuration. All I/Os that are not used during the configuration process are 3-Stated with internal pull-downs. During configuration, registers are reset. The combinatorial logic begins to function as the PZ3960 is configured. Figure 8 shows the flow between the initialization, configuration, and start-up states. Figure 9 gives the general timing information for configuring the device.

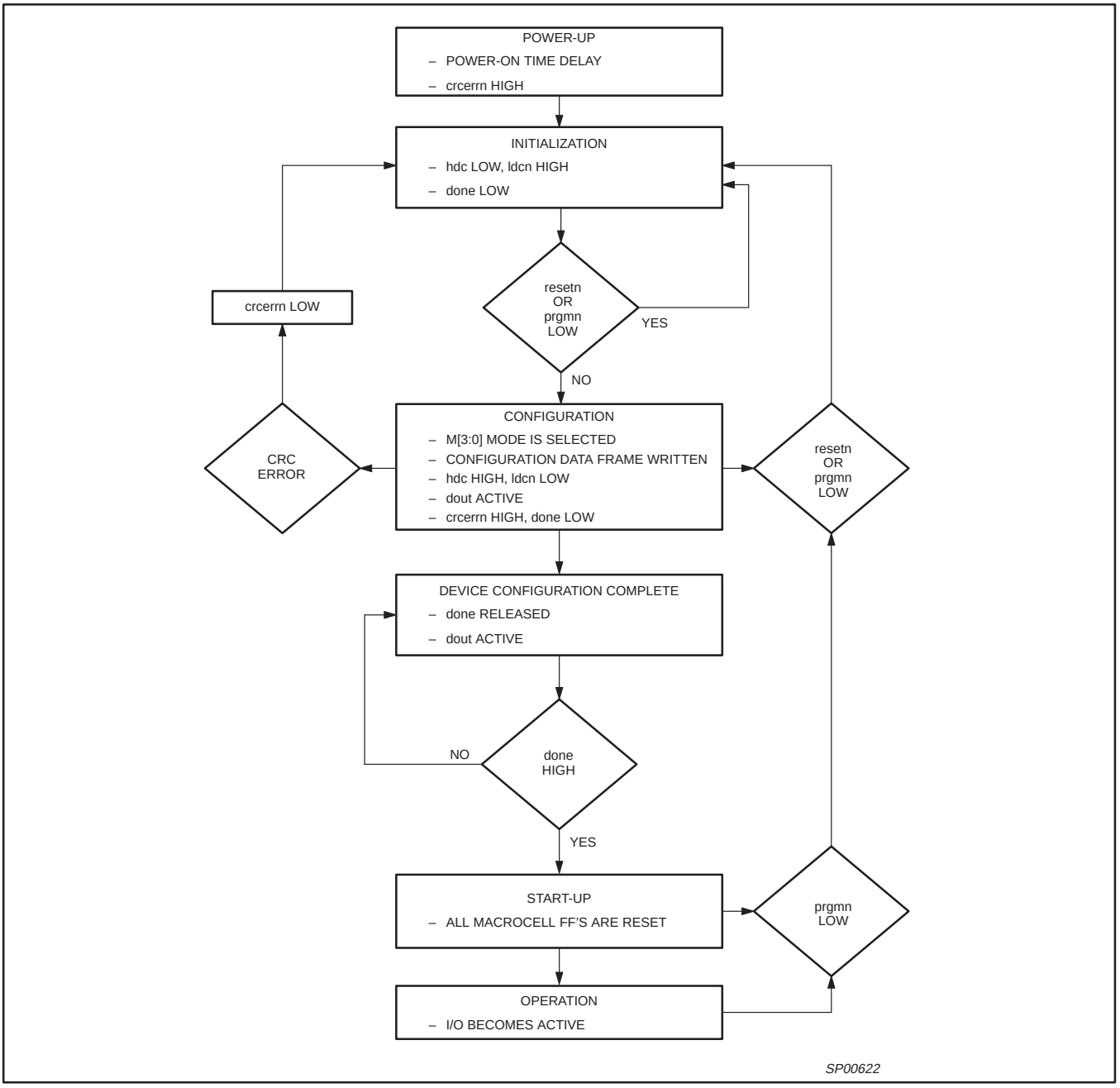


Figure 8. Flow chart of initialization, configuration, and operating states

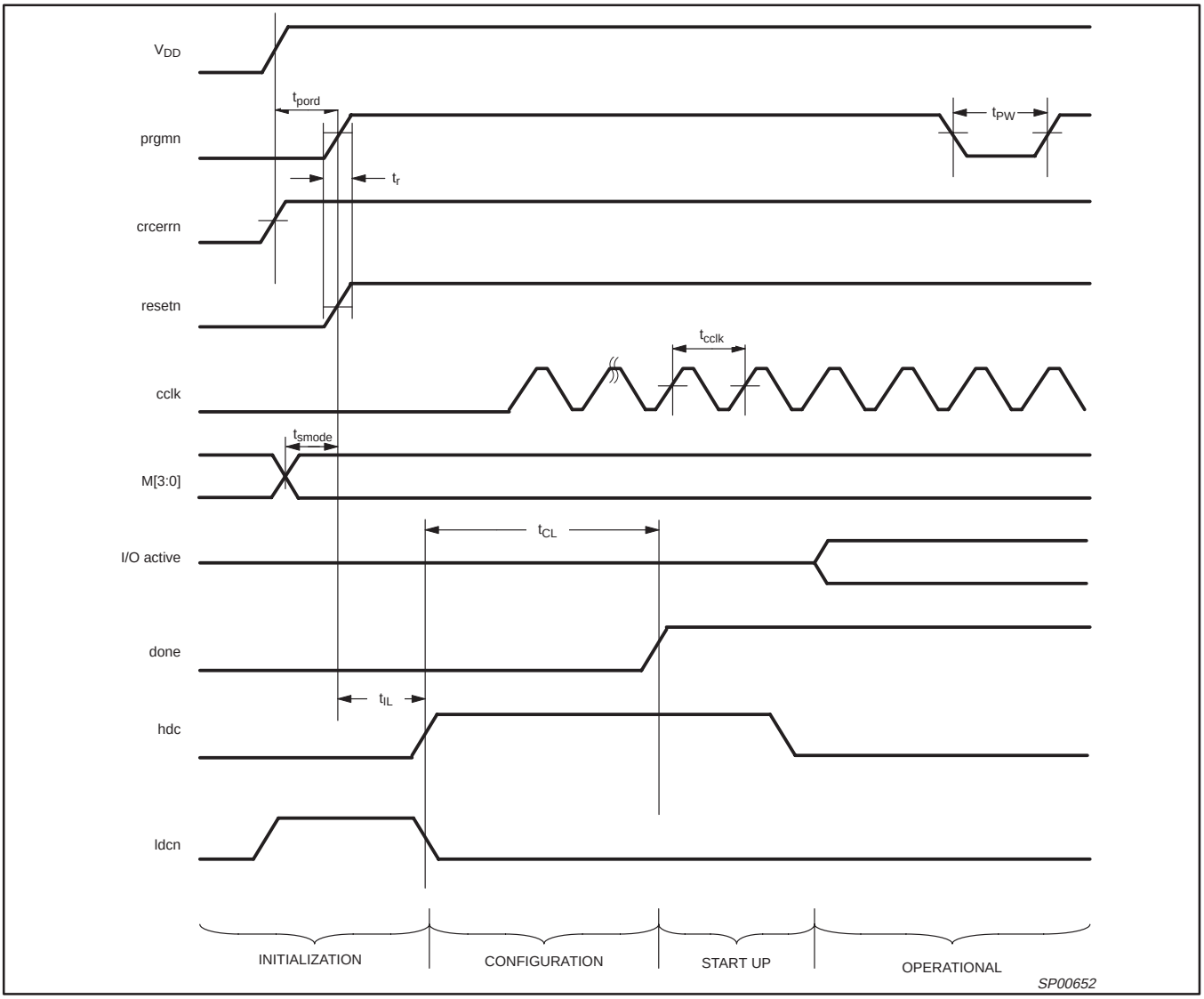


Figure 9. General configuration mode timing diagram

Table 4. General configuration mode timing characteristics

SYMBOL	PARAMETER		MIN	MAX	UNIT
All configuration modes					
t_{SMODE}	M[3:0] setup time to prgmn high		0	–	ns
t_{HMODE}	M[3:0] hold time from done high		10	–	µs
t_{PW}	prgmn pulse width low		50	–	ns
t_{gtsr}	Global 3-state disable			40	ns
t_{IL}	Initialization latency (prgmn high to hdc high) PZ3960	M3 = 1	250	700	ns
t_{PORD}	Power-on reset delay		1		µs
t_r	Configuration signal rise time		–	1.0	µs
Master modes					
t_{CCLK}	cclk period	M3 = 1	714	1667	ns
t_{CL}	Configuration latency (non-compressed) PZ3960	M3 = 1	404	943	ms
Slave serial, slave parallel, and Synchronous peripheral modes					
t_{CCLK}	cclk period	Single device	100	–	ns
		Daisy-chain	1000	–	ns
t_{CL}	Configuration latency (non-compressed) PZ3960	Single device	57	–	ms
		Daisy-chain	566	–	ms

Initialization

Upon power-up, the device goes through an initialization process. First, an internal power-on-reset circuit is triggered when power is applied. When V_{DD} reaches the voltage at which portions of the PZ3960 begin to operate (1.5V), the configuration pins are set to be inputs or outputs based on the configuration mode, as determined by the mode select inputs M[2:0]. The mode pins must be stable t_{smode} nanoseconds before the rising edge of prgmn or resetn. A time-out delay is initiated when V_{DD} reaches between 1.0V and 2.0V to allow the power supply voltage to stabilize. The done output is low. At power-up, if the power supply does not rise from 1.0V to V_{DD} in less than 25ms, the user should delay configuration by inputting a low into prgmn or resetn until V_{DD} is greater than the recommended minimum operating voltage (3.0V for commercial devices). If prgmn has a rise time of greater than one microsecond, resetn must be held low until after prgmn goes high. If the rise time for prgmn is 1 microsecond or less, the order in which these pins go high is arbitrary.

The High During Configuration (hdc), Low During Configuration (ldcn), and done signals are active outputs in the PZ3960's initialization and configuration states. hdc, ldcn, and done can be used to provide control of external logic signals such as reset, bus enable, or EEPROM enable during configuration. For master parallel configuration mode, these signals provide EEPROM enable control and allow the data pins to be shared with user logic signals.

If configuration has begun, an assertion of resetn or prgmn initiates an abort, returning the PZ3960 to the initialization state. The resetn and prgmn pins must be high before the PZ3960 will enter the configuration state, and the mode pins must be stable t_{smode} nanoseconds before they rise. During the start-up and operating states, only the assertion of prgmn causes a re-configuration.

During initialization and configuration, all I/O's are 3-stated and the internal weak pull-downs are active. See the section on terminations for more information.

Start-up

After configuration, the PZ3960 enters the start-up phase. This phase is the transition between the configuration and operational states. This transition occurs within three cclk cycles of the done pin going high (it is acceptable to have additional cclk cycles beyond the three required). The system design task in the start-up phase is to ensure that multi-function pins (see pin function on page 34) transition from configuration signals to user definable I/Os without inadvertently activating devices in the system or causing bus contention. The done signal goes high at the beginning of the start up phase, which allows configuration sources to be disconnected so that there is no bus contention when the I/Os become active. In addition to controlling the PZ3960 during start-up, additional start-up techniques to avoid contention include using isolation devices between the PZ3960 and other circuits in the system, re-assigning I/O locations, and keeping I/Os 3-stated until contentions are resolved. For example, Figure 10 shows how to use the global tri-state (gts) signal to avoid signal contention when any multi-function pins are used as I/O after configuration is finished. Holding gts high until after the multi-function pins are disconnected from the driving source allows these pins to transition from configuration pins to user definable I/O without signal contention. In this case, the I/O become active a t_{gtsr} delay after the gts pin is pulled low.

The flip-flops are reset one cycle after done goes high so that operation begins in a known state. The done outputs from multiple PZ3960s can be wire ANDed and used as an active-high ready signal, to disable PROMs with active-low enable(s), or to reset to other parts of the system (see Figure 27).

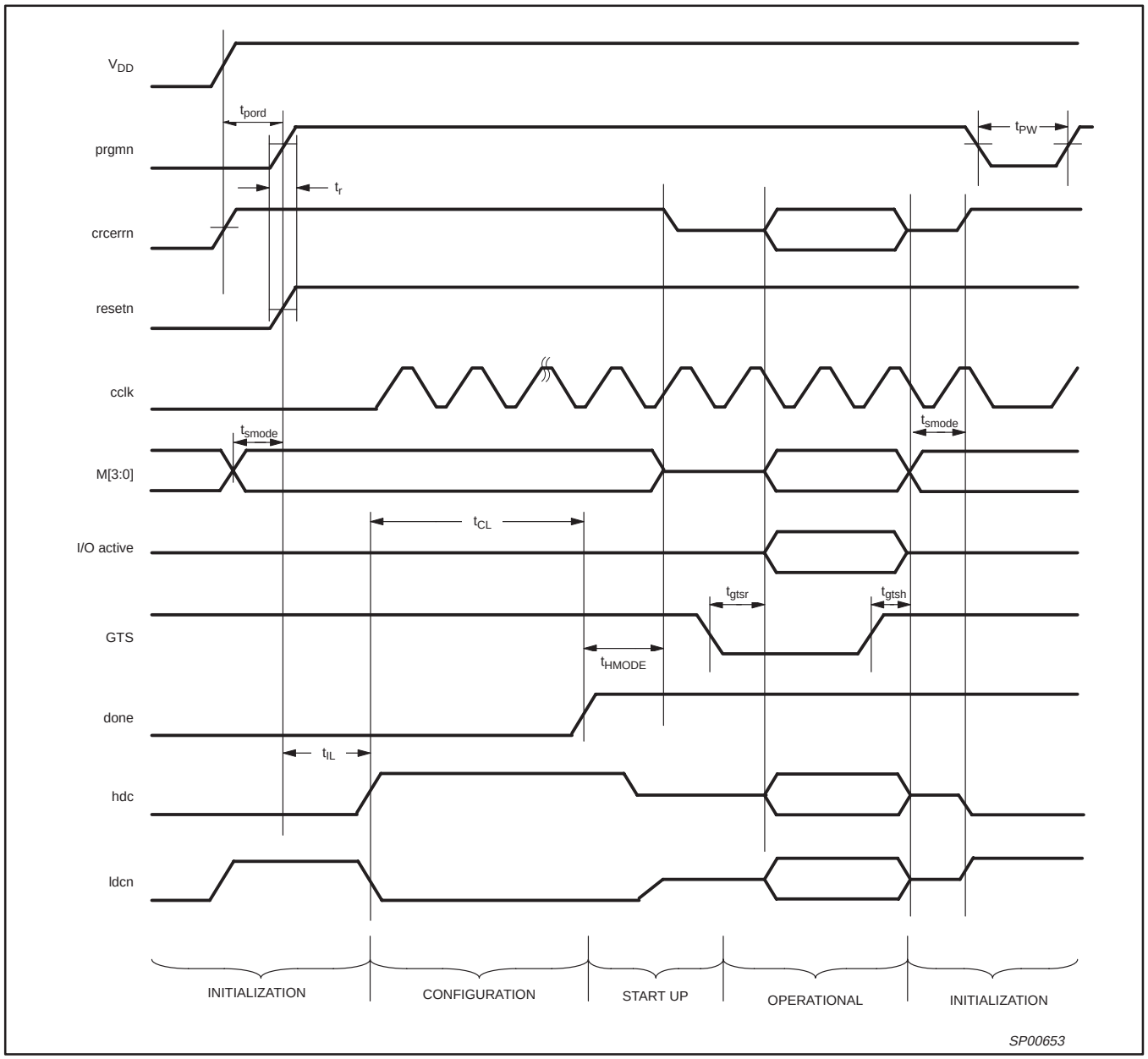


Figure 10. Using gts signal with power up to avoid signal contention with multi-function pins used as I/O

CONFIGURATION DATA FORMAT OVERVIEW

The PZ3960 functionality is determined by the state of internal configuration RAM. This section discusses the configuration data format, and the function of each field in configuration data packets.

Configuration Data Packets

Configuration of the PZ3960 is done using configuration packets. The configuration packet is shown in Figure 11. The data packet consists of a header and a data frame. There are four types of data frames. The header is shifted into the device first, followed by one data frame. Configuration of a single PZ3960 requires 1010 data packets, one for each address. All preceding data must contain only 1s. Once a device is configured, it re-transmits data of any polarity. Before and during configuration, all data re-transmitted out the daisy-chain port (dout) are 1s.

The ordering of the data packets may be random, but they cannot be mixed with other devices' data packets. Alignment bits are not required between data packets. If used, alignment bits must be included in the length count, and they must be at least 2 bits long.

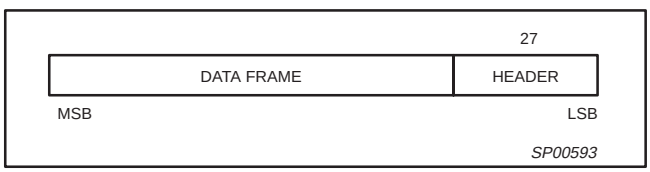


Figure 11. Data Packet

Table 5. Configuration Frame Size

DEVICE	PZ3960
Number of frames	1010
Data bits/standard frame	560
Data bits/compressed frame	14
Data bits/user_code frame	560
Data bits/isc_code frame	560
Maximum configuration data— # bits/frame × # frames	565600

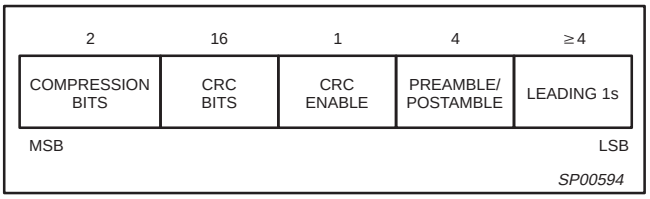


Figure 12. 27-bit Header

The header is fixed and consists of five fields:
– Leading 1s,
– Preamble,
– CRC Enable,
– CRC Bits,
– Compression Bits.

The leading 1s enter the device first. The following is a description of each field in the header.

Leading 1s:
This is a four or greater bit field consisting of 1s.

Preamble/Postamble:
This is a four bit field which indicates the start of a frame or the end of configuration:
Preamble: 0010 – signals the beginning of a configuration data packet
Postamble: 0100 – signals the end of configuration
All other values of the preamble field force configuration of the entire system to restart.

The segments CRC Enable, CRC Bits, and Compression Bits are valid only if the Preamble field is 0010.

Cyclic Redundancy Check (CRC) Enable:
In this single bit field, a 0 disables CRC checking of the data stream. If the CRC is disabled the 16 bit CRC field must be the default described below. A 1 enables CRC error checking of the data stream.

CRC Error Checking:
The CRC field is a 16 bit field. The default value is 1010_1010_1010_1010. The calculated value is from data, address, stop bit, and first alignment bit (starting with crc_reg[15:0] = [0]). Using verilog operators, the crc is calculated as:

```
crc_reg[14:2] <= cr_reg[14:2] << 1;
cr_reg[2] <= cr_reg[15]^din^cr_reg[1];
cr_reg[1] <= cr_reg[0];
cr_reg[0] < cr_reg[15]^din;
cr_reg[15] <= cr_reg[15]^din^cr_reg[14];
```

If a CRC error is detected, configuration is halted and must be restarted.

Compression Bits:
This 2-bit field defines the use of compression of the data packets.
00 – Standard mode:
The data packet contains both address and data
01 – Reset mode:
The data packet contains only the address field.
This pattern causes the configuration register to be reset.
10 – Hold mode:
The data packet contains only the address field.
This pattern causes the configuration register to hold its value.
11 – Set mode:
The data packet contains only the address field.
This pattern causes the configuration register to be set.

Data Frames

The four types of data frames are standard, compressed, user_code, and isc_code. All fields must be completely filled, with 1s used to fill unused bits. The definition of each frame is described below:

Standard frame

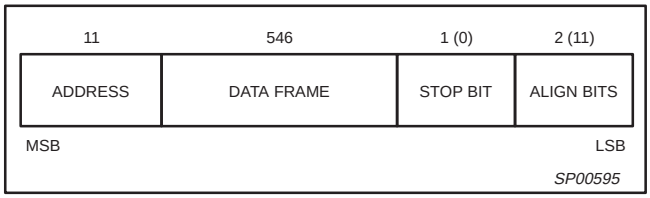


Figure 13. Standard Frame

Address:
This is an 11 bit filed for providing 1011 (1008 SRAM plus 3 user) addresses.

Data:
546 bit field.

Stop bit:
This is a one bit field which must be 0.

Align bit:
This is a two bit field which must be 11.

Compressed frame

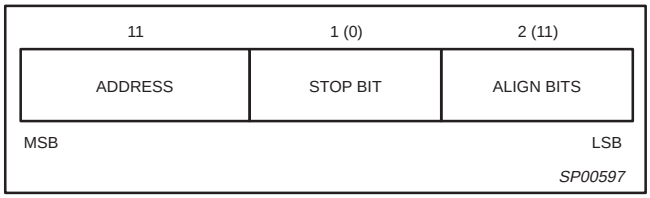


Figure 14. Compressed Frame

The compressed frame contains no data.

User code frame
The user code is located at address 1008D.

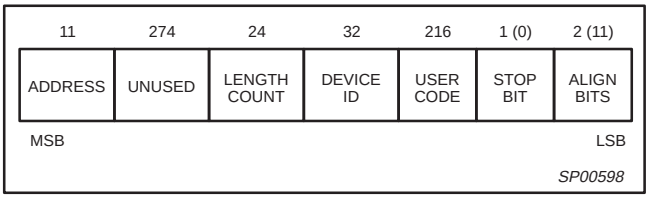


Figure 15. User code Frame

Length count:
This is a 24 bit field containing the length of the data stream transmitted to configure all of the devices in the daisy chain. This field is only used by a PZ3960 if it is in the master mode.

Device ID:
This is a 32-bit field containing PZ3960 device ID:
492 SBGA: 0000_001_001_101000_1_000_00000010101_1

User code:
This is a 216 bit field reserved for user information.

ISC code frame
The isc_code address is 1009.

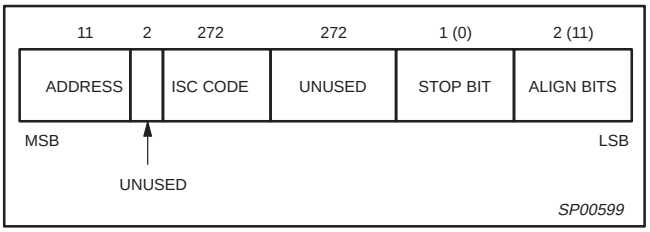


Figure 16. ISC Frame

The ISC frame allows the user to write an ISC code to the device.

Re-configuration

To reconfigure the PZ3960 when the device is operating in the system, a low pulse is input into prgmn. The I/Os not used for configuration are 3-Stated. The PZ3960 then samples the mode select inputs and begins re-configuration. The mode pins are continuously sampled, so the signals must be stable while prgmn is low. When configuration is compete, done is released, allowing it to be pulled high.

CRC Error Checking

CRC checking is done on each frame if enabled by setting the CRCen bit in the header. If there is an error, a CRC error is flagged by pulling crcerrn low. The PZ3960 is forced into the initialization state, and then moves into the configuration state after prgmn and resetn go high. The PZ3960 will also pull crcerrn low if an invalid preamble is detected within a configuration data packet.

PZ3960 CONFIGURATION MODES

The method for configuring the PZ3960 is selected by the m0, m1, and m2 inputs. The m3 input should be high for all modes. In master modes, cclk is an output with a nominal frequency of 1 MHz. In slave modes, cclk is an input with a maximum frequency of 10 MHz if configuring only a single device, and 1 MHz if devices are daisy chained.

Master Serial Mode

In the master serial mode, the PZ3960 loads the configuration data from an external serial ROM. The configuration data is either loaded automatically at start-up or on a command to reconfigure. Serial EEPROMs from Altera, Atmel, Lucent, Microchip, and Xilinx can be used to configure the PZ3960 in the master serial mode. This provides a simple four-pin interface in an eight-pin package. Serial EEPROMs are available in 32K, 64K, 128K, 256K, and 1M bit densities.

Configuration in the master serial mode can be done at power-up and/or upon a configure command. The system or the PZ3960 must activate the serial EEPROM's $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ inputs. At power-up, the PZ3960 and serial EEPROM each contain internal power-on reset circuitry which allows the PZ3960 to be configured without the system providing an external signal. The power-on reset circuitry causes the serial EEPROMs' internal address pointer to be reset. After power-up, the PZ3960 automatically enters its initialization phase.

The serial EEPROM/PZ3960 interface used depends on such factors as the availability of a system reset pulse, availability of an intelligent host to generate a configure command, whether a single serial EEPROM is used or multiple serial ROMs are cascaded, whether the serial EEPROM contains a single or multiple configuration programs, etc.

Data is read into the PZ3960 sequentially from the serial ROM. The DATA output from the serial EEPROM is connected directly into the din input of the PZ3960. The cclk output from the PZ3960 is connected to the CLOCK input of the serial EEPROM. During the configuration process, cclk clocks one data bit into the PZ3960 on each rising edge.

Since the data and clock are direct connects, the PZ3960/serial EEPROM interface task is to use the system or PZ3960 to enable the $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ of the serial EEPROM(s). The serial EEPROM's $\overline{\text{RESET}}$/OE is programmable to function with $\overline{\text{RESET}}$ active-low and OE active-high, which allows hdc from the PZ3960 to control this function.

Likewise, the serial EEPROM could be programmed to function with RESET active high and $\overline{\text{OE}}$ active low, allowing the ldcn pin from the PZ3960 to control this function. The PZ3960 done pin is connected to the serial EEPROM $\overline{\text{CE}}$ to enable the EEPROMs during configuration and disable them when configuration is complete.

In Figure 17, the serial EEPROMs $\overline{\text{RESET}}$/OE pin has been programmed to function with $\overline{\text{RESET}}$ active low and OE active high, and it is controlled by the PZ3960's hdc pin. This resets the serial EEPROMs during the initialization state and enables their output during the configuration state. If a bit error is found during configuration, hdc will go low, signifying the PZ3960 is back in initialization state and also resetting the EEPROMs. This restarts the configuration process.

The PZ3960 done pin is routed to the $\overline{\text{CE}}$ pin of the EEPROMs. The low signal on done during configuration enable the serial EEPROMs. At the completion of configuration, the high on done disables the EEPROMs.

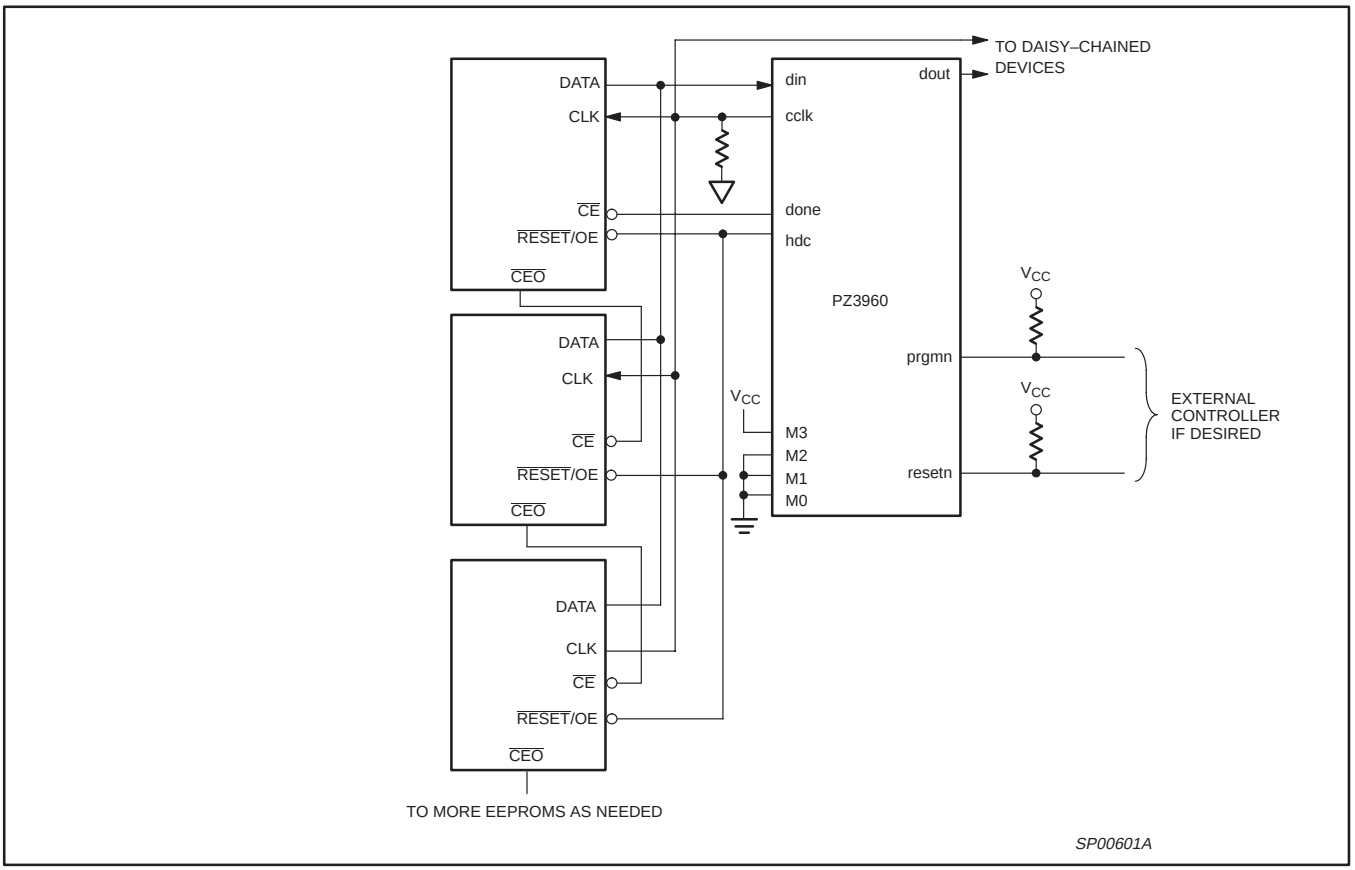


Figure 17. Master Serial Configuration

In Figure 17, three serial EEPROMs are cascaded to configure a PZ3960. When configuration data requirements exceed the capacity of a single serial EEPROM, multiple serial EEPROMs can be cascaded to support the configuration of a single (or multiple) PZ3960(s). After the last bit from the first serial ROM is read, the serial ROM outputs $\overline{CEO}$ low and 3-States the DATA output. The next serial ROM recognizes the low on $\overline{CE}$ input and outputs configuration data on the DATA output. After configuration is complete, the PZ3960's done output into $\overline{CE}$ disables the serial EEPROMs.

In applications in which a serial EEPROM stores multiple configuration programs, the subsequent configuration program(s) are stored in EEPROM locations that follow the last address for the previous configuration program. The user must ensure that the serial EEPROMs address pointer is not reset, causing the first device configuration to be reloaded.

Contention on the PZ3960's din pin must be avoided. During configuration, din receives configuration data. After configuration, it is a user I/O.

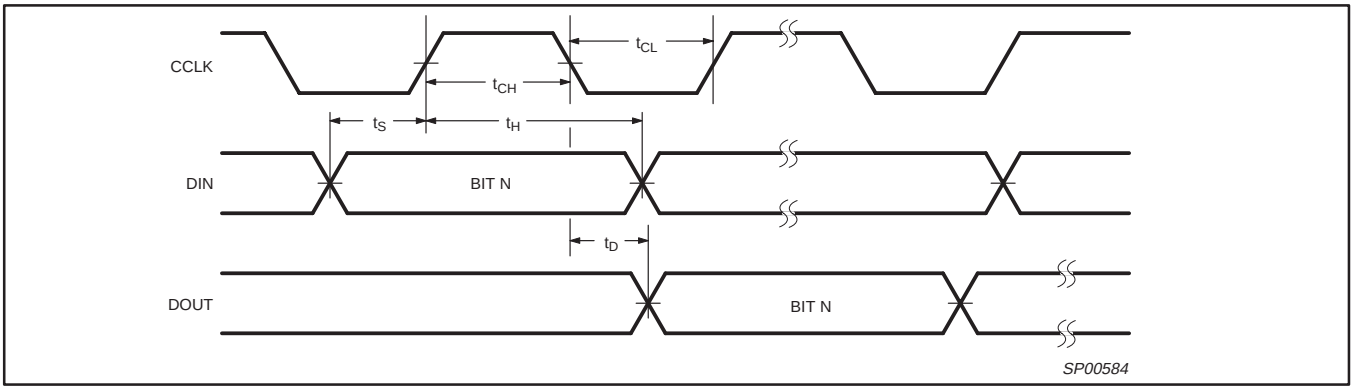


Figure 18. Master Serial Configuration Mode Timing Diagram

Table 6. Master serial configuration mode timing characteristics

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
t_S	din setup time		60	–	–	ns
t_H	din hold time		0	–	–	ns
t_D	cclk to dout delay		–	–	300	ns
t_{CL}	cclk low time	M3 = 1	357	500	833	ns
t_{CH}	cclk high time	M3 = 1	357	500	833	ns
t_C	cclk frequency	M3 = 1	0.6	1.0	1.4	MHz

Master Parallel Mode

The master parallel configuration mode is generally used to interface to industry-standard byte-wide memory such as 256K and larger EEPROMs. Figure 19 provides the interface for master parallel mode. The PZ3960 outputs a 20-bit address on A[19:0] to memory and reads one byte of configuration data every eighth cclk. The parallel bytes are internally serialized starting with the least significant bit, D0. The starting memory address is 00000 Hex and the PZ3960 increments the address for each byte loaded. The starting address is output when the device enters the configuration state. The PZ3960 latches the data byte on the second rising edge of CCLK. This next data byte is latched in the PZ3960 seven cclk cycles later.

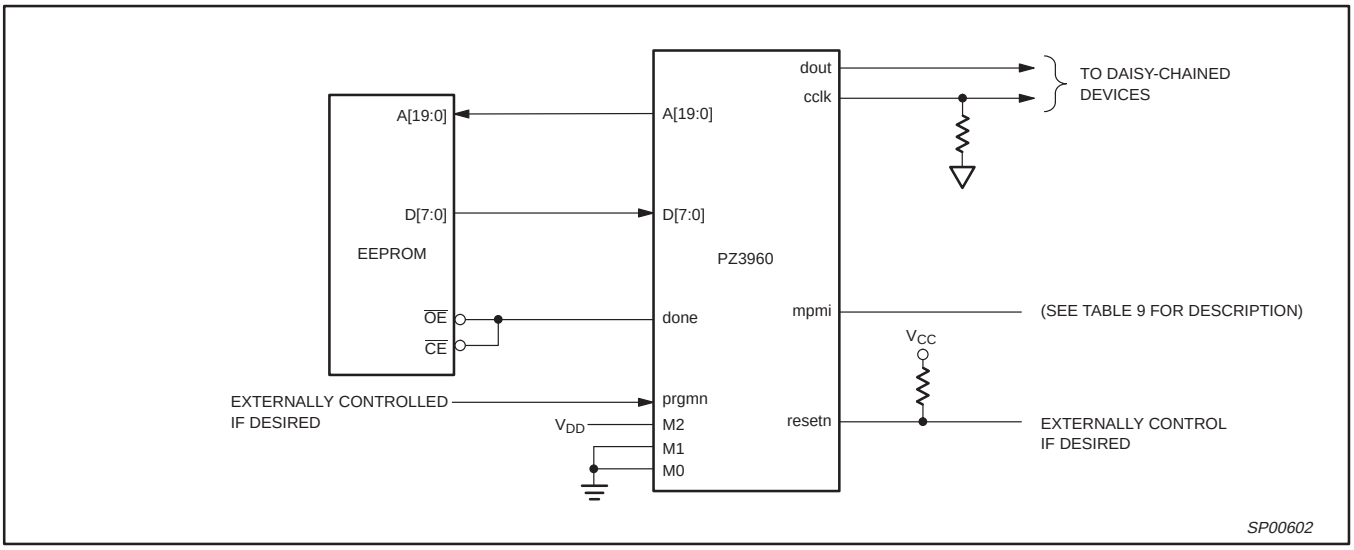


Figure 19. Master Parallel Configuration

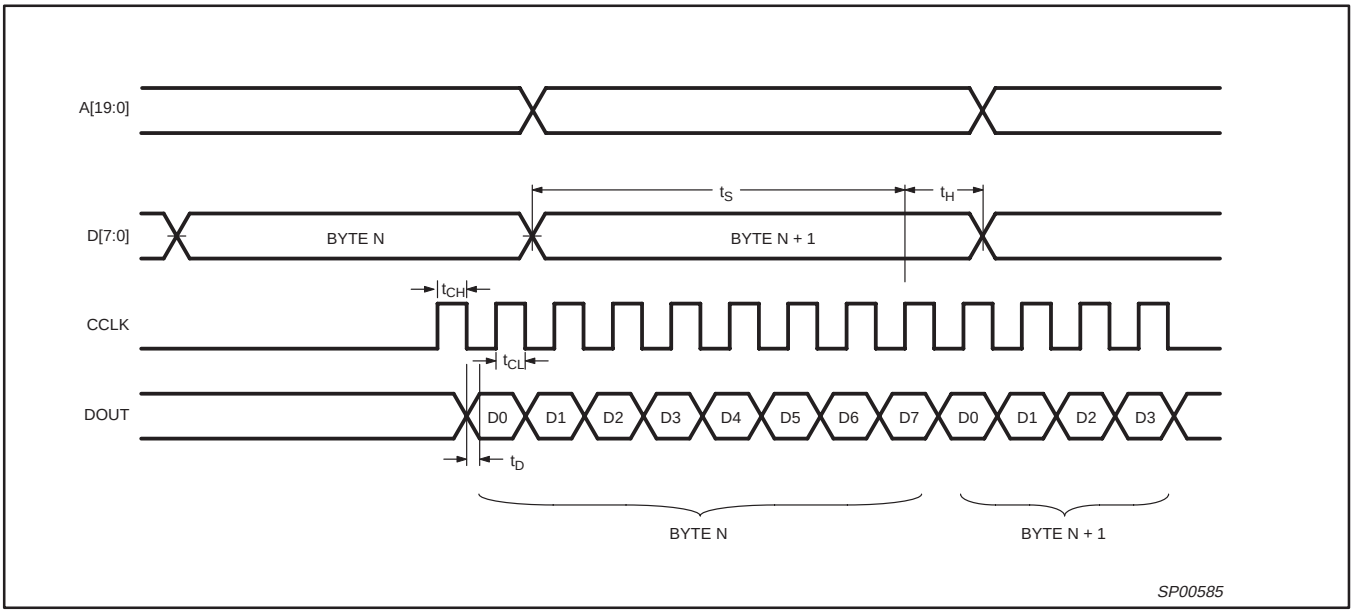


Figure 20. Master Parallel Configuration Mode Timing Diagram

Table 7. Master parallel configuration mode timing characteristics

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
t_{AV}	cclk to address valid		0	–	200	ns
t_S	D[7:0] setup time to cclk high		60		–	ns
t_H	D[7:0] hold time from cclk high		0		–	ns
t_{CL}	cclk low time	M3 = 1	357	500	833	ns
t_{CH}	cclk high time	M3 = 1	357	500	833	ns
t_D	cclk to dout delay		–		300	ns
f_C	cclk frequency	M3 = 1	0.6	1.0	1.4	MHz

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the cclk input. The first data byte is clocked in on the second cclk after hdc goes high. Subsequent data bytes are clocked in on every eighth rising edge of cclk. The process repeats until all of the data is loaded into the PZ3960. The serial data begins shifting out on dout 0.5 cycles after the parallel data was loaded. It requires additional cclks after the last byte is loaded to complete the shifting. Figure 21 shows the interface for synchronous peripheral mode. When configuring a single device, the frequency of cclk can be up to 10 MHz. As with master modes, this mode can be used for the lead PZ3960 for daisy-chained devices. Note that the cclk frequency for daisy-chained operation is limited to 1 MHz.

Also note that CS1 is a multi-function pin, which means that it is available as a user I/O during normal device operation. As with all user I/O on the PZ3960, CS1 has an internal pull-down resistor that is automatically activated if the I/O pin is not used (see section on terminations for more information). If CS1 is left attached to V_{CC} after configuration, and it is not used as an I/O, the internal pull-down must be disabled or a path from V_{CC} to ground is created. To disable the pull-down, use the XPLA property statement '*signal name:pin number* tri-state' to disable the resistor.

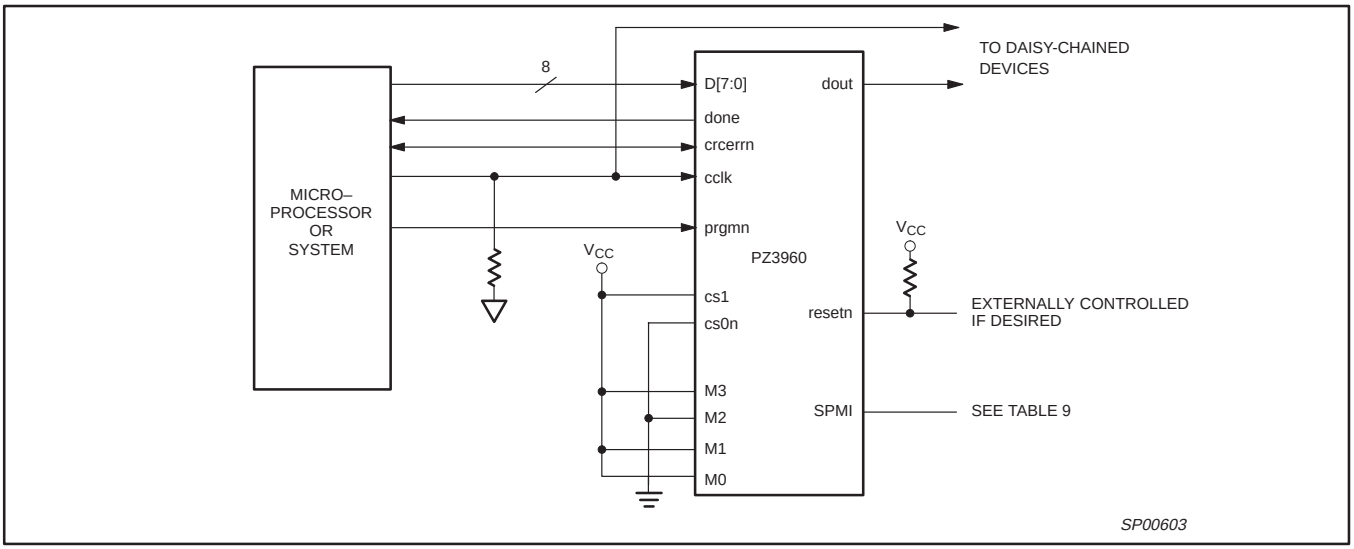


Figure 21. Synchronous Peripheral Configuration

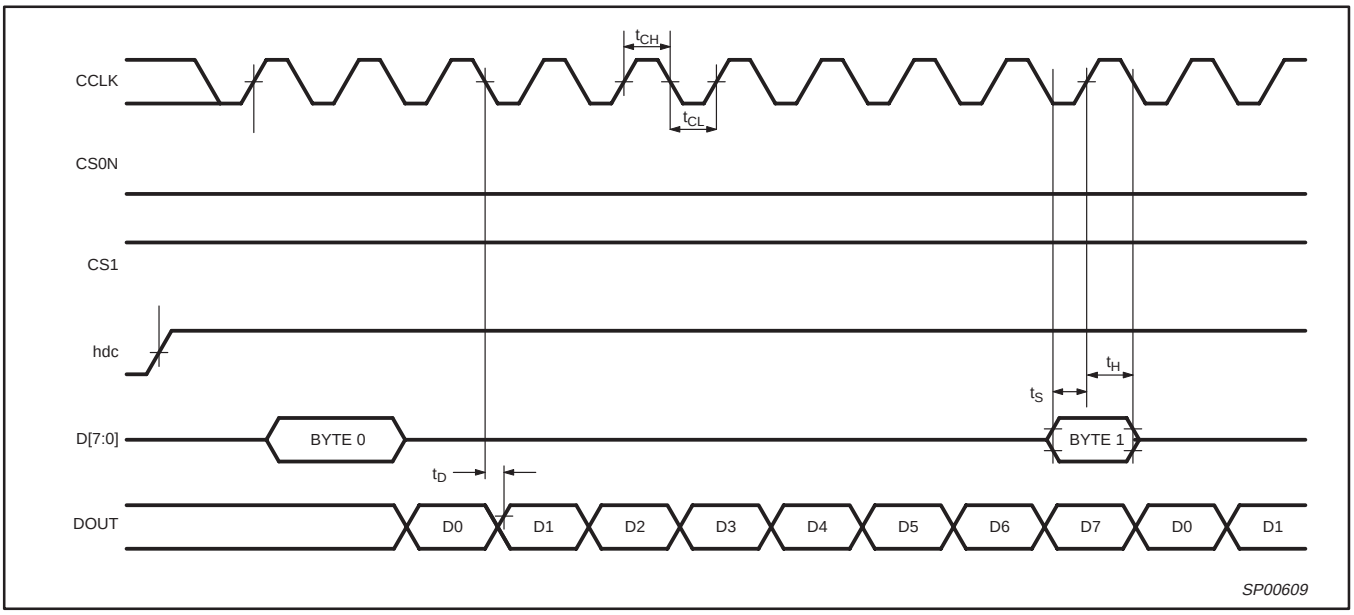


Figure 22. Synchronous Peripheral Configuration Mode Timing Diagram

Table 8. Synchronous peripheral configuration mode timing characteristics

SYMBOL	PARAMETER		MIN	MAX	UNIT
t_S	D[7:0] setup time		20	0	ns
t_H	D[7:0] hold time		0	–	ns
t_{CH}	cclk high time	Single device	50	–	ns
		Daisy-chain device	500	–	ns
t_{CL}	cclk low time	Single device	50	–	ns
		Daisy-chain device	500	–	ns
f_C	cclk frequency	Single device	–	10	MHz
		Daisy-chain device	–	1	MHz

Slave Serial Mode

Figure 23 shows the interface for the slave serial configuration mode. The configuration data is provided into the PZ3960's din input synchronous with the cclk input. After the PZ3960 has loaded its configuration data, it re-transmits incoming configuration data on dout. When configuring a single device, the frequency of cclk can be up to 10 MHz.

A device in slave serial mode can be used as the lead device in a daisy-chain. When used in daisy-chained operation, cclk is routed into all slave serial mode devices in parallel and the frequency is limited to 1 MHz. The dout pin of the lead device is connected to the din pin of the next device and so on. In daisy-chained operation, all downstream devices use slave serial mode regardless of the configuration mode of the lead device.

Multiple slave PZ3960s can be loaded with identical configurations simultaneously. This is done by loading the configuration data into the din inputs in parallel.

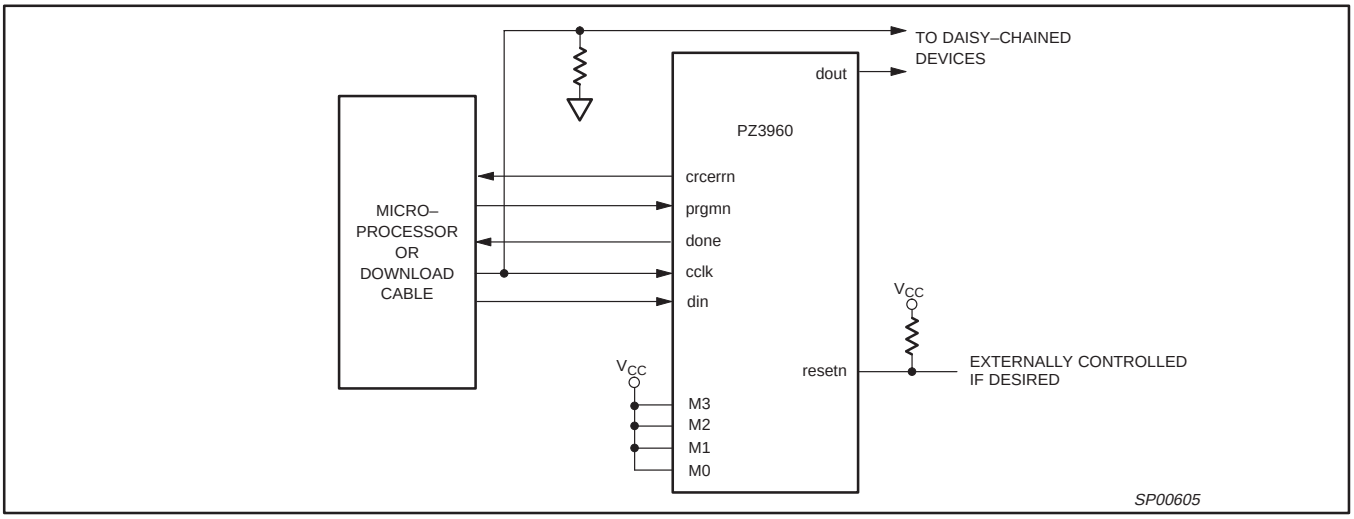


Figure 23. Slave Serial Configuration Schematic

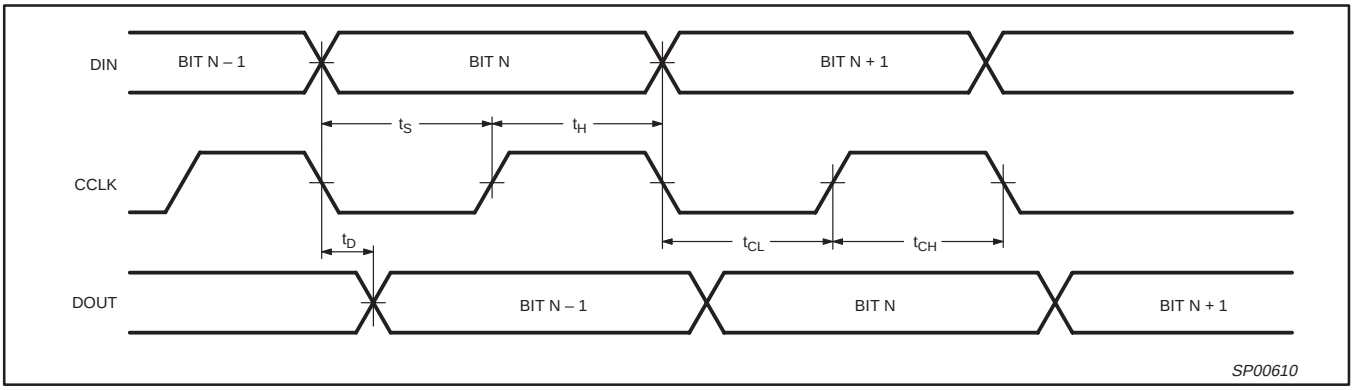


Figure 24. Slave Serial Configuration Mode Timing Diagram

Table 9. Slave serial configuration mode timing characteristics

SYMBOL	PARAMETER		MIN	MAX	UNIT
t_S	din setup time		20	0	ns
t_H	din hold time		0	–	ns
t_{CH}	cclk high time	Single device	50	–	ns
		Daisy-chain device	500	–	ns
t_{CL}	cclk low time	Single device	50	–	ns
		Daisy-chain device	500	–	ns
f_C	cclk frequency	Single device	–	10	MHz
		Daisy-chain device	–	1	MHz

Slave Parallel Mode

The slave parallel mode is essentially the same as the synchronous peripheral mode, except that the chip select pins (cs1 and cs0n) are not used. As in the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the cclk input. The first data byte is clocked in on the second cclk after hdc goes high. Subsequent data bytes are clocked in on every eighth rising edge of cclk. The process repeats until all of the data is loaded into the PZ3960. The serial data begins shifting out on dout 0.5 cycles after the parallel data was loaded. It requires additional cclks after the last byte is loaded to complete the shifting. Figure 25 shows the interface for slave parallel mode. When configuring a single device, the frequency of cclk can be up to 10 MHz.

As with synchronous peripheral mode, the slave parallel mode can be used as the lead PZ3960 for daisy-chained devices. Note that the cclk frequency for daisy-chain operation is limited to 1 MHz.

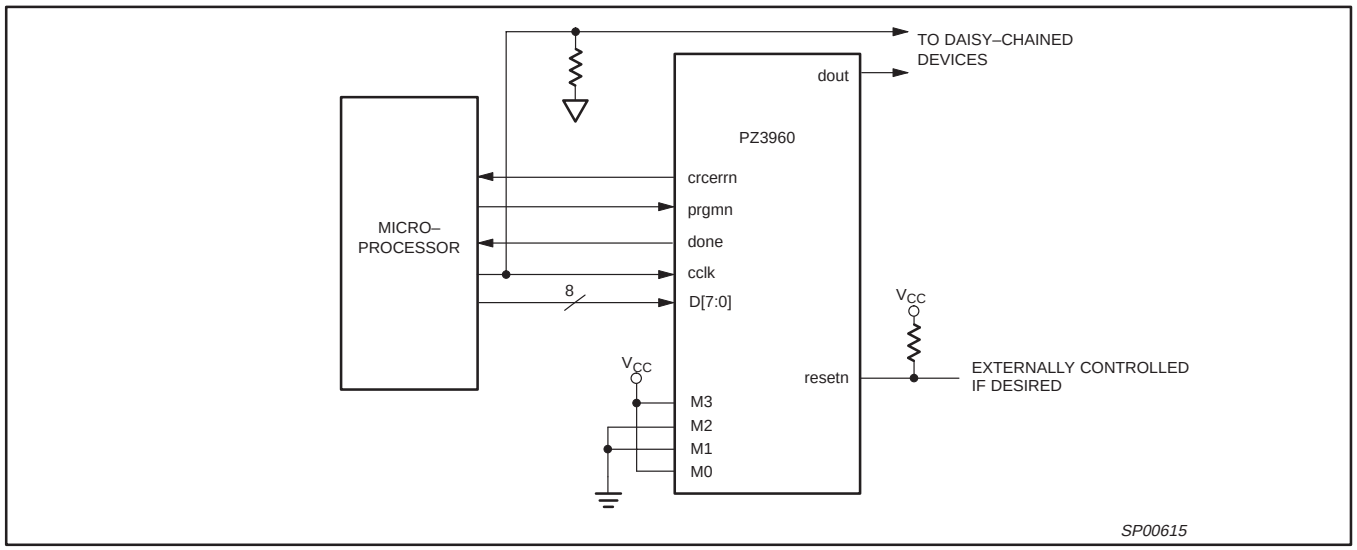


Figure 25. Slave Parallel Configuration Schematic

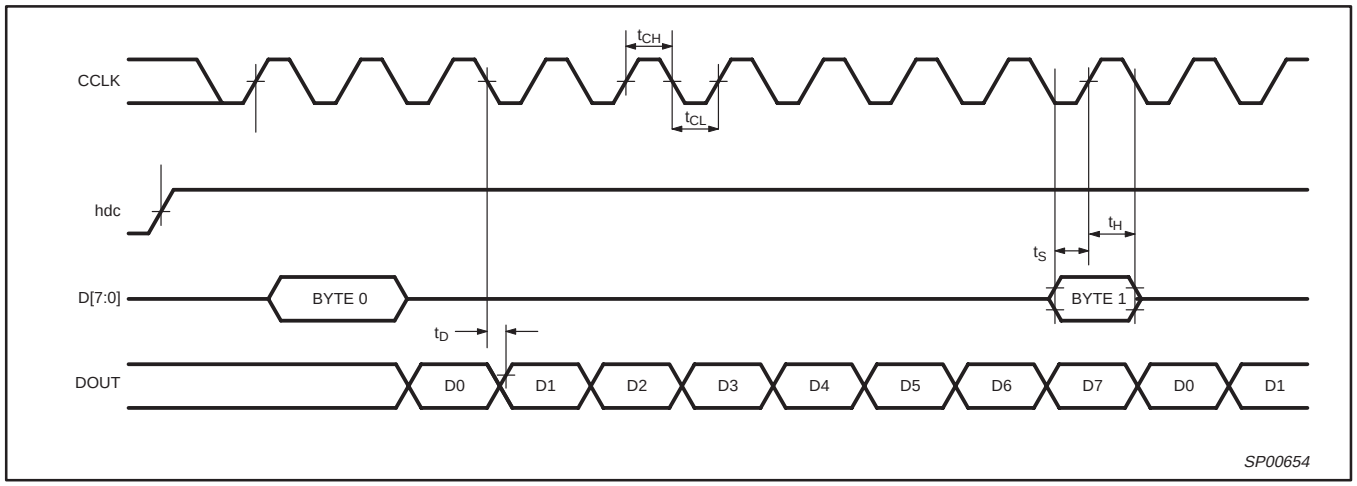


Figure 26. Slave Parallel Configuration Mode Timing Diagram

Table 10. Slave parallel configuration mode timing characteristics

SYMBOL	PARAMETER		MIN	MAX	UNIT
t_S	D[7:0] setup time		20	0	ns
t_H	D[7:0] hold time		0	–	ns
t_{CH}	cclk high time	Single device	50	–	ns
		Daisy-chain device	500	–	ns
t_{CL}	cclk low time	Single device	50	–	ns
		Daisy-chain device	500	–	ns
f_C	cclk frequency	Single device	–	10	MHz
		Daisy-chain device	–	1	MHz

DAISY CHAIN OPERATION

Multiple PZ3960s can be configured by using a daisy-chain of PZ3960s. Daisy-chaining uses a lead PZ3960 and one or more PZ3960s configured in slave serial mode. The lead PZ3960 can be configured in any mode. Figure 27 shows the connections for loading multiple PZ3960s in a daisy-chain configuration with the lead devices configured in master parallel mode. Figure 28 shows the connections for loading multiple PZ3960's with the lead device configured in master serial mode.

Daisy-chained PZ3960s are connected in series. An upstream PZ3960 which has received the preamble outputs a high on dout, ensuring that downstream PZ3960s do not receive frame start bits. When the lead device receives the postamble, its configuration is complete. At this point, the configuration RAM of the lead device is full and its done pin is released. The lead device continues to load configuration data until the internal frame bit counter reaches the length count or all the done pins of the chain have gone high. Since the configuration RAM of the lead device is full, this data is shifted out serially to the downstream devices on the dout pin. As the configuration is completed for the downstream devices, each will release its done pin. Because the done pins of each device in the chain are wire-anded together, the done pin will be pulled high when all devices in the daisy-chain have completed configuration. All devices now move to the start-up state simultaneously.

The generation of cclk for the daisy-chained devices which are in slave serial mode differs depending on the configuration mode of the lead device. A master parallel mode device uses its internal timing generator to produce an internal cclk. If the lead device is configured in either synchronous peripheral, slave serial mode, or slave parallel mode, cclk is an input and is mated to the lead device and to all of the daisy-chained devices in parallel. The configuration data is read into din of slave devices on the positive edge of cclk, and shifted out dout on the negative edge of cclk. Note that daisy-chain operation is limited to a cclk frequency of 1 MHz. If a CRC error or an invalid preamble is detected by a slave device, crcerrn will be pulled low and in turn pull prgmn low, halting configuration for all devices. If a CRC error is detected by the master device, hdc will be pulled low, resetting the EEPROM to the first address and restarting configuration.

The development software can create a composite configuration file for configuring daisy-chained PZ3960s. The configuration data consists of multiple concatenated data packets.

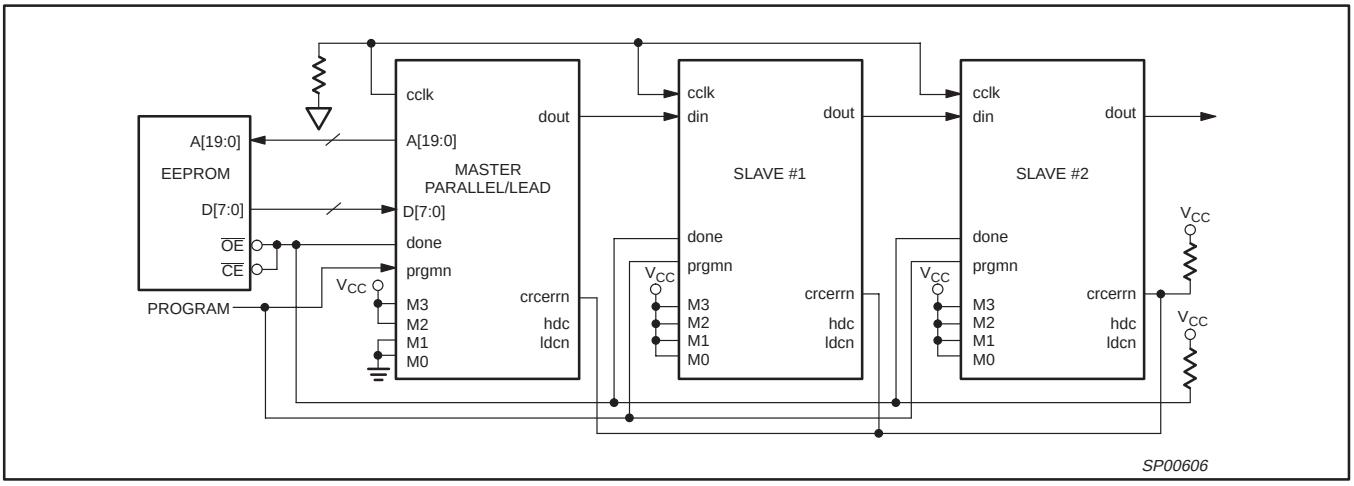


Figure 27. Daisy-chain Schematic with lead device in master parallel

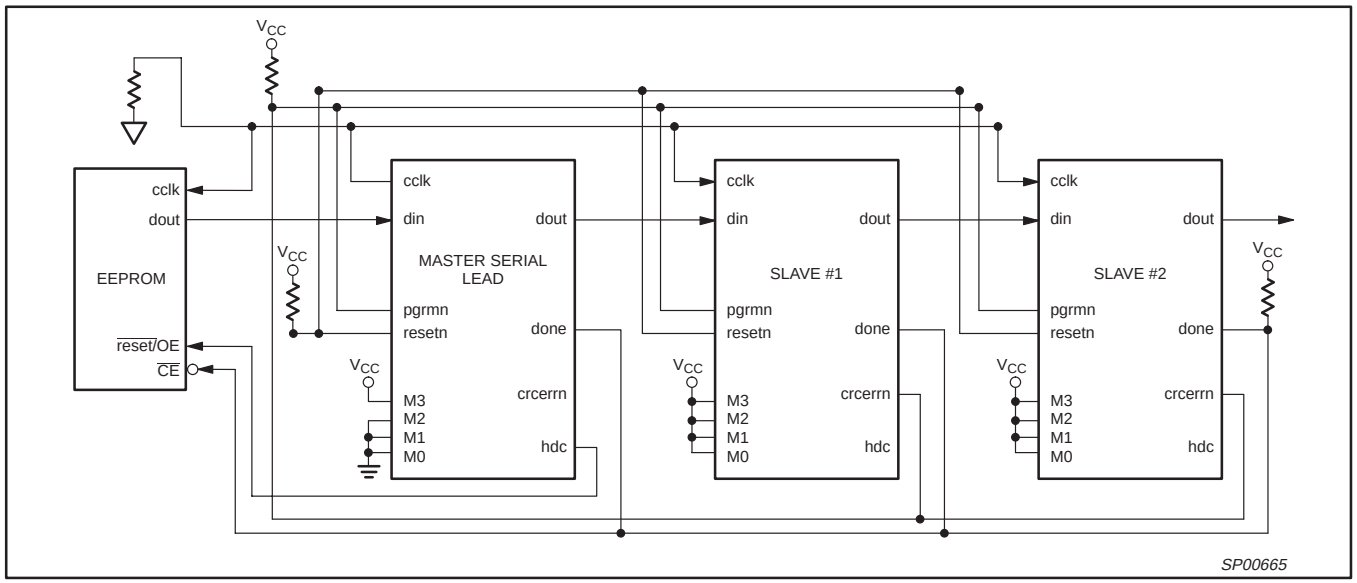


Figure 28. Daisy Chain Schematic with Master Serial Lead Device

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. BST provides the ability to test the external connections of a device, test the internal logic of the device, and capture data from the device during normal operation. BST provides a number of benefits in each of the following areas:

- Testability
  - Allows testing of an unlimited number of interconnects on the printed circuit board
  - Testability is designed in at the component level
  - Enables desired signal levels to be set at specific pins (Preload)
  - Data from pin or core logic signals can be examined during normal operation
- Reliability
  - Eliminates physical contacts common to existing test fixtures (e.g., “bed-of-nails”)
  - Degradation of test equipment is no longer a concern
  - Facilitates the handling of smaller, surface-mount components
  - Allows for testing when components exist on both sides of the printed circuit board
- Cost
  - Reduces/eliminates the need for expensive test equipment
  - Reduces test preparation time
  - Reduces spare board inventories

The Philips PZ3960’s JTAG interface includes a TAP Port and a TAP Controller, both of which are defined by the IEEE 1149.1 JTAG Specification. As implemented in the Philips PZ3960, the TAP Port includes five pins (refer to Table 11) described in the JTAG specification: tck, tms, tdi, tdo, and trstn. These pins should be connected to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

Table 12 defines the dedicated pins used by the mandatory JTAG signals for the PZ3960.

The JTAG specifications define two sets of commands to support boundary-scan testing: high-level commands and low-level commands. High-level commands are executed via board test software on an a user test station such as automated test equipment, a PC, or an engineering workstation (EWS). Each high-level command comprises a sequence of low level commands. These low-level commands are executed within the component under test, and therefore must be implemented as part of the TAP Controller design. The set of low-level boundary-scan commands implemented in the PZ3960 is defined in Table 13. By supporting this set of low-level commands, the PZ3960 allows execution of all high-level boundary-scan commands.

Table 11. JTAG Pin Description

PIN	NAME	DESCRIPTION
tck	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the tdi and tdo pins, respectively. tck is also used to clock the TAP Controller state machine.
tms	Test Mode Select	Serial input pin selects the JTAG instruction mode. tms should be driven high during user mode operation.
tdi	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of tck.
tdo	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of tck. The signal is tri-stated if data is not being shifted out of the device.
trstn	Test Reset	Forces TAP controller to test logic reset state. This signal is active low.

Table 12. PZ3960 JTAG Pinout by Package Type

DEVICE	(PIN NUMBER / MACROCELL #)				
	tck	tms	tdi	tdo	trstn
PZ3960 492 pin PBGA	P4	N4	P1	P3	N3

Table 13. PZ3960 Low-Level JTAG Boundary-Scan Commands

INSTRUCTION (Instruction Code) *Register Used*	DESCRIPTION
SAMPLE/PRELOAD (00010) *Boundary-Scan Register*	The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan Shift-Register prior to selection of the other boundary-scan test instructions.
EXTEST (00000) *Boundary-Scan Register*	The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-Scan Shift-Register using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.
BYPASS (11111) *Bypass Register*	Places the 1 bit bypass register between the tdi and tdo pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The BYPASS instruction can be entered by holding tdi at a constant high value and completing an Instruction-Scan cycle.
IDCODE (00001) *Boundary-Scan Register*	Selects the IDCODE register and places it between tdi and tdo, allowing the IDCODE to be serially shifted out of tdo. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
HIGHZ (00101) *Bypass Register*	The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HIGHZ instruction also forces the Bypass Register between tdi and tdo.

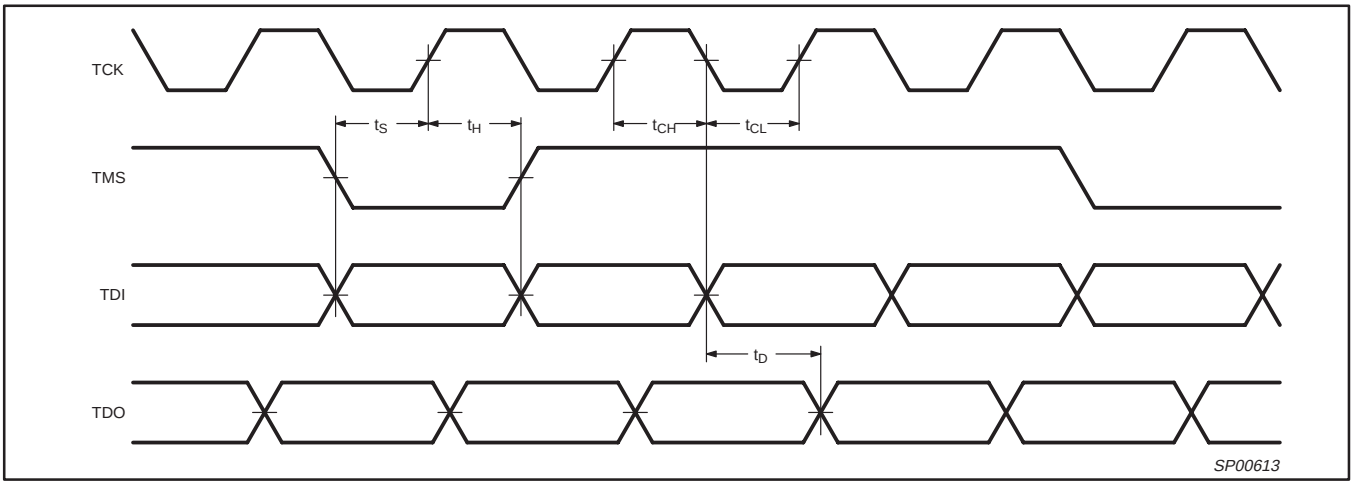


Figure 29. Boundary Scan Timing Diagram

Table 14. Boundary scan timing characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_S	tdi/tms to tck setup time	20	–	ns
t_H	tdi/tms from tck hold time	0	–	ns
t_{CH}	tck high time	50	–	ns
t_{CL}	tck low time	50	–	ns
f_{TCK}	tck frequency	–	10	MHz
t_D	tck to tdo delay	–	35	ns

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	4.6	V
V_{IN}	Input voltage	–1.2	V_{DD}+0.5	V
V_{OUT}	Output voltage	–0.5	V_{DD}+0.5	V
I_{IN}	Input current	–30	30	mA
T_J	Junction temperature range	–40	150	°C
T_{STG}	Storage temperature range	–65	150	°C

NOTE:
1. Stresses above these listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.

OPERATING RANGE

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to 70°C	3.3 ±10% V
Industrial	–40 to 85°C	3.3 ±10% V

DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial temperature range: V_{DD} = 3.0V to 3.6V; 0°C < T_{amb} < 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	Input high voltage	V_{DD} = 3.6V	2.0	V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD} = 3.0V	–0.3	0.8	V
V_{OH}	Output high voltage	V_{DD} = 3.0V; I_{OH} = –8mA	2.4	–	V
V_{OL}	Output low voltage	V_{DD} = 3.0V; I_{OH} = 8mA	–	0.4	V
I_I	Input leakage current	V_{DD} = 3.6V; 0 < V_{IN} < V_{DD}	–10	10	µA
I_{DDSB}	Standby current	T_{amb} = 25°C; no output loads, inputs at V_{DD} or V_{SS}.	–	100	µA
C_{IN}	Input capacitance	T_{amb} = 25°C; V_{DD} = 3.3V; f = 1MHz	–	10	pF
C_{IO}	I/O capacitance	T_{amb} = 25°C; V_{DD} = 3.3V; f = 1MHz	–	10	pF
C_{CLK}	Clock pin capacitance	T_{amb} = 25°C; V_{DD} = 3.3V; f = 1MHz	–	12	pF
R_{DONE}	done pull-up resistor	V_{DD} = 3.0 V; V_{IN} = 0 V	10	30	kΩ
R_{PD}	Unused I/O pull-down resistor	V_{DD} = 3.6V; V_{IN} = V_{DD}	100	400	kΩ

AC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial temperature range: V_{DD} = 3.0V to 3.6V; 0°C < T_{amb} < 70°C

SYMBOL	PARAMETER	MIN	MAX	UNIT
Timing requirements				
t_{CL}	Clock LOW time	2.5		ns
t_{CH}	Clock HIGH time	2.5		ns
t_{SU_PAL}	PAL setup time (Global clock)	4.0		ns
t_{SU_PLA}	PLA setup time (Global clock)	5.5		ns
t_{SU_XOR}	XOR setup time (Global clock)	6.5		ns
t_H	Hold time (Global clock)		0	ns
Output characteristics				
t_{PD_PAL}	Input to output delay through PAL		7.5	ns
t_{PD_PLA}	Input to output delay through PLA		9.0	ns
t_{PD_XOR}	Input to output delay through XOR		10.0	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		4.0	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PLA		5.5	ns
t_{PDF_XOR}	Input (or feedback node) to internal feedback node delay time through XOR		6.5	ns
t_{CF}	Global clock to feedback delay		2.5	ns
t_{CO}	Global clock to out delay		6.0	ns
t_{CS}	Clock skew (variance for switching outputs with common global clock)		1.0	ns
f_{MAX1}	Maximum flip-flop toggle rate $\left(\frac{1}{t_{CL} + t_{CH}}\right)$	200		MHz
f_{MAX2}	Maximum internal frequency $\left(\frac{1}{t_{SU\_PAL} + t_{CF}}\right)$	154		MHz
f_{MAX3}	Maximum external frequency $\left(\frac{1}{t_{SU\_PAL} + t_{CO}}\right)$	100		MHz
t_{BUFF}	Output buffer delay (fast)		3.5	ns
t_{SSR}	Slow slew rate incremental delay		8.0	ns
t_{EA}	Output enable delay		8.0	ns
t_{ER}	Output disable delay[1]		8.0	ns
t_{GTSH}	Global 3-State enable		40.0	ns
t_{GTSR}	Global 3-State disable		40.0	ns
t_{RR}	Input to register reset		10.5	ns
t_{RP}	Input to register preset		10.5	ns
t_{GRR}	Global reset to register reset		40	ns
t_{GZIA}	Global ZIA delay		4.0	ns

NOTE:
1. Output C_L = 5.0pF.

DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial temperature range: V_{DD} = 3.0V to 3.6V; –40°C < T_{amb} < 85°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	Input high voltage	V_{DD} = 3.6V	2.0	V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD} = 3.0V	–0.3	0.8	V
V_{OH}	Output high voltage	V_{DD} = 3.0V; I_{OH} = –8mA	2.4	–	V
V_{OL}	Output low voltage	V_{DD} = 3.0V; I_{OH} = 8mA	–	0.4	V
I_I	Input leakage current	V_{DD} = 3.6V; 0 < V_{IN} < V_{DD}	–10	10	µA
I_{DDSB}	Standby current	T_{amb} = 25°C; no output loads, inputs at V_{DD} or V_{SS}.	–	100	µA
C_{IN}	Input capacitance	T_{amb} = 25°C; V_{DD} = 3.3V; f = 1MHz	–	10	pF
C_{IO}	I/O capacitance	T_{amb} = 25°C; V_{DD} = 3.3V; f = 1MHz	–	10	pF
C_{CLK}	Clock pin capacitance	T_{amb} = 25°C; V_{DD} = 3.3V; f = 1MHz	–	12	pF
R_{DONE}	done pull-up resistor	V_{DD} = 3.0 V; V_{IN} = 0 V	10	30	kΩ
R_{PD}	Unused I/O pull-down resistor	V_{DD} = 3.6V; V_{IN} = V_{DD}	100	400	kΩ

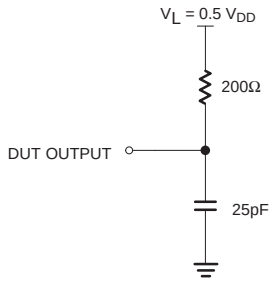
AC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial temperature range: V_{DD} = 3.0V to 3.6V; –40°C < T_{amb} < 85°C

SYMBOL	PARAMETER	MIN	MAX	UNIT
Timing requirements				
t_{CL}	Clock LOW time	2.5		ns
t_{CH}	Clock HIGH time	2.5		ns
t_{SU_PAL}	PAL setup time (Global clock)	4.5		ns
t_{SU_PLA}	PLA setup time (Global clock)	6.0		ns
t_{SU_XOR}	XOR setup time (Global clock)	7.0		ns
t_H	Hold time (Global clock)		0	ns
Output characteristics				
t_{PD_PAL}	Input to output delay through PAL		8.0	ns
t_{PD_PLA}	Input to output delay through PLA		9.5	ns
t_{PD_XOR}	Input to output delay through XOR		10.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		4.0	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PLA		5.5	ns
t_{PDF_XOR}	Input (or feedback node) to internal feedback node delay time through XOR		6.5	ns
t_{CF}	Global clock to feedback delay		2.5	ns
t_{CO}	Global clock to out delay		6.5	ns
t_{CS}	Clock skew (variance for switching outputs with common global clock)		1.0	ns
f_{MAX1}	Maximum flip-flop toggle rate $\left(\frac{1}{t_{CL} + t_{CH}}\right)$	200		MHz
f_{MAX2}	Maximum internal frequency $\left(\frac{1}{t_{SU\_PAL} + t_{CF}}\right)$	143		MHz
f_{MAX3}	Maximum external frequency $\left(\frac{1}{t_{SU\_PAL} + t_{CO}}\right)$	91		MHz
t_{BUFF}	Output buffer delay (fast)		4.0	ns
t_{SSR}	Slow slew rate incremental delay		8.0	ns
t_{EA}	Output enable delay		8.5	ns
t_{ER}	Output disable delay[1]		8.5	ns
t_{GTSH}	Global 3-State enable		40.0	ns
t_{GTSR}	Global 3-State disable		40.0	ns
t_{RR}	Input to register reset		11.0	ns
t_{RP}	Input to register preset		11.0	ns
t_{GRR}	Global reset to register reset		40	ns
t_{GZIA}	Global ZIA delay		4.5	ns

NOTE:
1. Output C_L = 5.0pF.

THEVENIN EQUIVALENT



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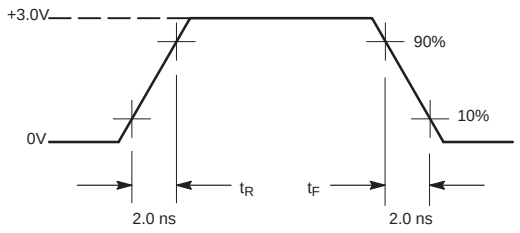
VOLTAGE WAVEFORM



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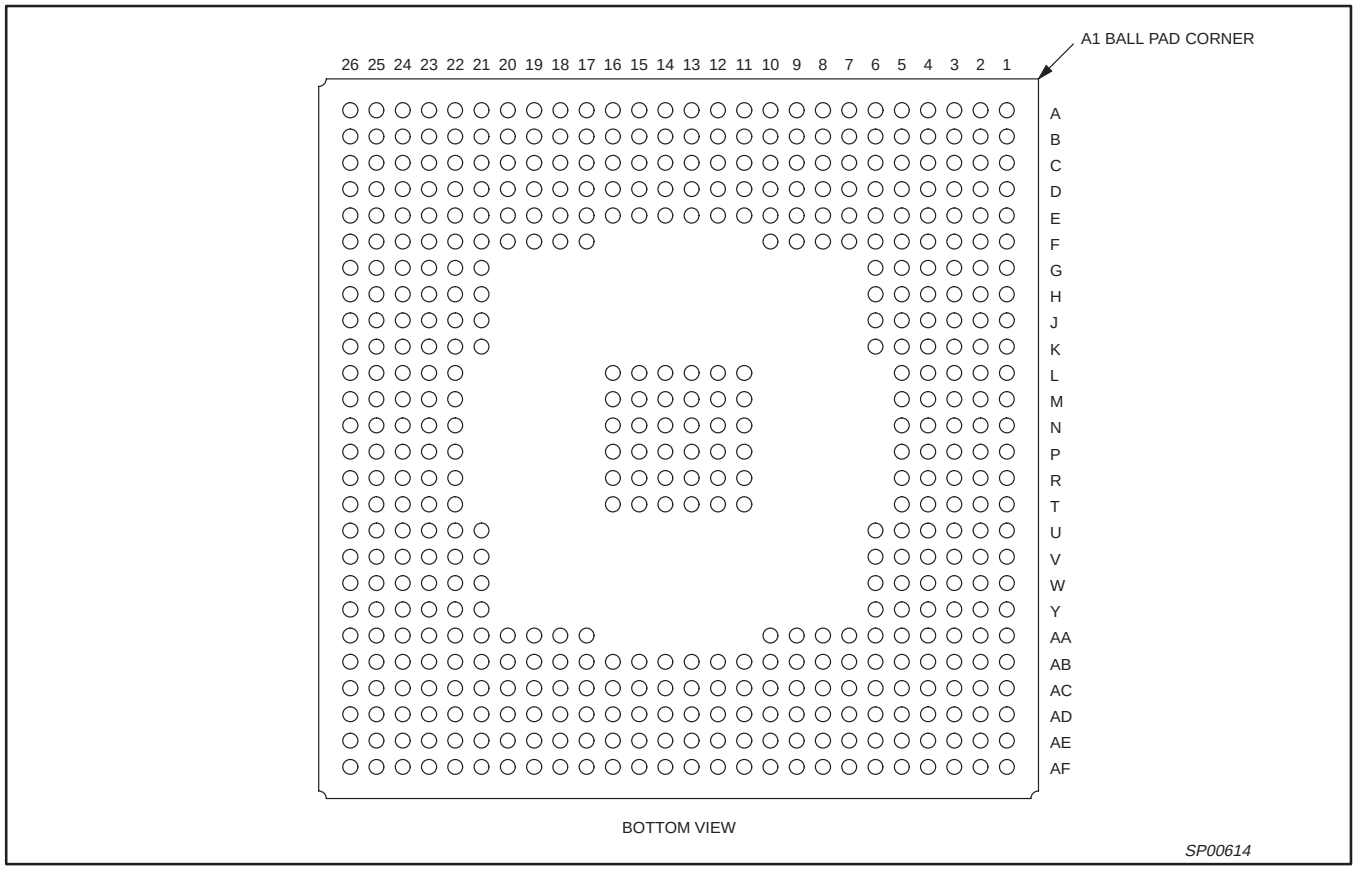
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

PINNING

492-pin Plastic Ball Grid Array (PBGA)



Pin Functions

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell 5.

Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function
A1	F1_0_5	D1	F1_1_12	G1	F0_2_17	M1*	F0_1_8	T1	F11_3_30	AA1*	F11_1_8	AD1	F10_2_18
A2	F1_0_7	D2	F1_1_13	G2	F0_2_16	M2	F0_1_10	T2	F11_2_18	AA2	F10_3_24	AD2	F10_2_19
A3	F1_2_22	D3	F1_1_15	G3	F0_3_30	M3	clk0	T3	F11_2_17	AA3	F10_3_25	AD3	F10_2_20
A4	F1_2_19	D4	F1_0_3	G4	F0_3_29	M4	clk1	T4	F11_2_16	AA4	F10_3_26	AD4	F10_0_1
A5	F1_3_30	D5	F1_2_18	G5	V_{DD}	M5	V_{DD}	T5	V_{DD}	AA5	V_{DD}	AD5*	F10_1_13
A6	F1_3_26	D6	F1_3_29	G6	V_{DD}	M11	GND	T11	GND	AA6	GND	AD6*	F10_1_8
A7	F2_1_10	D7	F1_3_24	G21	V_{DD}	M12	GND	T12	GND	AA7	F10_0_2	AD7*	F9_3_27
A8	F2_1_15	D8	F2_1_11	G22	V_{DD}	M13	GND	T13	GND	AA8	F9_3_30	AD8	F9_2_16
A9	F2_0_3	D9	F2_0_0	G23	F5_1_9	M14	GND	T14	GND	AA9	V_{DD}	AD9	F9_2_20
A10	F2_2_23	D10	F2_0_4	G24	F5_1_11	M15	GND	T15	GND	AA10	V_{DD}	AD10	F9_0_6
A11	F2_2_19	D11	F2_2_20	G25	F5_1_12	M16	GND	T16	GND	AA17	V_{DD}	AD11	F9_0_2
A12	F2_2_17	D12	F2_3_30	G26	F5_1_13	M22	F5_3_25	T22	F6_1_8	AA18	V_{DD}	AD12	F9_1_12
A13	F2_3_28	D13	F2_3_26			M23	F5_3_26	T23	F6_1_12	AA19	F8_1_14	AD13*	F9_1_8
A14	F3_1_9	D14	F2_3_25	H1	F0_2_22	M24	F5_3_27	T24	F6_1_13	AA20	F7_2_17	AD14*	F8_3_27
A15	F3_1_13	D15	F3_1_11	H2	F0_2_21	M25	F5_3_29	T25	F6_1_14	AA21	GND	AD15*	F8_3_31
A16	F3_1_15	D16	F3_0_1	H3	F0_2_19	M26	F5_3_28	T26	F6_1_11	AA22	V_{DD}	AD16	F8_2_21
A17	F3_0_4	D17	F3_0_7	H4	F0_2_18					AA23	F6_3_24	AD17*	F8_0_5
A18	F3_2_23	D18	F3_2_19	H5	F0_0_5	N1	clk3	U1	F11_2_19	AA24	F6_3_25	AD18	F8_0_1
A19	F3_2_18	D19*	F3_3_31	H6	F0_1_15	N2	clk2	U2	F11_2_20	AA25	F6_3_27	AD19	F8_1_12
A20	F3_3_29	D20	F3_3_26	H21	F5_3_31	N3	trstn	U3	F11_2_22	AA26	F6_3_28	AD20*	F8_1_8
A21	F3_3_25	D21	F4_1_9	H22	F5_2_21	N4	tms	U4	F11_2_23			AD21	F7_3_28
A22	F4_1_11	D22	F4_1_14	H23	F5_1_14	N5	gts	U5	V_{DD}	AB1	F10_3_27	AD22	F7_2_16
A23	F4_1_15	D23	F4_0_7	H24	F5_0_0	N11	GND	U6	F11_1_15	AB2	F10_3_28	AD23	F7_2_21
A24	F4_0_3	D24	F4_2_17	H25	F5_0_1	N12	GND	U21	F6_3_31	AB3	F10_3_29	AD24	F7_0_7
A25	F4_0_5	D25	F4_2_16	H26	F5_0_2	N13	GND	U22	V_{DD}	AB4	F10_3_30	AD25	F7_0_0
A26	F4_2_23	D26*	F4_3_31			N14	GND	U23	F6_0_3	AB5	GND	AD26	F7_1_15
				J1	F0_0_4	N15	GND	U24	F6_0_2	AB6	F10_2_22		
B1	F1_0_1	E1	F1_1_8	J2	F0_0_6	N16	GND	U25	F6_0_1	AB7	F10_1_10	AE1	F10_2_21
B2	F1_0_2	E2	F1_1_9	J3	F0_0_7	N22	V_{DD}	U26	F6_0_0	AB8	F9_2_22	AE2	F10_0_6
B3	F1_2_23	E3	F1_1_10	J4	F0_2_23	N23	resetn			AB9	V_{DD}	AE3	F10_0_4
B4	F1_2_20	E4	F1_1_11	J5	F0_2_20	N24	GND	V1	F11_0_7	AB10	V_{DD}	AE4	F10_0_0
B5*	F1_3_31	E5	GND	J6	F0_3_26	N25	F5_3_24	V2	F11_0_6	AB11	F9_0_0	AE5	F10_1_12
B6	F1_3_27	E6	F1_0_6	J21	F5_1_10	N26	GND	V3	F11_0_4	AB12	V_{DD}	AE6	F9_3_24
B7	F2_1_9	E7	F1_3_25	J22	F5_0_4			V4	F11_0_3	AB13	V_{DD}	AE7	F9_3_28
B8	F2_1_13	E8	F2_0_6	J23	F5_0_3	P1	tdi	V5*	F11_0_5	AB14	F8_3_24	AE8	F9_2_17
B9	F2_0_2	E9	V_{DD}	J24	F5_0_5	P2	F11_3_24	V6	F11_1_10	AB15	V_{DD}	AE9	F9_2_21
B10	F2_0_7	E10	F2_2_16	J25	F5_0_6	P3	tdo	V21	F6_3_26	AB16	V_{DD}	AE10*	F9_0_5
B11	F2_2_22	E11	V_{DD}	J26	F5_0_7	P4	tck	V22	F6_2_21	AB17	F8_2_17	AE11*	F9_0_3
B12	F2_2_18	E12	V_{DD}			P5	V_{DD}	V23	F6_2_23	AB18	V_{DD}	AE12	F9_1_14
B13	F2_3_29	E13*	F3_1_8	K1	F0_0_0	P11	GND	V24	F6_0_7	AB19	F8_0_6	AE13	F9_1_10
B14	F3_1_10	E14	V_{DD}	K2	F0_0_1	P12	GND	V25	F6_0_6	AB20	F7_3_26	AE14	F8_3_29
B15	F3_1_14	E15	V_{DD}	K3	F0_0_2	P13	GND	V26	F6_0_4	AB21	F7_0_6	AE15	F8_2_18
B16	F3_0_3	E16	F3_0_0	K4	F0_0_3	P14	GND			AB22	GND	AE16	F8_2_22
B17	F3_0_5	E17	V_{DD}	K5	V_{DD}	P15	GND	W1	F11_0_2	AB23	F7_1_11	AE17	F8_0_7
B18	F3_2_21	E18	V_{DD}	K6	F0_3_31	P16	GND	W2	F11_0_1	AB24	F7_1_10	AE18	F8_0_2
B19	F3_2_17	E19	F3_2_22	K21	F5_1_15	P22	done	W3	F11_0_0	AB25	F7_1_9	AE19*	F8_1_13
B20	F3_3_28	E20	F4_1_10	K22	V_{DD}	P23	prgmn	W4	F11_1_14	AB26	F7_1_8	AE20	F8_1_9
B21	F3_3_24	E21	F4_2_22	K23	F5_2_23	P24	cclk	W5	F11_2_21			AE21*	F7_3_27
B22	F4_1_12	E22	GND	K24	F5_2_22	P25	clk6	W6*	F11_3_31	AC1*	F10_3_31	AE22*	F7_3_31
B23	F4_0_0	E23	F4_3_30	K25	F5_2_20	P26	clk7	W21	F6_1_15	AC2	F10_2_16	AE23	F7_2_20
B24	F4_0_4	E24	F4_3_29	K26	F5_2_19			W22	F6_0_5	AC3	F10_2_17	AE24*	F7_2_23
B25	F4_0_6	E25	F4_3_28			R1	F11_3_28	W23	F6_2_18	AC4	F10_0_7	AE25	F7_0_2
B26	F4_2_21	E26	F4_3_27	L1	F0_1_11	R2	F11_3_29	W24*	F6_2_19	AC5	F10_1_14	AE26	F7_0_1
				L2	F0_1_14	R3*	F11_3_27	W25	F6_2_20	AC6	F10_1_9		
C1	F1_1_14	F1	F0_3_28	L3*	F0_1_13	R4	F11_3_26	W26	F6_2_22	AC7	F9_3_26	AF1	F10_2_23
C2	F1_0_0	F2	F0_3_27	L4	F0_1_12	R5	F11_3_25			AC8*	F9_3_31	AF2*	F10_0_5
C3	F1_0_4	F3	F0_3_25	L5	F0_1_9	R11	GND	Y1*	F11_1_13	AC9*	F9_2_19	AF3*	F10_0_3
C4	F1_2_21	F4	F0_3_24	L11	GND	R12	GND	Y2	F11_1_12	AC10	F9_0_7	AF4	F10_1_15
C5	F1_2_16	F5	V_{DD}	L12	GND	R13	GND	Y3	F11_1_11	AC11	F9_0_1	AF5	F10_1_11
C6	F1_3_28	F6	GND	L13	GND	R14	GND	Y4	F11_1_9	AC12	F9_1_11	AF6	F9_3_25
C7*	F2_1_8	F7	F1_2_17	L14	GND	R15	GND	Y5	V_{DD}	AC13	F8_3_25	AF7	F9_3_29
C8	F2_1_12	F8	F2_1_14	L15	GND	R16	GND	Y6	V_{DD}	AC14	F8_3_26	AF8	F9_2_18
C9	F2_0_1	F9	V_{DD}	L16	GND	R22	V_{DD}	Y21	V_{DD}	AC15	F8_3_30	AF9*	F9_2_23
C10	F2_0_5	F10	V_{DD}	L22	V_{DD}	R23	clk5	Y22	V_{DD}	AC16	F8_2_20	AF10	F9_0_4
C11	F2_2_21	F17	V_{DD}	L23	F5_2_16	R24	clk4	Y23	F6_3_29	AC17	F8_0_4	AF11	F9_1_15
C12*	F2_3_31	F18	V_{DD}	L24	F5_2_17	R25	F6_1_10	Y24	F6_3_30	AC18	F8_0_0	AF12*	F9_1_13
C13	F2_3_27	F19	F3_3_30	L25	F5_2_18	R26	F6_1_9	Y25	F6_2_16	AC19	F8_1_11	AF13	F9_1_9
C14	F2_3_24	F20	F4_0_2	L26	F5_3_30			Y26	F6_2_17	AC20	F7_3_24	AF14	F8_3_28
C15	F3_1_12	F21	GND							AC21	F7_3_29	AF15	F8_2_16
C16	F3_0_2	F22	V_{DD}							AC22	F7_2_18	AF16*	F8_2_19
C17	F3_0_6	F23	F4_3_26							AC23	F7_0_3	AF17*	F8_2_23
C18	F3_2_20	F24	F4_3_25							AC24	F7_1_14	AF18*	F8_0_3
C19	F3_2_16	F25	F4_3_24							AC25	F7_1_13	AF19	F8_1_15
C20	F3_3_27	F26	F5_1_8							AC26	F7_1_12	AF20	F8_1_10
C21*	F4_1_8											AF21	F7_3_25
C22	F4_1_13											AF22	F7_3_30
C23	F4_0_1											AF23*	F7_2_19
C24	F4_2_20											AF24	F7_2_22
C25	F4_2_19											AF25	F7_0_5
C26	F4_2_18											AF26	F7_0_4

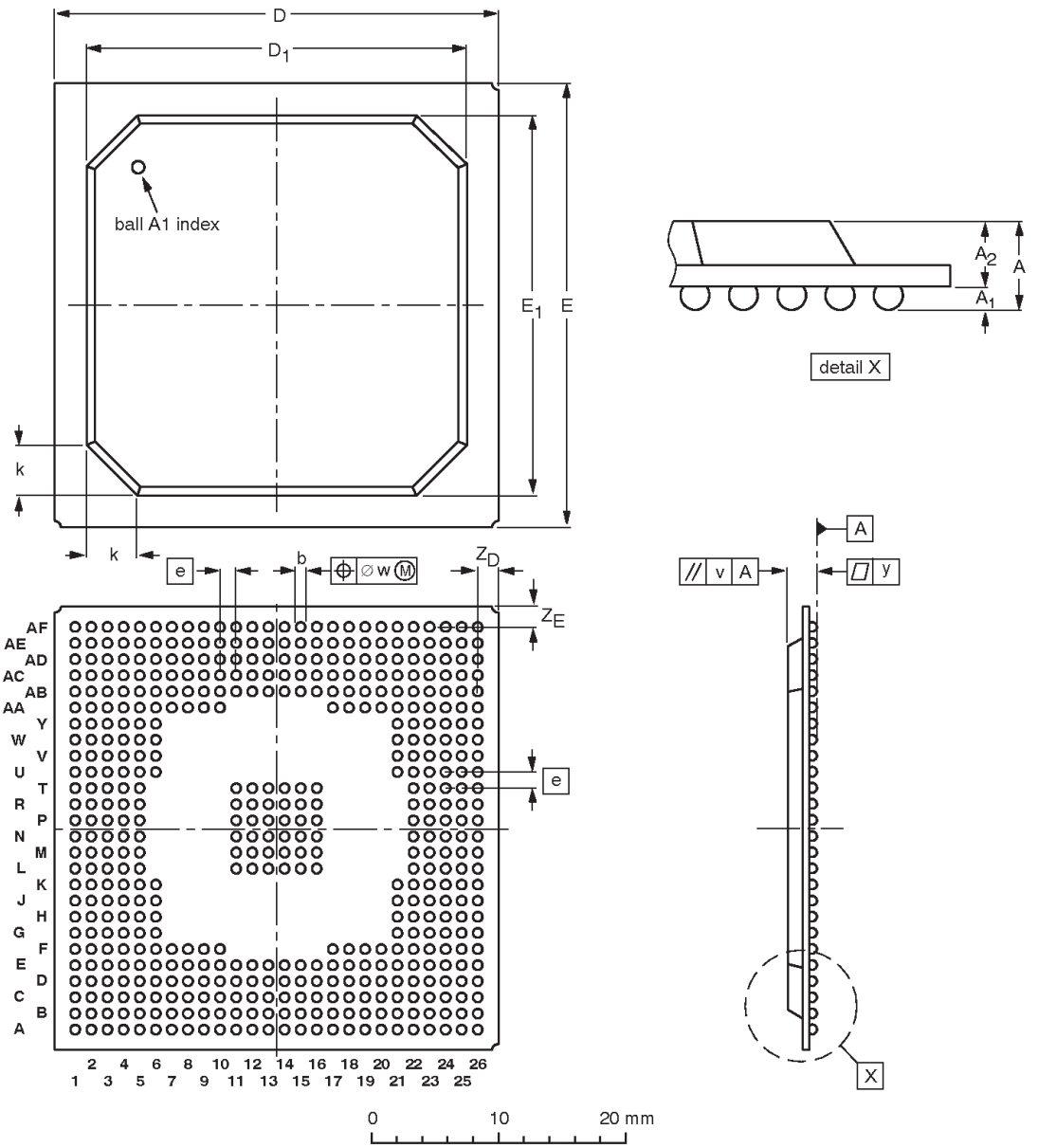
* Multi-function pin used during configuration. See Table 15 for information.

Table 15. Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{DD}	E9, E11, E12, E14, E15, E17, E18, F5, F9, F10, F17, F18, F22, G5, G6, G21, G22, K5, K22, L22, M5, N22, P5, R22, T5, U5, U22, Y5, Y6, Y21, Y22, AA5, AA9, AA10, AA17, AA18, AA22, AB9, AB10, AB12, AB13, AB15, AB16, AB18	–	Positive power supply.
GND	E5, E22, F6, F21, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, N24, N26, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, AA6, AA21, AB5, AB22	–	Ground supply.
resetn	N23	I	During configuration, resetn forces the start of initialization (see Figure 8). After configuration, resetn is a direct input which can be used to asynchronously reset all the flip-flops. If the global reset is not being used, this pin should be pulled high. If the rise time of the prgmn signal is greater than 1 microsecond, this signal must be held low until prgmn is high.
cclk	P24	I/O	In the master modes, cclk is an output which strobes configuration data in. In the slave or synchronous peripheral mode, cclk is an input synchronous with the data on din or D[7:0]. After configuration, this pin should be pulled low.
done	P22	I/O	done is a bi-directional signal with a weak pull-up resistor attached. As an output, done pulling high indicates configuration is complete. As an input, a low level on done will delay the enabling of user I/O. If only one device is used, this pin can be left floating. If multiple devices are daisy chained, an external pull-up should be used (see Figure 27).
prgmn	P23	I	prgmn is an active-low input that forces the restart of configuration and initialization (see Figure 8) and resets the boundary-scan circuitry. After configuration, the pin should be pulled high. This signal must have a rise time less than 1 microsecond. If the rise time of this signal is greater than 1 microsecond, resetn must be held low until prgmn is high.
spmi	E13	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
mpmi	C12	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
din	AC1	I	During slave serial or master serial configuration modes, din accepts serial configuration data synchronous with cclk. During parallel configuration modes, din is the D[0] input. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
M2	AE22	I	M2/M1/M0 are used to select the configuration mode as defined in Table 3. After configuration, the pins are user-programmable I/O, and no external termination is required. See the section on terminations for more information.
M0	AE24		
M1	AF23		

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M3	AD20	I	M3 should be pulled high during configuration for all configuration modes. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
tdi tdo tck tms trstn	P1 P3 P4 N4 N3	I O I I I	Test Data In, Test Data Out, Test Clock, Test Mode Select, Test Reset are dedicated pins for boundary-scan through the JTAG port. If JTAG is not being used, tdi, tck, tms, and trstn should be terminated with a weak pull-up resistor. tdo can be left unterminated. See section on terminations for more information.
hdc	C21	O	High During Configuration (hdc) is output high when the PZ3960 is in the configuration state. hdc is used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
ldcn	D19	O	Low During Configuration (ldcn) is output low when the PZ3960 is in the configuration state. ldcn is used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
crcerrn	D26	I/O	crcerrn goes low when the PZ3960 detects a CRC error or an invalid peramble during configuration. The PZ3960 that detected the error will go into the initialization state and will not resume configuration until prgmn and resetn are both high. Once configuration has resumed crcerrn will go high. During configuration, an internal pull-up is enabled. If only one device is used, this pin can be left floating. If multiple devices are daisy chained, an external pull-up should be used (see Figure 27). After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
gts	N5	I	Global 3-State is an active-high dedicated input used to 3-state the I/Os and activate the internal pull-down resistors. If this feature is not used, the pin should be pulled low.
cs0n cs1	B5 C7	I	cs0n/cs1 are used in the peripheral configuration mode. The PZ3960 is selected when cs0n is low and cs1 is high. After configuration, these pins are user-programmable I/O. cs0N requires no external termination is required. See the section on terminations for more information. If cs1 is not used as an I/O after configuration in synchronous peripheral mode, the tristate property should be used to disable the internal pull-down resistor. See the section on synchronous peripheral configuration for more information.
A[19:0]	AF2, AF3, AD5, AD6, AD7, AC8, AC9, AF9, AE10, AE11, AF12, AD13, AD14, AD15, AF16, AF17, AD17, AF18, AE19, AE21	O	In the master parallel configuration mode, A[19:0] address the configuration EEPROM. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
D[7:0]	L3, M1, R3, W6, V5, Y1, AA1, AC1	I	During master parallel, peripheral, and slave parallel configuration modes, D[7:0] receive configuration data. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
dout	W24	O	During configuration, dout is the serial data out that is used to drive the din of daisy-chained slave devices. Data on dout changes on the falling edge of cclk. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.

BGA492: plastic ball grid array package; 492 balls; body 35 x 35 x 1.75 mm **SOT514-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	D_1	E	E_1	e	k	v	w	y	Z_D	Z_E
mm	2.54	0.7 0.5	1.84 1.62	0.9 0.6	35.1 34.9	30.7 30.0	35.1 34.9	30.7 30.0	1.27	4.1 3.9	0.35	0.3	0.15	1.93 1.28	1.93 1.28

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT514-1						98-04-08

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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