# TrenchMOS™ transistor Logic level FET

# BUK9830-30

## GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology, the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

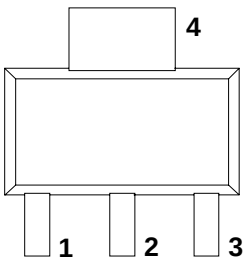
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 30 | V |
| $I_D$ | Drain current (DC) $T_{sp}$ = 25 ˚C | 12.8 | A |
| | Drain current (DC) $T_{amb}$ = 25 ˚C | 5.9 | A |
| $P_{tot}$ | Total power dissipation | 8.3 | W |
| $T_j$ | Junction temperature | 150 | ˚C |
| $R_{DS(ON)}$ | Drain-source on-state resistance $V_{GS}$ = 5 V | 30 | mΩ |

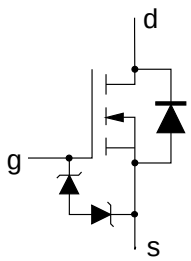
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | gate |
| 2 | drain |
| 3 | source |
| 4 | drain (tab) |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | - | - | 30 | V |
| $V_{DGR}$ | Drain-gate voltage | $R_{GS}$ = 20 kΩ | - | 30 | V |
| $\pm V_{GS}$ | Gate-source voltage | - | - | 10 | V |
| $I_D$ | Drain current (DC) | $T_{sp}$ = 25 ˚C | - | 12.8 | A |
| | | $T_{amb}$ = 25 ˚C | - | 5.9 | A |
| $I_D$ | Drain current (DC) | $T_{sp}$ = 100 ˚C | - | 9 | A |
| | | $T_{amb}$ = 100 ˚C | - | 4.1 | A |
| $I_{DM}$ | Drain current (pulse peak value) | $T_{sp}$ = 25 ˚C | - | 51 | A |
| | | $T_{amb}$ = 25 ˚C | - | 23.6 | A |
| $P_{tot}$ | Total power dissipation | $T_{sp}$ = 25 ˚C | - | 8.3 | W |
| | | $T_{amb}$ = 25 ˚C | - | 1.8 | W |
| $T_{stg}$, $T_j$ | Storage & operating temperature | - | - 55 | 150 | ˚C |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | Thermal resistance junction to solder point | Mounted on any PCB | 12 | 15 | K/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction to ambient | Mounted on PCB of Fig.19 | - | 70 | K/W |

## ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_C$ | Electrostatic discharge capacitor voltage, all pins | Human body model (100 pF, 1.5 kΩ) | - | 2 | kV |

## STATIC CHARACTERISTICS

$T_j$= 25˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 0.25 mA; | 30 | - | - | V |
| | | $T_j$ = -55˚C | 27 | - | - | V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$; $I_D$ = 1 mA | 1 | 1.5 | 2 | V |
| | | $T_j$ = 150˚C | 0.5 | - | - | V |
| | | $T_j$ = -55˚C | - | - | 2.3 | |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; | - | 0.05 | 10 | µA |
| | | $T_j$ = 150˚C | - | - | 500 | µA |
| $I_{GSS}$ | Gate source leakage current | $V_{GS}$ = ±5 V; $V_{DS}$ = 0 V | - | 0.02 | 1 | µA |
| | | $T_j$ = 150˚C | - | | 10 | µA |
| $\pm V_{(BR)GSS}$ | Gate-source breakdown voltage | $I_G$ = ±1 mA; | 10 | - | - | V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 3.2 A | - | 24 | 30 | mΩ |
| | | $T_j$ = 150˚C | - | - | 51 | mΩ |

## DYNAMIC CHARACTERISTICS

$T_{sp}$ = 25˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $g_{fs}$ | Forward transconductance | $V_{DS}$ = 25 V; $I_D$ = 5.9 A | 7 | 14 | - | S |
| $Q_{g(tot)}$ | Total gate charge | $I_D$ = 5.9 A; $V_{DD}$ = 24 V; $V_{GS}$ = 5 V | - | 24 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 3 | - | nC |
| $Q_{gd}$ | Gate-drain (Miller) charge | | - | 11 | - | nC |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz | - | 1050 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 270 | - | pF |
| $C_{rss}$ | Feedback capacitance | | - | 140 | - | pF |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD}$ = 15 V; $I_D$ = 5.9 A; | - | 30 | 45 | ns |
| $t_r$ | Turn-on rise time | $V_{GS}$ = 5 V; $R_G$ = 5 Ω | - | 80 | 130 | ns |
| $t_{d\ off}$ | Turn-off delay time | Resistive load | - | 95 | 135 | ns |
| $t_f$ | Turn-off fall time | | - | 40 | 55 | ns |
| $L_d$ | Internal drain inductance | Measured from contact screw on tab to centre of die | - | 3.5 | - | nH |
| $L_d$ | Internal drain inductance | Measured from drain lead 6 mm from package to centre of die | - | 4.5 | - | nH |
| $L_s$ | Internal source inductance | Measured from source lead 6 mm from package to source bond pad | - | 7.5 | - | nH |

## REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j$ = 25˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{DR}$ | Continuous reverse drain current | | - | - | 40 | A |
| $I_{DRM}$ | Pulsed reverse drain current | | - | - | 160 | A |
| $V_{SD}$ | Diode forward voltage | $I_F$ = 3.2 A; $V_{GS}$ = 0 V | - | 0.75 | 1.2 | V |
| | | $I_F$ = 5.9 A; $V_{GS}$ = 0 V | - | 0.85 | - | |
| $t_{rr}$ | Reverse recovery time | $I_F$ = 5.9 A; -d$I_F$/dt = 100 A/µs; | - | 100 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | $V_{GS}$ = -10 V; $V_R$ = 25 V | - | 0.4 | - | µC |

## AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $W_{DSS}$ | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D$ = 5.9 A; $V_{DD} \leq$ 25 V; $V_{GS}$ = 10 V; $R_{GS}$ = 50 Ω; $T_{sp}$ = 25 ˚C | - | - | 60 | mJ |

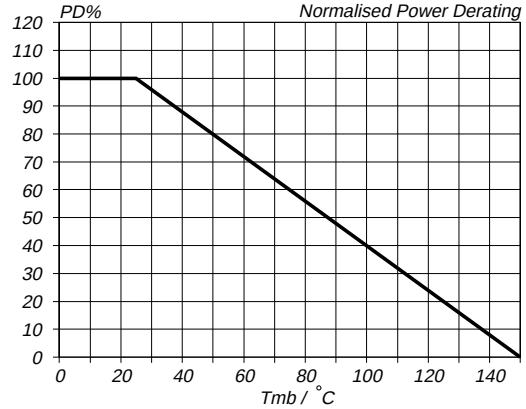



*Fig.1. Normalised power dissipation.*
*PD% = 100·$P_D$/$P_{D\ 25\ ˚C}$ = f($T_{mb}$)*

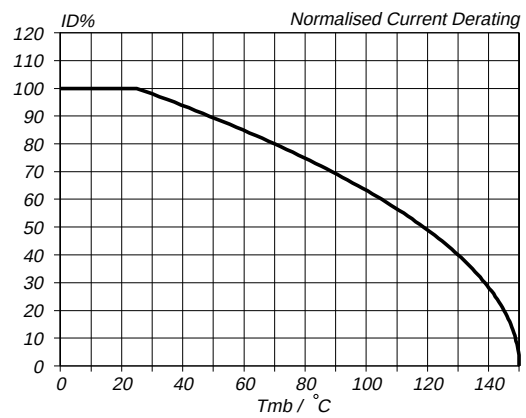



*Fig.2. Normalised continuous drain current.*
*ID% = 100·$I_D$/$I_{D\ 25\ ˚C}$ = f($T_{mb}$); conditions: $V_{GS}$ ≥ 5 V*

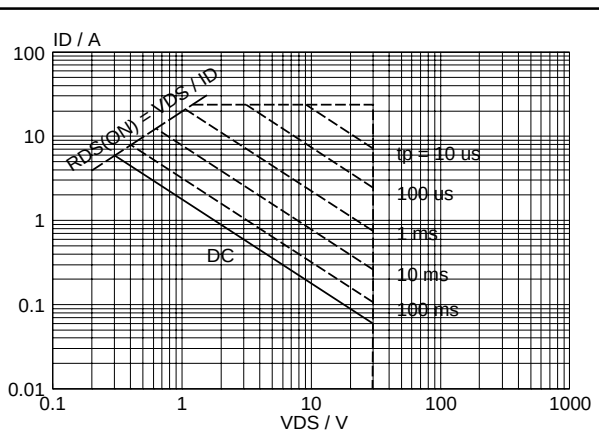



*Fig.3. Safe operating area. $T_{mb}$ = 25 ˚C*
*$I_D$ & $I_{DM}$ = f($V_{DS}$); $I_{DM}$ single pulse; parameter $t_p$*

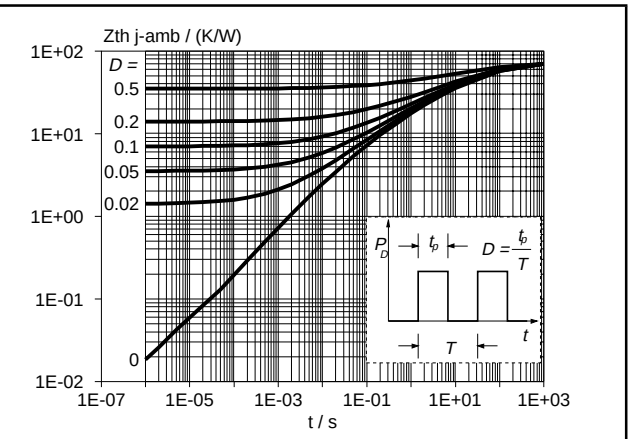



*Fig.4. Transient thermal impedance.*
*$Z_{th\ j\text{-}mb}$ = f(t); parameter D = $t_p$/T*

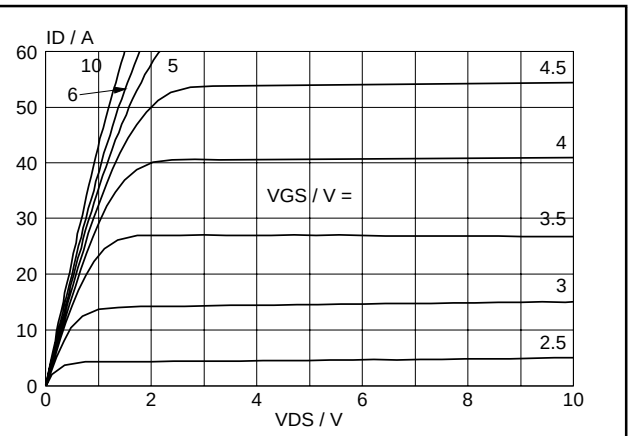



*Fig.5. Typical output characteristics, $T_j$ = 25 ˚C.*
*$I_D$ = f($V_{DS}$); parameter $V_{GS}$*

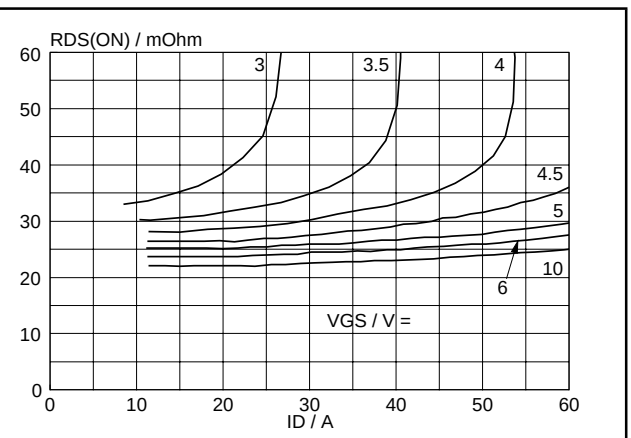



*Fig.6. Typical on-state resistance, $T_j$ = 25 ˚C.*
*$R_{DS(ON)}$ = f($I_D$); parameter $V_{GS}$*

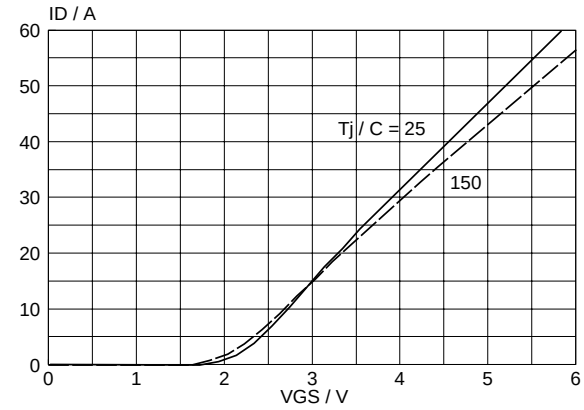



*Fig.7. Typical transfer characteristics.*
*$I_D = f(V_{GS})$ ; conditions: $V_{DS}$ = 25 V; parameter $T_j$*

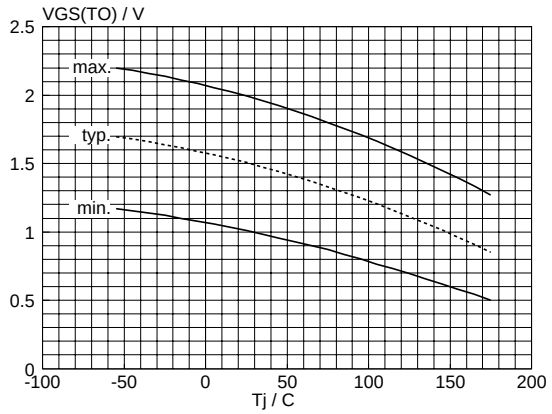



*Fig.10. Gate threshold voltage.*
*$V_{GS(TO)} = f(T_j)$; conditions: $I_D$ = 1 mA; $V_{DS} = V_{GS}$*

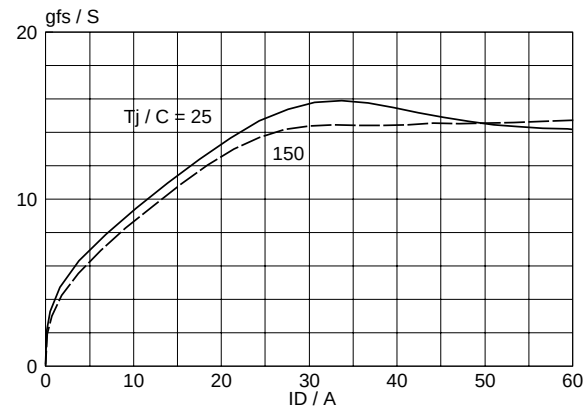



*Fig.8. Typical transconductance, $T_j$ = 25 ˚C.*
*$g_{fs} = f(I_D)$; conditions: $V_{DS}$ = 25 V*

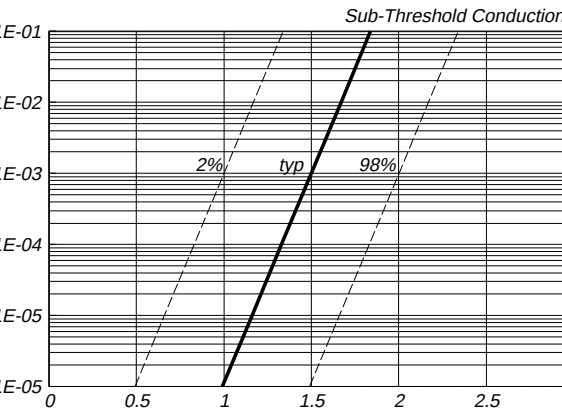



*Fig.11. Sub-threshold drain current.*
*$I_D = f(V_{GS})$; conditions: $T_j$ = 25 ˚C; $V_{DS} = V_{GS}$*

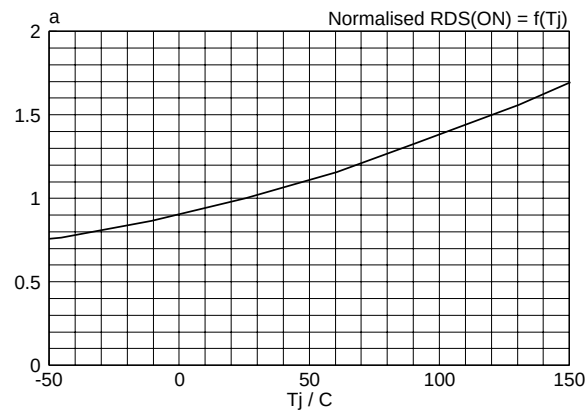



*Fig.9. Normalised drain-source on-state resistance.*
*$a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; $I_D$ = 3.2 A; $V_{GS}$ = 5 V*

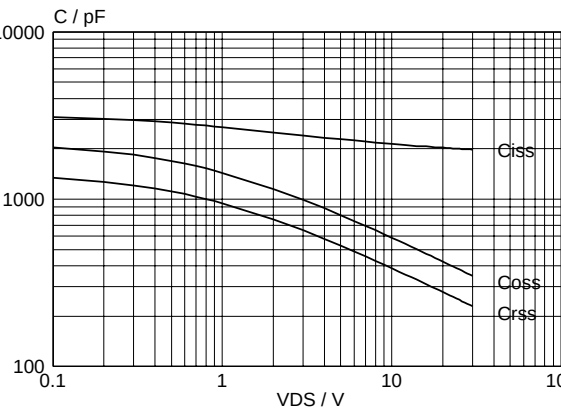



*Fig.12. Typical capacitances, $C_{iss}$, $C_{oss}$, $C_{rss}$.*
*$C = f(V_{DS})$; conditions: $V_{GS}$ = 0 V; f = 1 MHz*

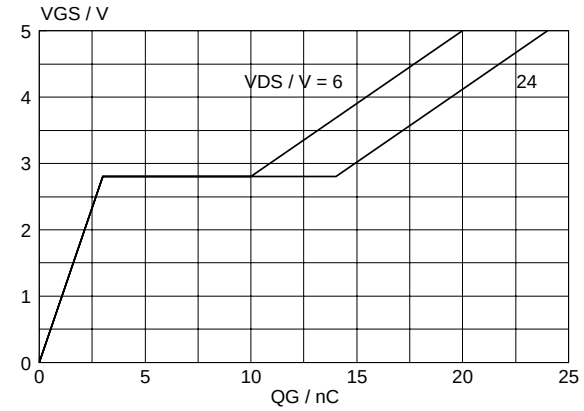



*Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 5.9$ A; parameter $V_{DS}$*

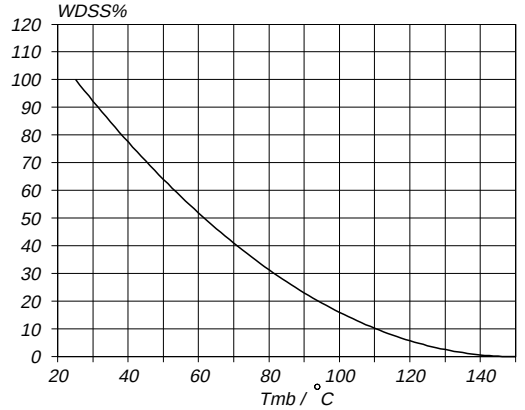



*Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 5.9$ A*

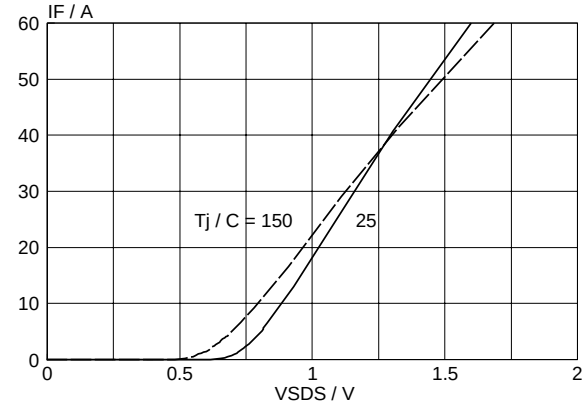



*Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter $T_j$*

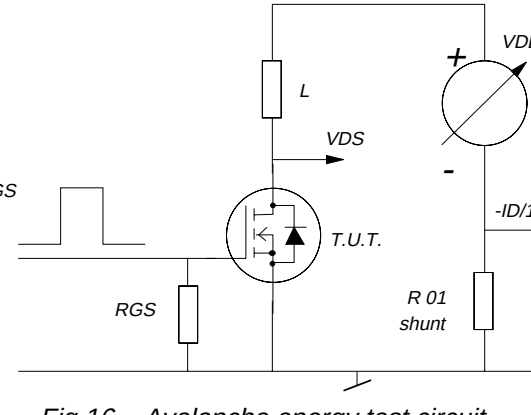



*Fig.16. Avalanche energy test circuit.*

$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

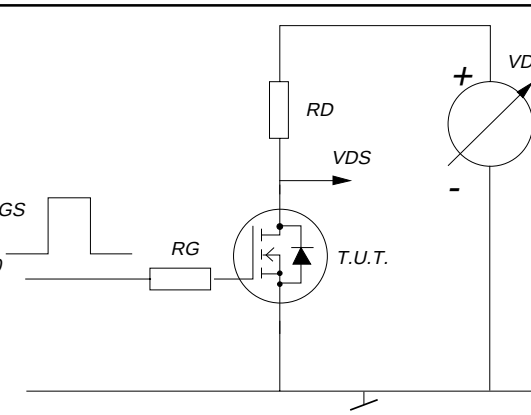



*Fig.17. Switching test circuit.*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

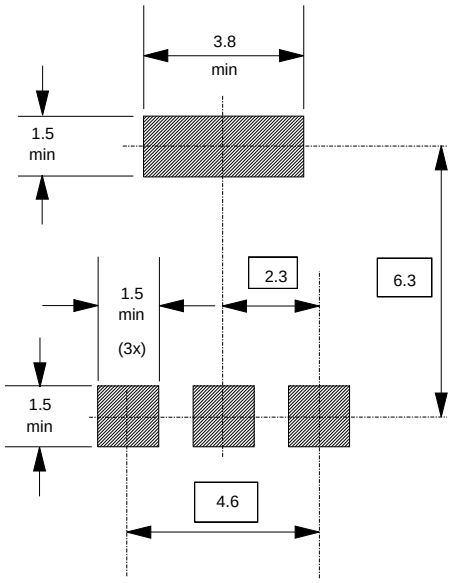



*Fig.18. soldering pattern for surface mounting SOT223.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

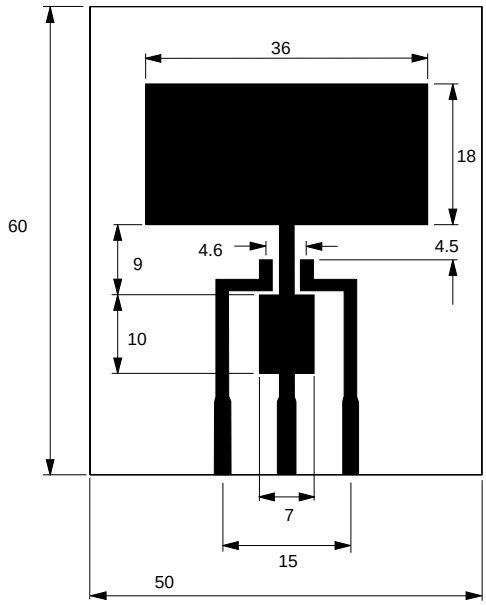



*Fig.19. PCB for thermal resistance and power rating for SOT223.*
*PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 0.11 g*

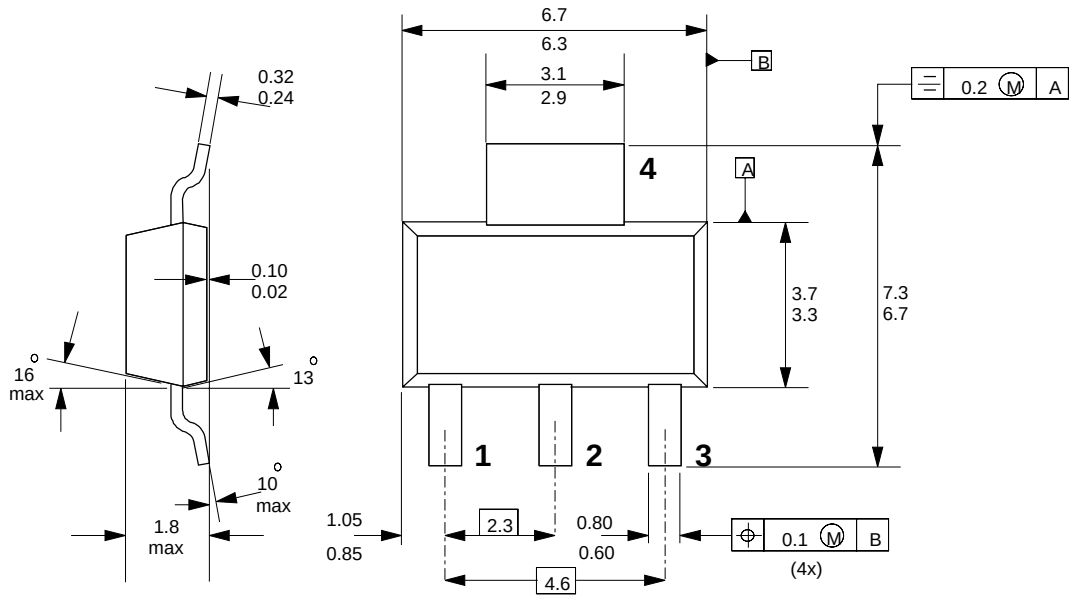



*Fig.20. SOT223 surface mounting package.*

**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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## LIFE SUPPORT APPLICATIONS

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