DATA SHEET

BST72A
N-channel vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

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Philips Semiconductors

PHILIPS

N-channel vertical D-MOS transistor BST72A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

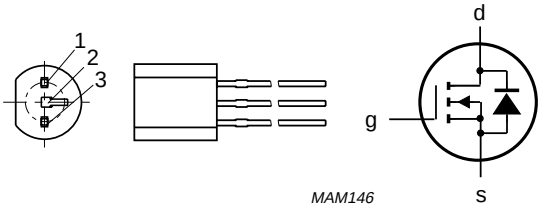
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance				
I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	typ.	150	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor BST72A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80	V
Drain-source leakage current				
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance (see Fig.4)				
I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
I_D = 200 mA; V_{DS} = 5 V	$\|Y_{fs}\|$	typ.	150	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	15	pF
		max.	30	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13	pF
		max.	20	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3	pF
		max.	6	pF
Switching times (see Figs 2 and 3)				
I_D = 200 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	4	ns
		max.	10	ns

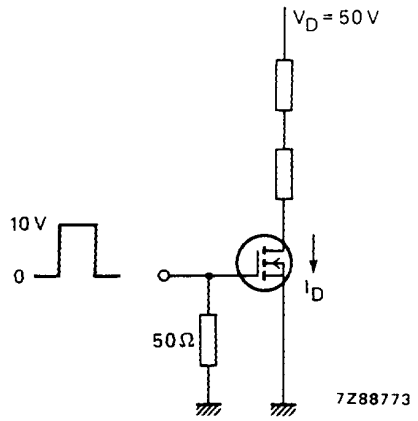


Fig.2 Switching times test circuit.

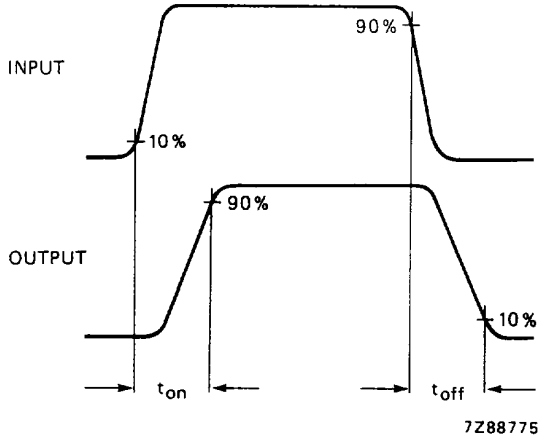


Fig.3 Input and output waveforms.

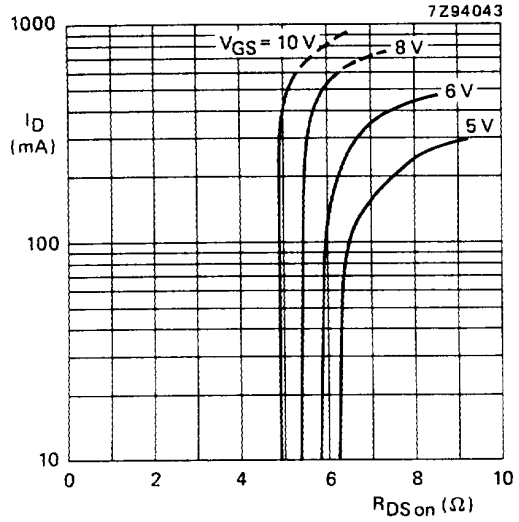


Fig.4 T_j = 25 °C; typical values.

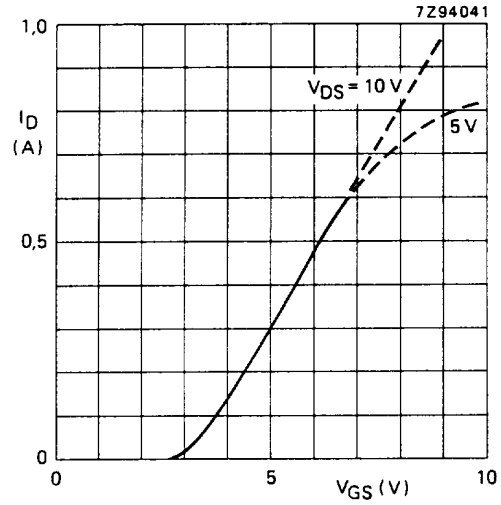


Fig.5 T_j = 25 °C; typical values.

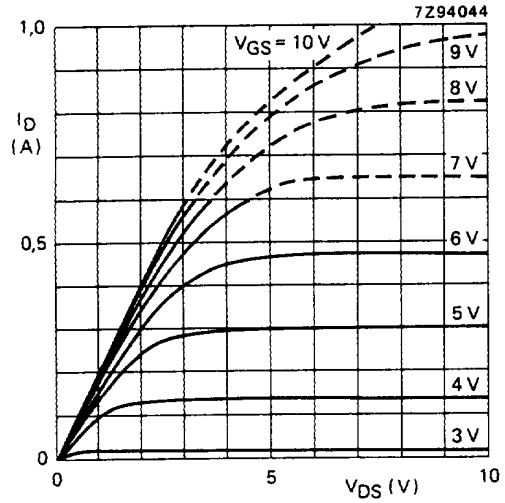


Fig.6 T_j = 25 °C; typical values.

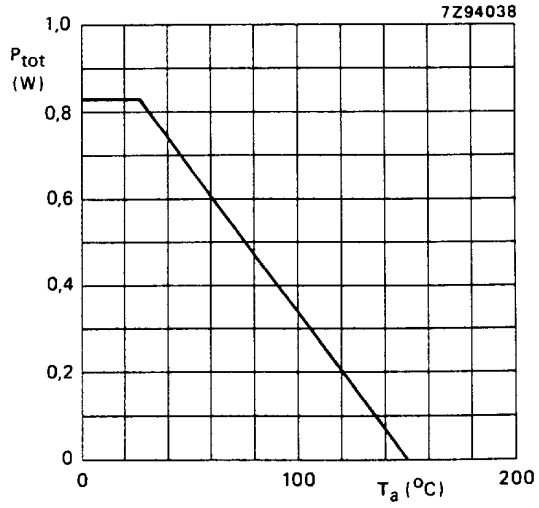


Fig.7 Power derating curve.

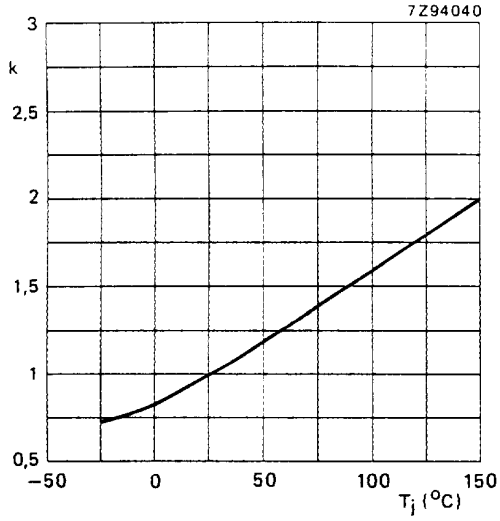


Fig.8

$$k = \frac{R_{DS\ on} \text{ at } T_j}{R_{DS\ on} \text{ at } 25\ °C};$$

typ. values at 150 mA/5 V.

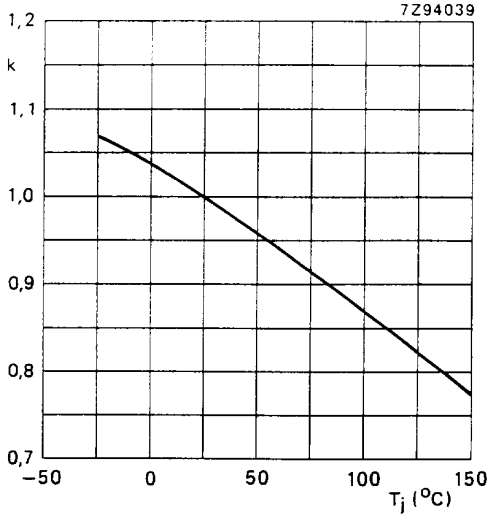


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

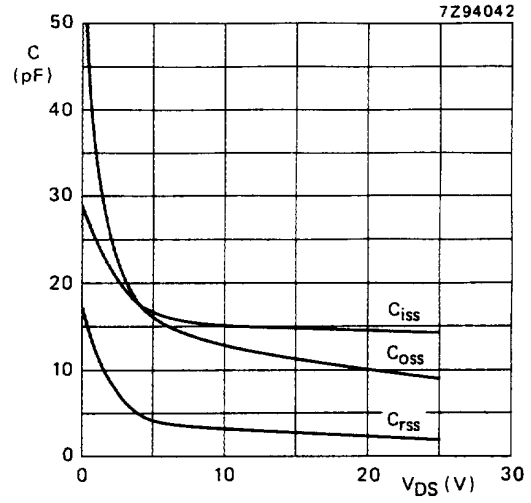
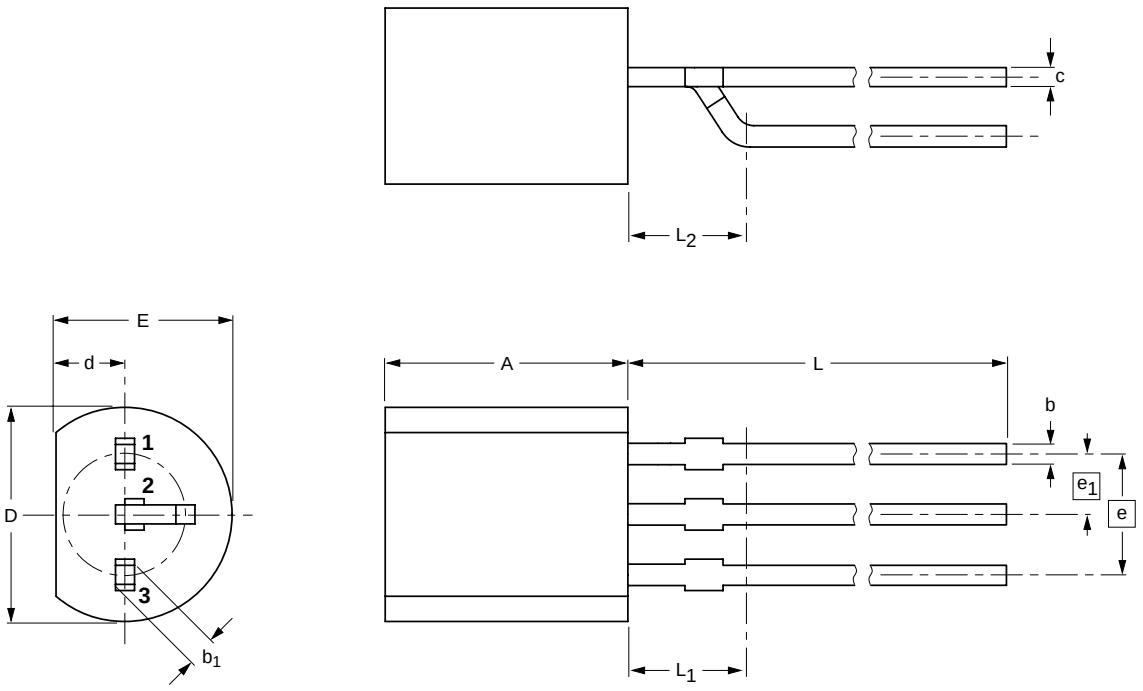


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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