HB54A2569F1-10B

256 MB Registered DDR SDRAM DIMM
32-Mword × 72-bit, 1-Bank Module
(9 pcs of 32 M × 8 Components)

HITACHI

Preliminary
Rev. 0.0
Jan. 25, 2000

Description

The HB54A2569F1 is a 32M × 72 × 1-bank Double Data Rate (DDR) SDRAM Module, mounted 9 pieces of 256-Mbit DDR SDRAM (HM5425801BTT) sealed in TSOP package, 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). Read and write operations are performed at the cross points of the CK and the CK. This high speed data transfer is realized by the 2-bit prefetch piplined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 184-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 184-pin socket type package (dual lead out)
  - Outline: 133.35 mm (Length) × 43.18 mm (Height) × 4.00 mm (Thickness)
  - Lead pitch: 1.27 mm
- 2.5 V power supply (V_{CC}/V_{CCQ})
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 100MHz (max)
- Data inputs, outputs and DM are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2/4/8
  - Burst read stop capability

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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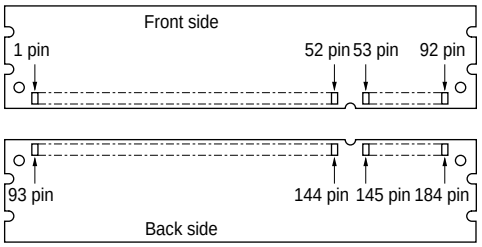
- Programmable burst sequence
  - — Sequential
  - — Interleave
- Start addressing capability
  - — Even and Odd
- CAS latency: 3
- 8192 refresh cycles: 7.8 μs (8192 row/64 ms)
- 2variations of refresh
  - — Auto refresh
  - — Self refresh

Ordering Information

Type No.	Frequency	/CAS latency	Package	Contact pad
HB54A2569F1-10B	100 MHz	3	184-pin dual lead out socket type	Gold

Pin Arrangement



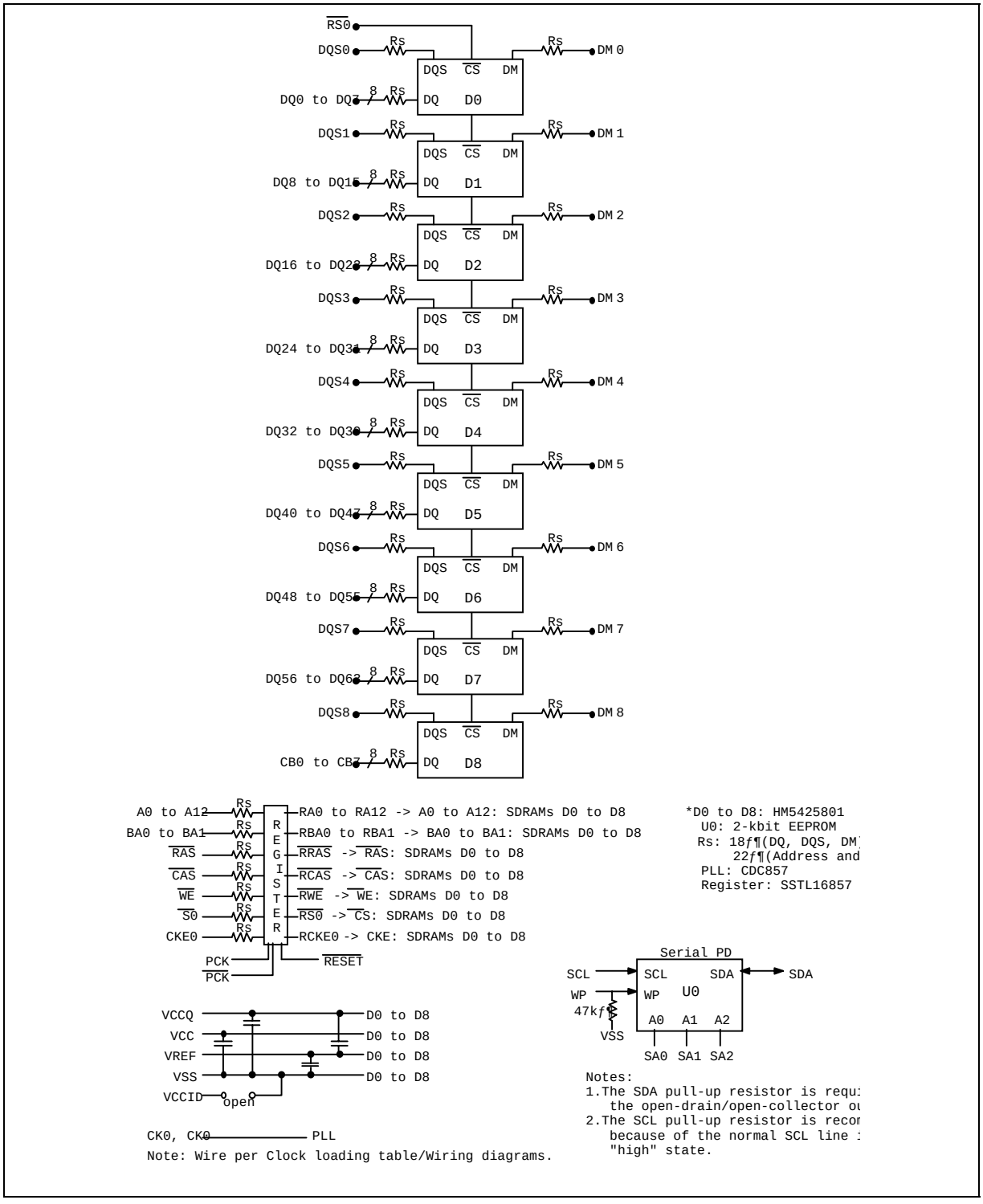
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DM8
3	V_{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	CB6
5	DQS0	51	CB3	97	DM0	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	/RESET	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DM4
12	DQ8	58	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DM1	153	DQ44
16	NC	62	V_{CCQ}	108	V_{CC}	154	/RAS
17	NC	63	/WE	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	/CAS	111	NC	157	/S0
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V_{CCQ}	76	NC	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DM6
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	V_{CCQ}
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	WP	136	V_{CCQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	/CK0	184	V_{CCSPD}

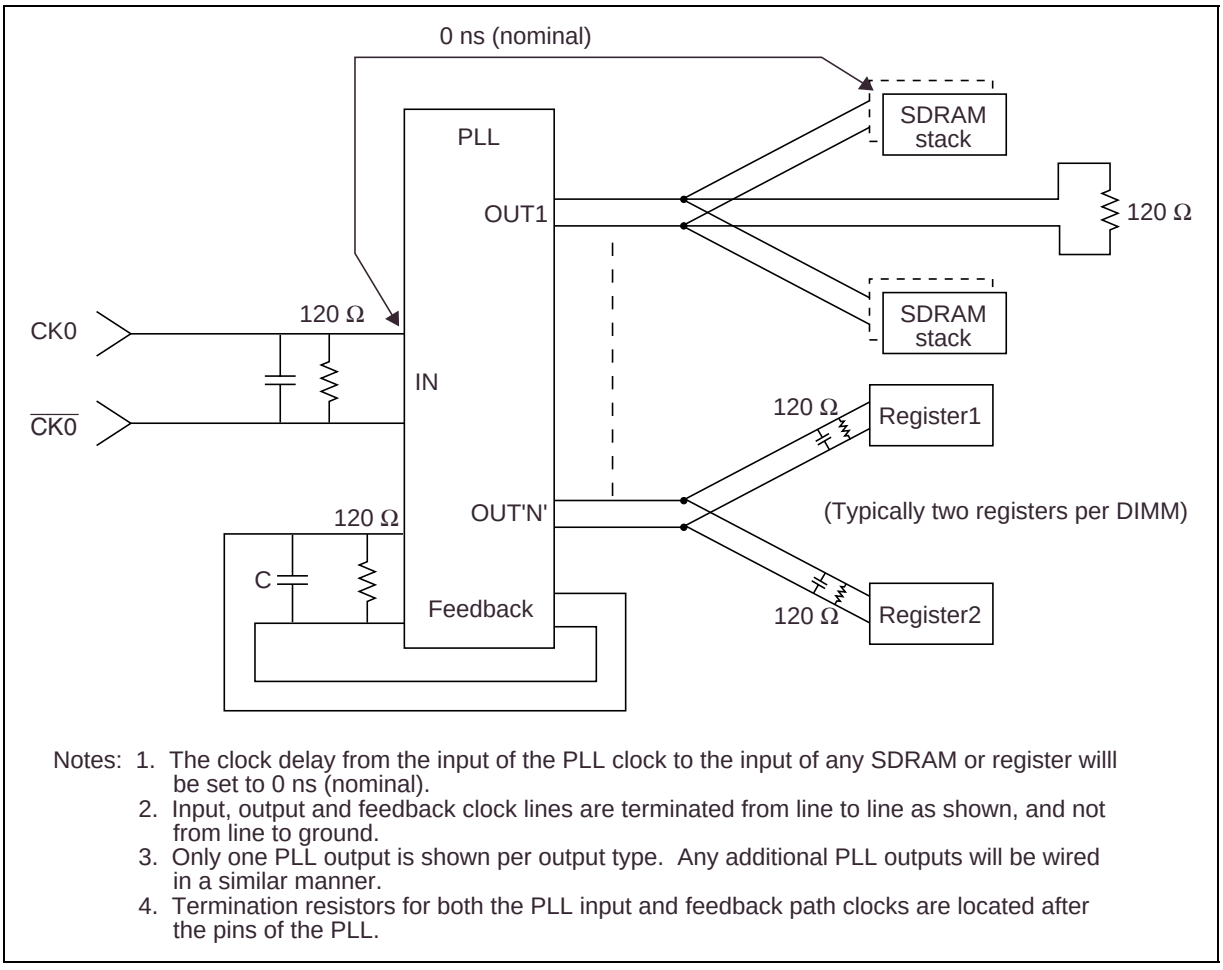
Pin Description

Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/S0	Chip select
CKE0	Clock enable
CK0	Clock input
CK0	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
WP	Write protect for serial PD
SA0 to SA2	Serial address input
V_{CC}	Power for internal circuit
V_{CCQ}	Power for DQ circuit
V_{CCSPD}	Power for serial EEPROM
V_{REF}	Input reference voltage
V_{SS}	Ground
V_{CCID}	V_{CC} identification flag
/RESET	Reset pin (forces register inputs low)
NC	No connection

Block Diagram

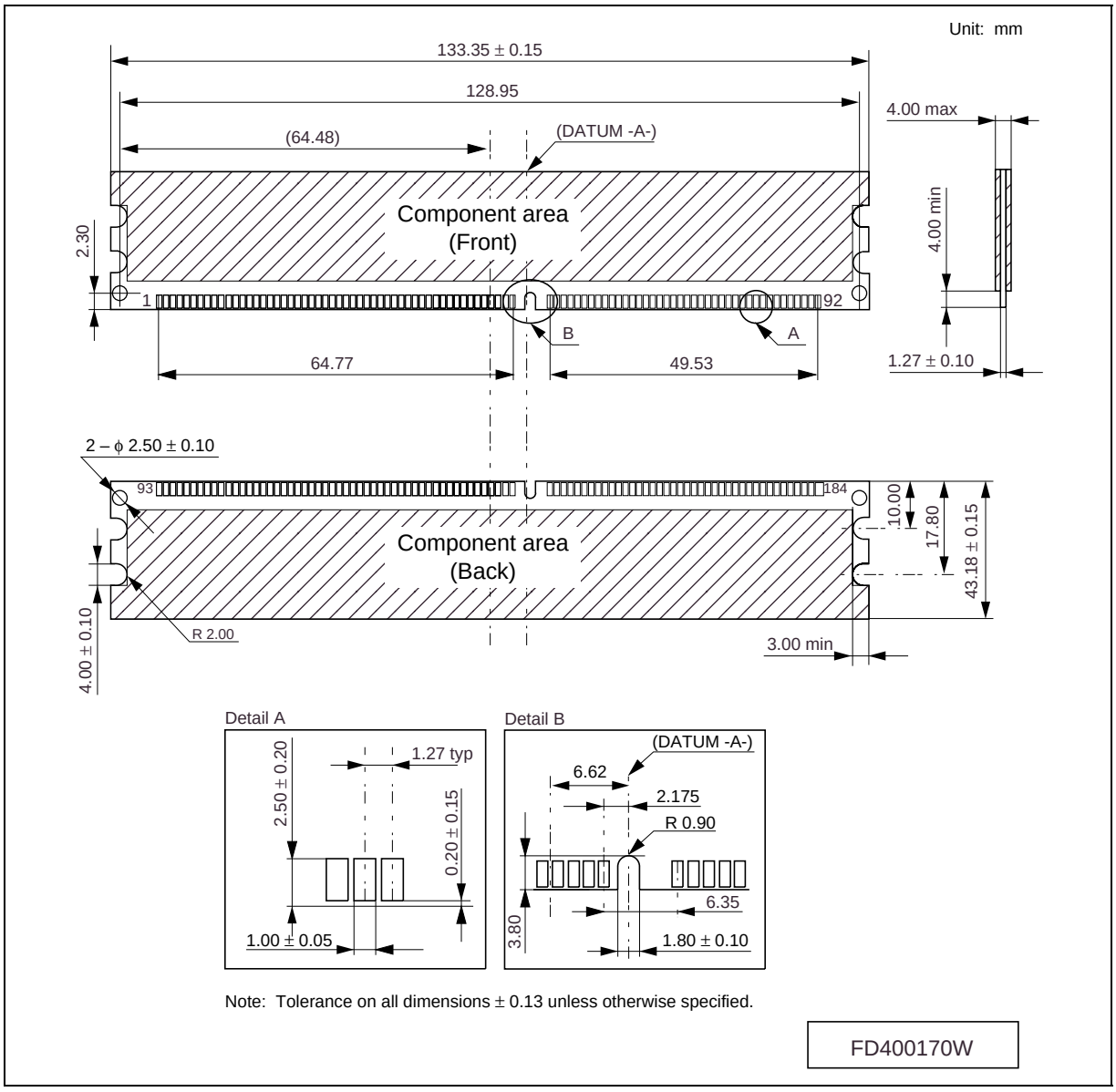


Differential Clock Net Wiring (CK0, /CK0)



Notes: 1. The clock delay from the input of the PLL clock to the input of any SDRAM or register willl be set to 0 ns (nominal).
2. Input, output and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for both the PLL input and feedback path clocks are located after the pins of the PLL.

Physical Outline



Note: Tolerance on all dimensions ± 0.13 unless otherwise specified.

FD400170W

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	1	1	07	SDRAM DDR
3	Number of row address	0	0	0	0	1	1	0	1	0D	13
4	Number of column address	0	0	0	0	1	0	1	0	0A	10
5	Number of DIMM banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	1	0	0	0	48	72 bit
7	Module data width continuation	0	0	0	0	0	0	0	0	00	0 (+)
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04	SSTL 2.5 V
9	DDR SDRAM cycle time, CL = X	1	0	1	0	0	0	0	0	A0	CL = 2*[5]
10	SDRAM access from clock (t_{AC})	1	0	0	0	0	0	0	0	80	0.8 ns*[5]
11	DIMM configuration type	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	7.8 µs Self refresh
13	Primary SDRAM width	0	0	0	0	1	0	0	0	08	× 8
14	Error checking SDRAM width	0	0	0	0	1	0	0	0	08	× 8
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0E	2, 4, 8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
18	SDRAM device attributes: CAS latency	0	0	0	0	0	1	0	0	04	2
19	SDRAM device attributes: CS latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: WE latency	0	0	0	0	0	0	1	0	02	1
21	SDRAM module attributes	0	0	1	0	0	1	1	0	26	Registered
22	SDRAM device attributes: General	0	0	0	0	0	0	0	0	00	± 0.2 V
23	Minimum clock cycle time at CLX - 0.5	0	0	0	0	0	0	0	0	00	
24	Maximum data access time (t_{AC}) from clock at CLX - 0.5	0	0	0	0	0	0	0	0	00	
25	Minimum clock cycle time at CLX - 1	0	0	0	0	0	0	0	0	00	
26	Maximum data access time (t_{AC}) from clock at CLX - 1	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time (t_{RP})	0	1	0	1	0	0	0	0	50	20 ns
28	Minimum row active to row active delay (t_{RRD})	0	0	1	1	1	1	0	0	3C	15 ns
29	Minimum RAS to CAS delay (t_{RCD})	0	1	0	1	0	0	0	0	50	20 ns
30	Minimum active to precharge time (t_{RAS})	0	0	1	1	0	0	1	0	32	50 ns
31	Module bank density	0	1	0	0	0	0	0	0	40	1 bank 256MB

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
32	Address and command setup time before clock (t_{IS})	1	1	0	0	0	0	0	0	C0	1.2 ns*[5]
33	Address and command hold time after clock (t_{IH})	1	1	0	0	0	0	0	0	C0	1.2 ns*[5]
34	Data input setup time before clock (t_{DS})	0	1	1	0	0	0	0	0	60	0.6 ns*[5]
35	Data input hold time after clock (t_{DH})	0	1	1	0	0	0	0	0	60	0.6 ns*[5]
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD revision	0	0	0	0	0	0	0	0	00	Initial
63	Checksum for bytes 0 to 62	0	1	1	1	0	1	0	1	75	117
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*[2] (ASCII-8bit code)
73	Module part number	0	1	0	0	1	0	0	0	48	H
74	Module part number	0	1	0	0	0	0	1	0	42	B
75	Module part number	0	0	1	1	0	1	0	1	35	5
76	Module part number	0	0	1	1	0	1	0	0	34	4
77	Module part number	0	1	0	0	0	0	0	1	41	A
78	Module part number	0	0	1	1	0	0	1	0	32	2
79	Module part number	0	0	1	1	0	1	0	1	35	5
80	Module part number	0	0	1	1	0	1	1	0	36	6
81	Module part number	0	0	1	1	1	0	0	1	39	9

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
82	Module part number	0	1	0	0	0	1	1	0	46	F
83	Module part number	0	0	1	1	0	0	0	1	31	1
84	Module part number	0	0	1	0	1	1	0	1	2D	—
85	Module part number	0	0	1	1	0	0	0	1	31	1
86	Module part number	0	0	1	1	0	0	0	0	30	0
87	Module part number	0	1	0	0	0	0	1	0	42	B
88 to 90	Module part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Module serial number	*[3]									
99 to 127	Manufacturer specific data	*[4]									

Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High” These SPD are based on JEDEC Committee Ballot JC-42.5-99-129.

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 127 are not defined (“1” or “0”).
5. These specifications are defined based on component specification, not module.