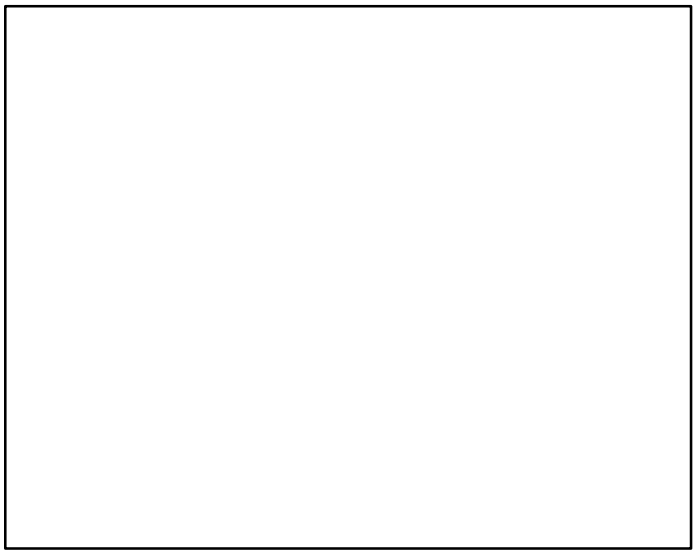
Design Considerations, Testing and Applications Assistance Form

3

FAST AND LS TTL



DESIGN CONSIDERATIONS

SELECTING TTL LOGIC. TTL Families may be mixed in a system for optimum performance. For instance, in new designs, ALS would commonly be used in non-critical speed paths to minimize power consumption while FAST™ TTL would be used in high speed paths. The ratio of ALS to FAST™ will depend on overall system design goals.

NOISE IMMUNITY. When mixing TTL families it is often desirable to know the guaranteed noise immunity for both LOW and HIGH logic levels. Table 3.1 lists the guaranteed logic levels for various TTL families and can be used to calculate noise margin. Table 3.2 specifies these noise margins for systems containing LS, S, ALS and/or FAST™ TTL. Note that Table 3.2 represents "worst case" limits and assumes a maximum power supply and temperature variation across the IC's which are interconnected, as well as maximum rated load. Increased noise immunity can be achieved by designing with decreased maximum allowable operating ranges.

Table 3.1
Worst Case TTL Logic Levels

Electrical Characteristics

	TTL Families	Military (–55 to +125°C)				Commercial (0 to 70°C)				Unit
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
HTTL	High Speed TTL 54/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LPTTL	Low Power TTL 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
STTL	Schottky TTL 54/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LSTTL	Low Power Schottky TTL 54/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V
ALS TTL (5% V_{CC})	Advanced LS TTL, 54/74ALS					0.8	2.0	0.5	2.75	V
(10% V_{CC})		0.8	2.0	0.4	2.5	0.8	2.0	0.5	2.5	V
FAST TTL (5% V_{CC})	Advanced S TTL, 54/74F					0.8	2.0	0.5	2.7	V
(10% V_{CC})		0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.5	V

V_{OL} and V_{OH} are the voltages generated at the output V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

Table 3.2a
LOW Level Noise Margins (Military)

From \ To	LS	S	ALS	FAST	Unit
LS	300	400	400	400	mV
S	200	300	300	300	mV
ALS	300	400	400	400	mV
FAST™	200	300	300	300	mV

From "V_{OL}" to "V_{IL}"

Table 3.2b
HIGH Level Noise Margins (Military)

From \ To	LS	S	ALS	FAST	Unit
LS	500	500	500	500	mV
S	500	500	500	500	mV
ALS	500	500	500	500	mV
FAST™	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

Table 3.2c
LOW Level Noise Margins (Commercial)

From \ To	LS	S	ALS	FAST	Unit
LS	300	300	300	300	mV
S	300	300	300	300	mV
ALS	300	300	300	300	mV
FAST™	300	300	300	300	mV

From "V_{OL}" to "V_{IL}"

Table 3.2d
HIGH Level Noise Margins (Commercial)

From \ To	LS	S	ALS	FAST	Unit
LS	700	700	700	700	mV
S	700	700	700	700	mV
ALS (5% V_{CC})	750	750	750	750	mV
FAST (5% V_{CC})	700	700	700	700	mV
ALS (10% V_{CC})	500	500	500	500	mV
FAST (10% V_{CC})	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

POWER CONSUMPTION. With the exception of ECL, all logic families exhibit increased power consumption at high frequencies. Care must be taken when switching multiple gates at high frequencies to assure that their combined dissipation does not exceed package and/or device capabilities. TTL devices are more efficient at high frequencies than CMOS.

FAN-IN AND FAN-OUT. In order to simplify designing with Motorola TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA
in the HIGH state (Logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA
in the LOW state (Logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES — INPUT LOAD

1. A 7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 74LS95B which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of:

$$\frac{0.8\text{ mA}}{1.6\text{ mA}} \text{ or 0.5 U.L.} \quad \text{and an input HIGH load factor of} \quad \frac{40\ \mu\text{A}}{40\ \mu\text{A}} \quad \text{or 1 U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.4 mA and an I_{IH} of 20 μA, has an input LOW load factor of:

$$\frac{0.4\text{ mA}}{1.6\text{ mA}} \text{ or 0.25 U.L.} \quad \text{an input HIGH load factor of} \quad \frac{20\ \mu\text{A}}{40\ \mu\text{A}} \quad \text{or 0.5 U.L.}$$

EXAMPLES — OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore:

$$\frac{16\text{ mA}}{1.6\text{ mA}} = 10\text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800\ \mu\text{A}}{40\ \mu\text{A}} \text{ or 20 U.L.}$$

2. The output of the 74LS00 will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is:

$$\frac{8.0\text{ mA}}{1.6\text{ mA}} = 5\text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400\ \mu\text{A}}{40\ \mu\text{A}} \text{ or 10 U.L.}$$

Relative load and drive factors for the basic TTL families are given in Table 3.3.

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L	1.25 U.L.	25 U.L.	12.5 U.L.
74 ALS	0.5 U.L	0.0625 U.L	10 U.L.	5 U.L.
74 FAST	0.5 U.L	0.375 U.L.	25 U.L.	12.5 U.L.

Table 3.3

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS. Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \bullet 1.6\ mA} \qquad R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(HIGH) \bullet 40\ \mu A}$$

where:

R_X	= External Pull-up Resistor
N_1	= Number of Wired-OR Outputs
N_2	= Number of Input Unit Loads (U.L.) being Driven
$I_{OH} = I_{CEX}$	= Output HIGH Leakage Current
I_{OL}	= LOW Level Fan-out Current of Driving Element
V_{OL}	= Output LOW Voltage Level (0.5 V)
V_{OH}	= Output HIGH Voltage Level (2.4 V)
V_{CC}	= Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ V - 0.5\ V}{8.0\ mA - 1.6\ mA} = \frac{4.75\ V}{6.4\ mA} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ V - 2.4\ V}{4 \bullet 100\ \mu A + 2 \bullet 40\ \mu A} = \frac{2.35\ V}{0.48\ mA} = 4.9\ k\Omega$$

where:

N_1	= 4
N_2 (HIGH)	= 4 • 0.5 U.L. = 2 U.L.
N_2 (LOW)	= 4 • 0.25 U.L. = 1 U.L.
I_{OH}	= 100 μA
I_{OL}	= 8.0 mA
V_{OL}	= 0.5 V
V_{OH}	= 2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS. For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC}, LS and FAST™ TTL inputs have a breakdown voltage >7.0 V and require, therefore no series resistor.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: *Do not connect an unused LS or FAST™ input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.*

INPUT CAPACITANCE. As a rule of thumb, LS and FAST™ TTL inputs have an average capacitance of 5.0 pF for DIP packages. For an input that serves more than one internal function, each additional function adds approximately 1.5 pF.

LINE DRIVING — Because of its superior capacitive drive characteristics, TTL logic is often used in line driving applications which require various termination techniques to maintain signal integrity. Parameters associated with this application are listed in Table 3.4.

It is also often necessary to construct load lines to determine reflection waveforms in line driving applications. The input and output characteristics graphs of section 3 (Figs. 2-4, 2-7 and 2-8) can be very useful for this purpose.

OUTPUT RISE AND FALL TIMES provide important information in determining reflection waveforms and crosstalk coefficients. Typical rise and fall times are approximately 6 ns for LS and about 2.0 ns for FAST™ with a 50 pF load (measured 10–90%). Output rise and fall times become longer as capacitive load is increased.

INTERCONNECTION DELAYS. For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 100 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

(ALL MAXIMUM RATINGS)		LS		FAST		
Characteristic	**Symbol**	**54LSxxx**	**74LSxxx**	**54Fxxx**	**74Fxxx**	**Unit**
Operating Voltage Range	V_{CC}	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	Vdc
Output Drive:	I_{OH}	–0.4	–0.4	–1.0	–1.0	mA
Standard Output	I_{OL}	4.0	8.0	20	20	mA
	I_{SC}	–20 to –100	–20 to –100	–60 to –150	–60 to –150	mA
	I_{OH}	–12	–15	–12	–15	mA
Buffer Output	I_{OL}	12	24	48	64	mA
	I_{SC}	–40 to –225	–40 to –225	–100 to –225	–100 to –225	mA

Table 3.4
Output Characteristics for Schottky TTL Logic

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)
Functional operation under these conditions is not implied.

CHARACTERISTIC	LS	FAST
Storage Temperature	−65°C to +150°C	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V	−0.5 V to +7.0 V
*Input Voltage (dc) Diode Inputs	−0.5 V to 15 V	−0.5 V to 7.0 V
*Input Current (dc)	−30 mA to +5.0 mA	−30 mA to +5.0 mA
Voltage Applied to Open Collector Outputs (Output HIGH)	−0.5 V to +10 V	−0.5 V to +5.5 V
High Level Voltage Applied to Disabled 3-State Output	5.5 V	5.5 V
Current Applied to Output in Low State (Max)	Twice Rated I_{OL}	Twice Rated I_{OL}

*Either input voltage limit or input current limit is sufficient to protect the inputs — Circuits with 5.5 V maximum limits are listed below.

Device types having inputs limited to 5.5 V are as follows:

SN74LS242/243, SN74LS245 — Inputs connected to outputs.
SN74LS640/641/642/645 — Inputs connected to outputs.
SN74LS299/322A/323 — Certain Inputs.
SN74LS151/251 — Multiplexer Inputs.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA BOOK

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply Current** — The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH current** — The current flowing into an input when a specified HIGH voltage is applied to that input.

I_{IL} **Input LOW current** — The current flowing out of an input when a specified LOW voltage is applied to that input.

I_{OH} **Output HIGH current.** The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current** — The current flowing into an output which is in the LOW state.

I_{OS} **Output short-circuit current** — The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).

I_{OZH} **Output off current HIGH** — The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW** — The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES — All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.,* –10 V is greater than –1.0 V).

V_{CC} **Supply voltage** — The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{IK(MAX)}$ **Input clamp diode voltage** — The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage** — The range of input voltages recognized by the device as a logic HIGH.

$V_{IH(MIN)}$ **Minimum input HIGH voltage** — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW voltage** — The range of input voltages recognized by the device as a logic LOW.

$V_{IL(MAX)}$ **Maximum input LOW voltage** — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

$V_{OH(MIN)}$ **Output HIGH voltage** — The minimum guaranteed voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(MAX)}$ **Output LOW voltage** — The maximum guaranteed voltage at an output terminal sinking the maximum specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage** — The input voltage of a variable threshold device (*ie.,* Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

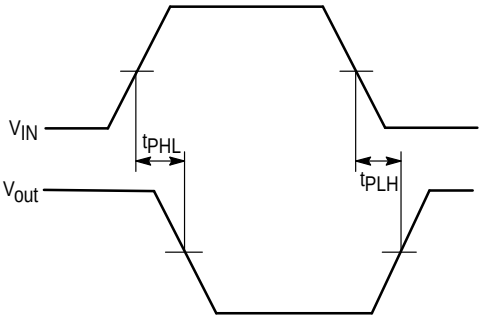
V_{T-} **Negative-going threshold voltage** — The input voltage of a variable threshold device (*ie.,* Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS AND WAVEFORMS

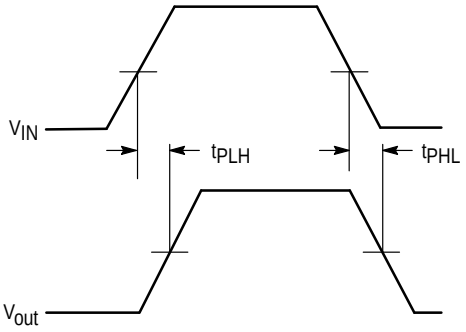
t_{PLH} **LOW-TO-HIGH propagation delay time :**
The time delay between specified reference points, typically 1.3 V for LS and 1.5 V for FAST, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **HIGH-TO-LOW propagation delay time:**
The time delay between specified reference points, typically 1.3 V for LS and 1.5 V for FAST, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

For Inverting Function



For Non-Inverting

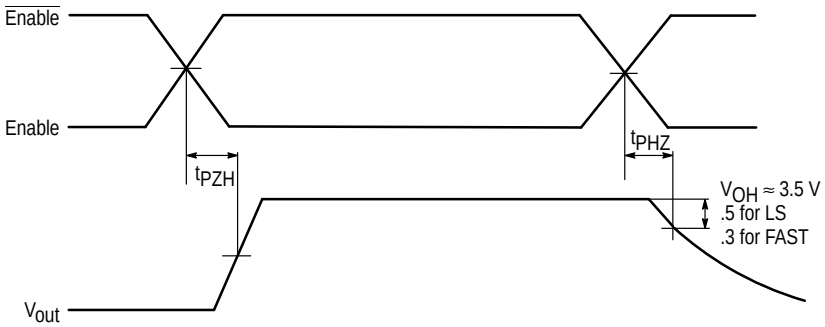


t_r **Waveform Rise Time:**
LOW to HIGH logic transition time, measured from the 10% to 90% points of the waveform.

t_f **Waveform Fall Time:**
HIGH to LOW logic transition time, measured the 90% to the 10% points of the waveform.

t_{PHZ} **Output disable time: HIGH to Z**
The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the defined HIGH level to a high impedance (OFF) state. Reference point on the output voltage waveform is V_{OH} – 0.5 V for LS and V_{OH} – 0.3 V for FAST.

t_{PZH} **Output enable time: Z to HIGH**
The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from a high impedance (OFF) state to a HIGH level.

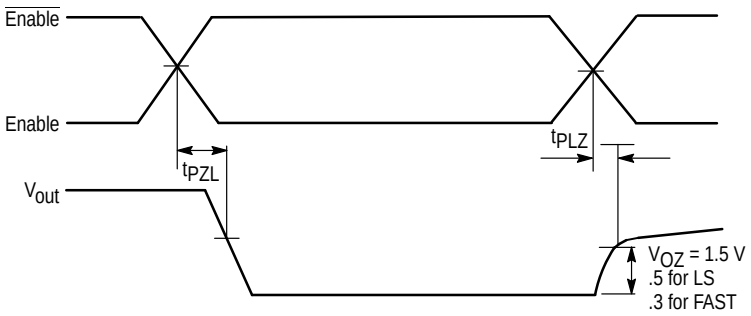


t_{PLZ} **Output disable time: LOW to Z**

The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the defined LOW level to a high impedance (OFF) state. Reference point on the output voltage waveform is V_{OL} + 0.5 V for LS and V_{OL} + 0.3 V for FAST.

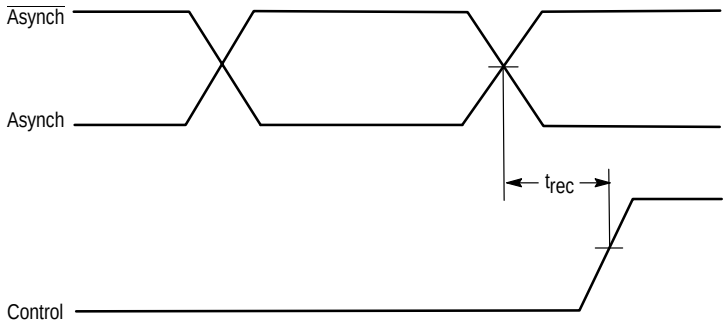
t_{PZL} **Output enable time: Z to LOW**

The time delay between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance (OFF) state to a HIGH level.



t_{rec} **Recovery time**

Time required between an asynchronous signal (SET, RESET, CLEAR or PARALLEL load) and the active edge of a synchronous control signal, to insure that the device will properly respond to the synchronous signal.

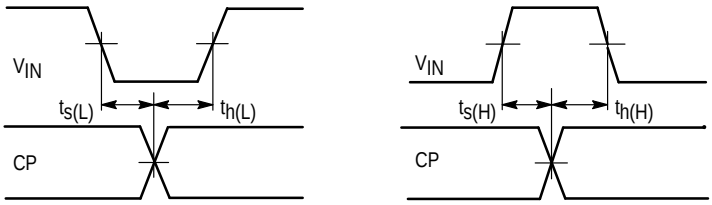


t_h **Hold Time**

The interval of time from the active edge of the control signal (usually the clock) to when the data to be recognized is no longer required to ensure proper interpretation of the data. A negative hold time indicates that the data may be removed at some time prior to the active edge of the control signal.

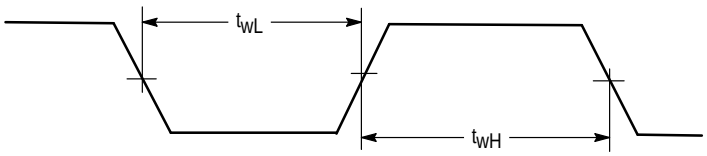
t_s **Setup time**

The interval of time during which the data to be recognized is required to remain constant prior to the active edge of the control signal to ensure proper data recognition. A negative setup time indicates that data may be initiated sometime after the active transition of the timing pulse and still be recognized.



t_w or t_{pw} **Pulse width**

The time between the specified amplitude points (1.3 V for LS and 1.5 V for FAST™) on the leading and trailing edges of a pulse.



f_{MAX} **Toggle frequency/operating frequency**

The maximum rate at which clock pulses meeting the clock requirements (*ie.,* t_{WH}, t_{WL}, and t_r, t_f) may be applied to a sequential circuit. Above this frequency the device may cease to function.

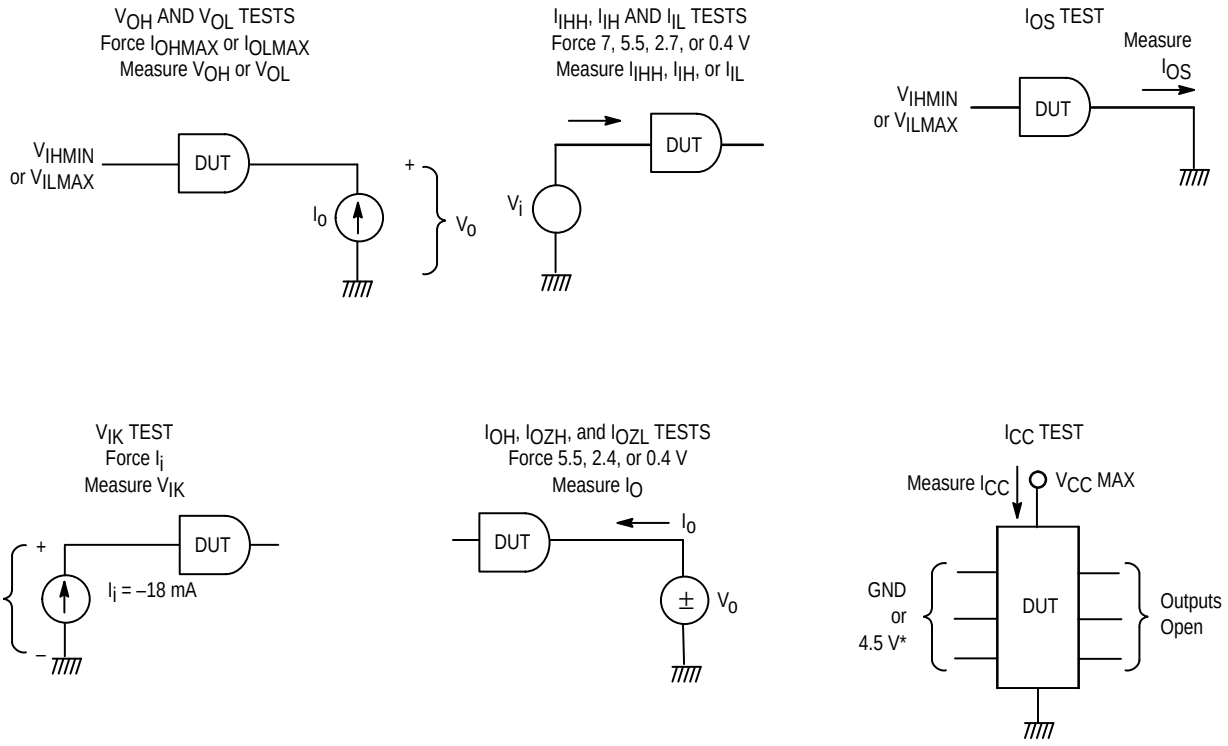
f_{MAX}min **Guaranteed maximum clock frequency**

The lowest possible value for f_{MAX}.

TESTING

DC TEST CIRCUITS

The following test circuits and forcing functions represent Motorola's typical DC test procedures.



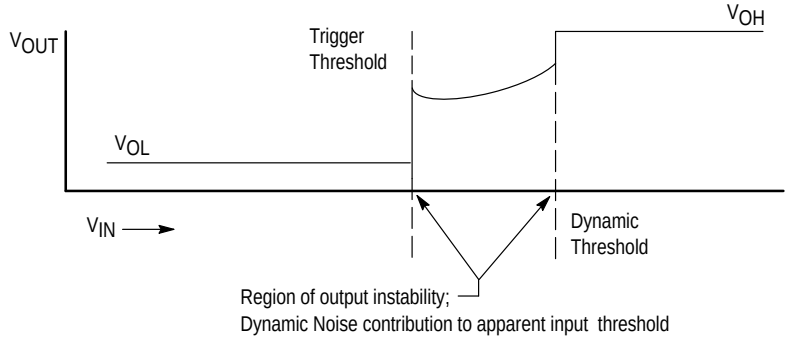
*Unless otherwise indicated, input conditions are selected to produce a worst case condition.

AC TEST CIRCUITS. The following test circuits and conditions represent Motorola's typical test procedures. AC waveforms and terminology can be found on pages 3-8 to 3-10.

Proper testing requires that care be taken in the construction of AC test fixtures. This is especially true of FAST™ TTL. Maintaining a 50 Ω environment on the ac test fixture, as well as the use of multilayer boards with internal V_{CC} and ground planes is highly recommended for FAST™ TTL. Bypassing with both electrolytic and high quality RF type capacitors should be provided on the board. Lead lengths for all components should be kept as short as possible (Motorola uses and recommends chip capacitors and resistors for ac test fixtures). Following these rules will result in cleaner waveforms as well as better correlation between Motorola and the FAST™ TTL consumer.

FUNCTIONAL TESTING OF TTL IN A NOISY ENVIRONMENT/"DYNAMIC" THRESHOLD

Testing noise (noise generated by the test system itself and noise generated by TTL devices under test interacting with the test system) adds to, or subtracts from the threshold voltage applied to the TTL device under test. For this reason Motorola does not recommend functional testing of TTL devices using threshold levels of 0.8 V and 2.0 V. Instead, good TTL testing techniques call for hard levels of less than 0.5 V V_{IL} and greater than 2.4 V V_{IH} to be applied for functional testing. Input threshold voltages should be tested separately, and only (for noise reasons above) after setting the device state with a hard level.



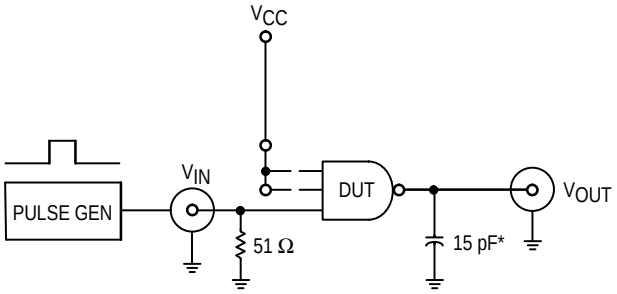
The V_{IN} versus V_{OUT} plot shows the practical effect of testing noise on a logic IC device. The actual device *Trigger threshold* is represented by the initial low to high output transition. The device will oscillate if the input voltage does not exceed the trigger threshold plus the noise generated by the interaction of the test system or given application with the device.

The *Dynamic threshold* (that creates Quiescent outputs), is the input logic level required to overcome the interactive DYNAMIC NOISE generated by a device switching states. The amount of interactive DYNAMIC NOISE can be characterized by the difference between the Trigger threshold and the Dynamic threshold of the device under test. A simple number cannot be assigned to this parameter as it is heavily dependent on any given application or test environment.

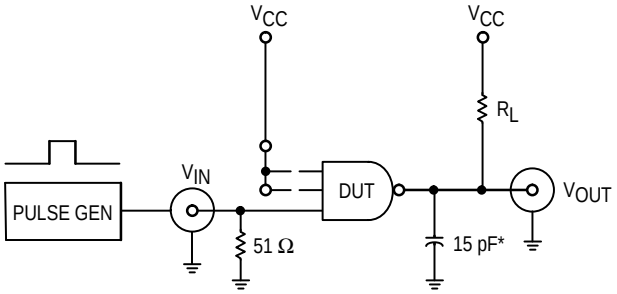
So although the Trigger threshold of any given device will correlate well between any test system, the correlation of "Dynamic" threshold cannot be made directly and will have meaning only in a relative sense.

LS TEST CIRCUITS

Test Circuit for Standard Output Devices

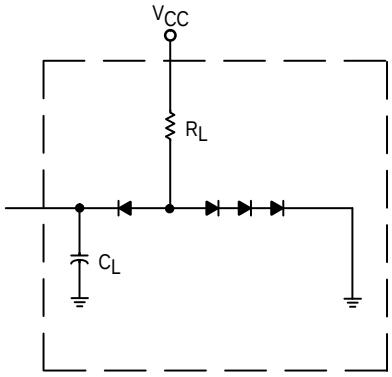


Test Circuit for Open Collector Output Devices



*includes all probe and jig capacitance

Optional LS Load (Guaranteed—Not Tested)

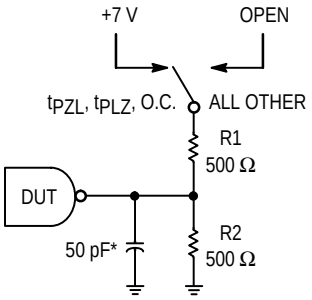


PULSE GENERATOR SETTINGS (UNLESS OTHERWISE SPECIFIED)

	LS	FAST
Frequency =	1 MHz	1 MHz
Duty Cycle =	50%	50%
1 TLH (t_r) =	6 ns (15)*	2.5 ns
1 THL (t_f) =	6 ns (15)*	2.5 ns
Amplitude =	0 to 3 V	0 to 3 V

* The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

FAST TEST CIRCUITS



*includes all probe and jig capacitance

APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any Motorola device listed in this catalog, please contact your local Motorola sales office or the Motorola Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting Motorola for assistance or are sending devices back to Motorola for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

Items 4 thru 8 of the following form contains important questions that can be invaluable in analyzing application or device problems. It can be used as a self-help diagnostic guideline or for a baseline of information gathering to begin a dialog with Motorola representatives.

MOTOROLA Device Correlation/Component Analysis Request Form

— Please fill out entire form and return with devices to MOTOROLA INC., R&QA DEPT., 2200 W. Broadway, Mesa, AZ 85202.

1) Name of Person Requesting Correlation: _____

   Phone No: _____ Job Title: _____ Company: _____

2) Alternate Contact: _____ Phone/Position: _____

3) Device Type (user part number): _____

4) Industry Generic Device Type: _____

5) # of devices tested/sampled: _____

   # of devices in question*: _____

   # returned for correlation: _____

   * In the event of 100% failure, does Customer have other date codes of Motorola devices that pass inspection?

   Yes _____ No _____ Please specify passing date code(s) if applicable _____

   If none, does customer have viable alternate vendor(s) for device type?

   Yes _____ No _____ Alternate vendor's name _____

6) Date code(s) and Serial Number(s) of devices returned for correlation — If possible, please provide one or two "good" units (Motorola's and/or other vendor) for comparison: _____

7) Describe USER process that device(s) are questionable in:

   _____ Incoming component inspection {test system = ?}: _____

   _____ Design prototyping: _____

   _____ Board test/burn-in: _____

   _____ Other (please describe): _____

   _____

8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:

> Describe all pin conditions (e.g. floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:

   _____ Input waveform timing relationships
   _____ Input edge rates
   _____ Input Overshoot or Undershoot — Magnitude and Duration
   _____ Output Overshoot or Undershoot — Magnitude and Duration

> Photographs, plots or sketches of relevent inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.

> V_{CC} and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and V_{CC} during device switching can dramatically effect input and internal operating levels. Ground & V_{CC} measurements should be made as physically close to the device in question as possible.

> Are there specific circumstances that seem to make the questionable unit(s) worse? Better?

   _____ Temperature _____

   _____ V_{CC} _____

   _____ Input rise/fall time _____

   _____ Output loading (current/capacitance) _____

   _____ Others _____

> ATE functional data should include pattern with decoding key and critical parameters such as V_{CC}, input voltages, Func step rate, voltage expected, time to measure.