8-Bit, High Speed, Multiplying D/A Converter (Universal Digital Logic Interface)

DAC08

FEATURES

- **Fast Settling Output Current: 85 ns**
- **Full-Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to 0.1% Maximum Over Temperature Range**
- **High Output Impedance and Compliance: –10 V to +18 V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability: 1 MHz Bandwidth**
- **Low FS Current Drift: ±10 ppm/°C**
- **Wide Power Supply Range: ±4.5 V to ±18 V**
- **Low Power Consumption: 33 mW @ ±5 V**
- **Low Cost**
- **Available in Die Form**

GENERAL DESCRIPTION

The DAC08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

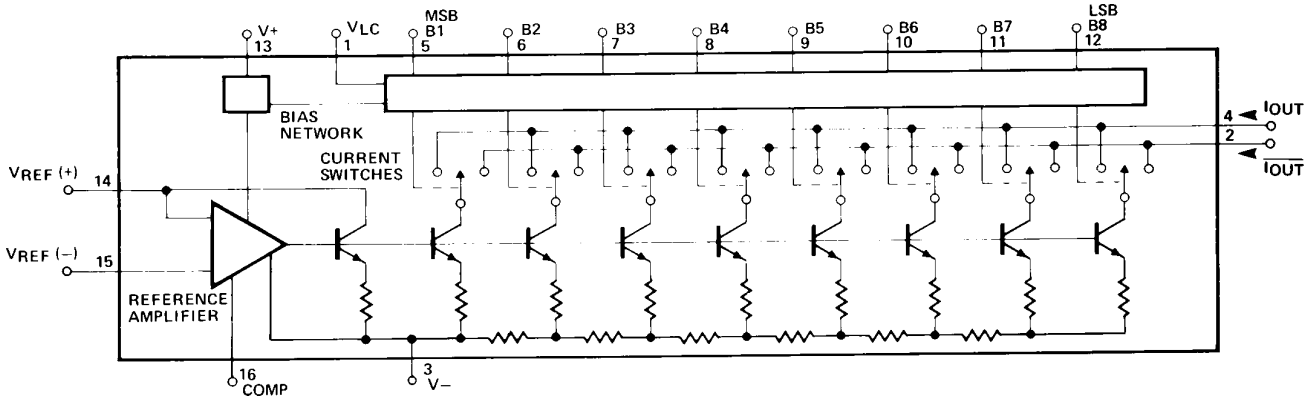
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 V to ±18 V power supply range, with 33 mW power consumption attainable at ±5 V supplies.

The compact size and low power consumption make the DAC08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC08 applications include 8-bit, 1 µs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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Tel: 617/329-4700 **Fax: 617/326-8703**

DAC08–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, I_{REF} = 2.0 mA, –55°C ≤ T_A ≤ +125°C for DAC08/08A, 0°C ≤ T_A ≤ +70°C for DAC08C, E & H unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC08A/H Min	DAC08A/H Typ	DAC08A/H Max	DAC08E Min	DAC08E Typ	DAC08E Max	DAC08C Min	DAC08C Typ	DAC08C Max	Units
Resolution			8			8			8			Bits
Monotonicity			8			8			8			Bits
Nonlinearity	NL				±0.1			±0.19			±0.39	% FS
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C[1]		85	135		85	150		85	150	ns
Propagation Delay												
Each Bit	t_{PLH}	T_A = 25°C[1]		35	60		35	60		35	60	ns
All Bits Switched	t_{PHL}			35	60		35	60		35	60	ns
Full-Scale Tempco[1]	TCI_{FS}			±10	±50		±10	±80		±10	±80	ppm/°C
		DAC08E						±50				
Output Voltage Compliance (True Compliance)	V_{OC}	Full-Scale Current Change <1/2 LSB, R_{OUT} > 20 MΩ typ	–10		+18	–10		+18	–10		+18	V
Full Range Current	I_{FR4}	V_{REF} = 10.000 V R14, R15 = 5.000 kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$		±0.5	±4		±1	±8		±2	±16	µA
Zero-Scale Current	I_{ZS}			0.1	1		0.2	2		0.2	4	µA
Output Current Range	I_{OR1}	R14, R15 = 5.000 kΩ	2.1			2.1			2.1			mA
	I_{OR2}	V_{REF} = +15.0 V, V– = –10 V										
		V_{REF} = +25.0 V, V– = –12 V	4.2			4.2			4.2			mA
Output Current Noise		I_{REF} = 2 mA		25			25			25		nA
Logic Input Levels												
Logic "0"	V_{IL}	V_{LC} = 0 V			0.8			0.8			0.8	V
Logic Input "1"	V_{IL}		2			2			2			V
Logic Input Current		V_{LC} = 0 V										
Logic "0"	I_{IL}	V_{IN} = –10 V to +0.8 V		–2	–10		–2	–10		–2	–10	µA
Logic Input "1"	I_{IH}	V_{IN} = 2.0 V to 18 V		0.002	10		0.002	10		0.002	10	µA
Logic Input Swing	V_{IS}	V– = –15 V	–10		+18	–10		+18	–10		+18	V
Logic Threshold Range	V_{THR}	V_S = ±15 V[1]	–10		+13.5	–10		+13.5	–10		+13.5	V
Reference Bias Current	I_{15}			–1	–3		–1	–3		–1	–3	µA
Reference Input Slew Rate	dI/dt	R_{EQ} = 200 Ω R_L = 100 Ω C_C = 0 pF See Fast Pulsed Ref. Info Following.[1]	4	8		4	8		4	8		mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5 V to 18 V		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	V– = –4.5 V to –18 V I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$
Power Supply Current	I+	V_S = ±5 V, I_{REF} = 1.0 mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
	I–			–4.3	–5.8		–4.3	–5.8		–4.3	–5.8	mA
	I+	V_S = +5 V, –15 V,		2.4	3.8		2.4	3.8		2.4	3.8	mA
	I–	I_{REF} = 2.0 mA		–6.4	–7.8		–6.4	–7.8		–6.4	–7.8	mA
	I+	V_S = ±15 V, I_{REF} =		2.5	3.8		2.5	3.8		2.5	3.8	mA
	I–	2.0 mA		–6.5	–7.8		–6.5	–7.8		–6.5	–7.8	mA
Power Dissipation	P_d	±5 V, I_{REF} = 1.0 mA		33	48		33	48		33	48	mW
		+5 V, –15 V, I_{REF} = 2.0 mA		108	136		103	136		108	136	mW
		±15 V, I_{REF} = 2.0 mA		135	174		135	174		135	174	mW

NOTES

[1]Guaranteed by design.

Specifications subject to change without notice.

TYPICAL ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, and I_{REF} = 2.0 mA, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	All Grades Typical	Units
Reference Input Slew Rate	dI/dt		8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C	85	ns

NOTES
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature
DAC08AQ, Q .....–55°C to +125°C
DAC08HQ, EQ, CQ, HP, EP, CP, CS ..... 0°C to +70°C
Junction Temperature (T_J) .....–65°C to +150°C
Storage Temperature Q Package .....–65°C to +150°C
Storage Temperature P Package .....–65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply .....36 V
Logic Inputs .....V– to V– plus 36 V
V_{LC} ..... V– to V+
Analog Current Outputs (at V_S– = 15 V) ..... 4.25 mA
Reference Input (V_{14} to V_{15}) ..... V– to V+
Reference Input Differential Voltage
(V_{14} to V_{15}) ..... ±18 V
Reference Input Current (I_{14}) ..... 5.0 mA

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	76	36	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

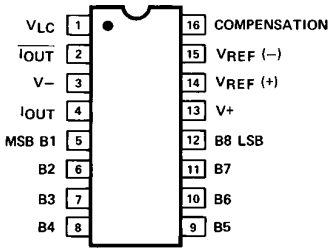
ORDERING GUIDE[1]

NL	16-Pin Dual-In-Line Package			Operating Temperature Range
	Hermetic	Plastic	LCC	
0.1%	DAC08AQ[2]			MIL
	DAC08HQ	DAC08HP		COM
0.19%	DAC08Q[2]		DAC08RC/883	MIL
	DAC08EQ	DAC08EP		COM
0.39%	DAC08CQ	DAC08CP		COM
		DAC08CS[3]		COM

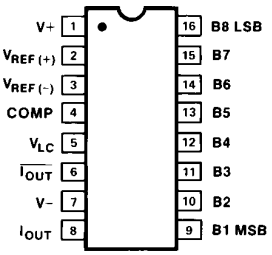
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

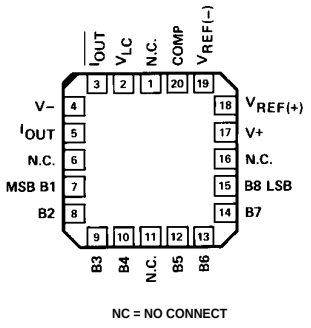
16-Pin Dual-In-Line Package (Q Suffix)



16-Lead SO (S Suffix)



DAC08RC/883 20-Lead LCC (RC Suffix)



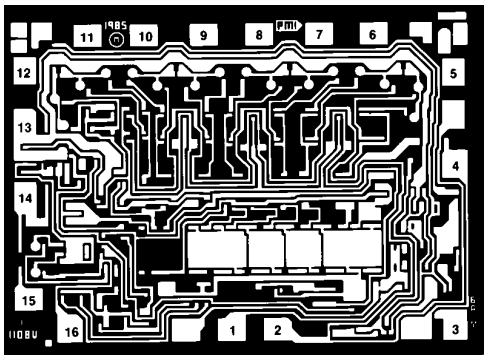
WAFER TEST LIMITS (@ V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 125°C for DAC08NT, DAC08GT devices; T_A = 25°C for DAC08N, DAC08G and DAC08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC08NT Limit	DAC08N Limit	DAC08GT Limit	DAC08G Limit	DAC08GR Limit	Units
Resolution			8	8	8	8	8	Bits min
Monotonicity			8	8	8	8	8	Bits min
Nonlinearity	NL		±0.1	±0.1	±0.19	±0.19	±0.39	% FS max
Output Voltage	V_{OC}	Full-Scale Current	+18	+18	+18	+18	+18	V max
Compliance		Change < 1/2 LSB	–10	–10	–10	–10	–10	V min
Full-Scale Current	I_{FS4} or	V_{REF} = 10.000 V	2.04	2.04	2.04	2.04	2.04	mA max
	I_{FS2}	R_{14}, R_{15} = 5.000 kΩ	1.94	1.94	1.94	1.94	1.94	mA min
Full-Scale Symmetry	I_{FSS}		±8	±8	±8	±8	±16	µA max
Zero-Scale Current	I_{ZS}		2	2	4	4	4	µA max
Output Current Range	I_{FS1}	V– = –10 V, V_{REF} = +15 V	2.1	2.1	2.1	2.1	2.1	mA min
	I_{FS2}	V– = –12 V, V_{REF} = +25 V, R_{14}, R_{15} = 5.000 kΩ	4.2	4.2	4.2	4.2	4.2	mA min
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V max
Logic Input "1"	V_{IH}		2	2	2	2	2	V min
Logic Input Current		V_{LC} = 0 V						
Logic "0"	I_{IL}	V_{IN} = –10 V to +0.8 V	±10	±10	±10	±10	±10	µA max
Logic "1"	I_{IH}	V_{IN} = 2.0 V to 18 V	±10	±10	±10	±10	±10	µA max
Logic Input Swing	V_{IS}	V– = –15 V	+18	+18	+18	+18	+18	V max
			–10	–10	–10	–10	–10	V min
Reference Bias Current	I_{15}		–3	–3	–3	–3	–3	µA max
Power Supply	$PSSI_{FS+}$	V+ = 4.5 V to 18 V	0.01	0.01	0.01	0.01	0.01	% FS/% V max
Sensitivity	$PSSI_{FS-}$	V– = –4.5 V to –18 V, I_{REF} = 1.0 mA						
Power Supply Current	I+	V_S = ±15 V	3.8	3.8	3.8	3.8	3.8	mA max
		I_{REF} ≤ 2.0 mA	–7.8	–7.8	–7.8	–7.8	–7.8	µA max
Power Dissipation	P_d	V_S = ±15 V, I_{REF} ≤ 2.0 mA	174	174	174	174	174	mW max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS

(+125°C Tested Dice Available)



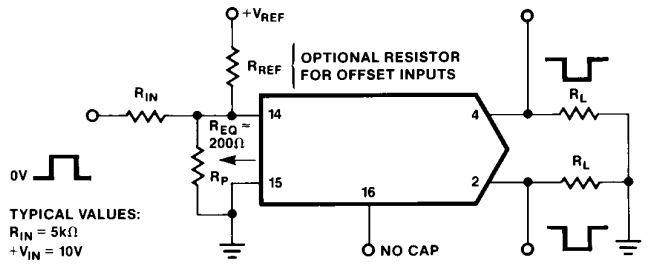


Figure 1. Pulsed Reference Operation

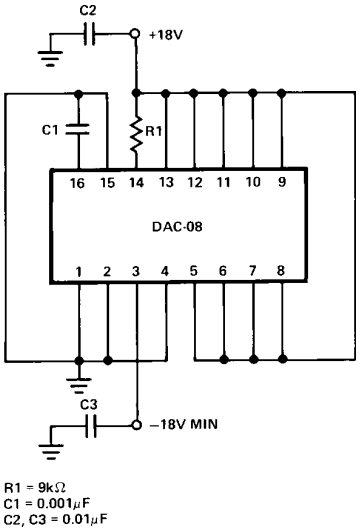


Figure 2. Burn-in Circuit

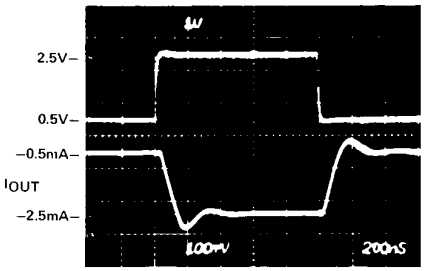


Figure 3. Fast Pulsed Reference Operation

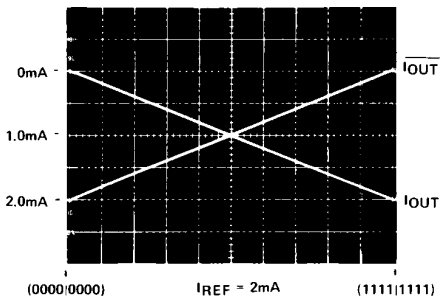


Figure 4. True and Complimentary Output Operation

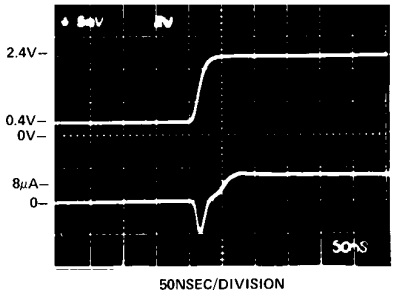


Figure 5. LSB Switching

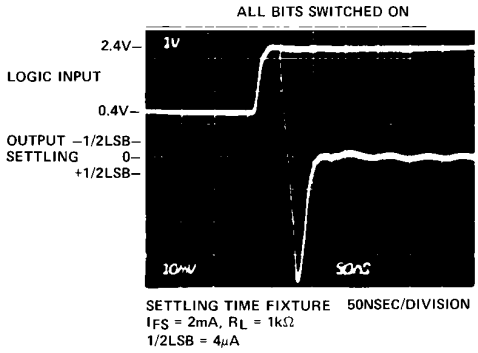


Figure 6. Full-Scale Settling Time

DAC08–Typical Performance Characteristics

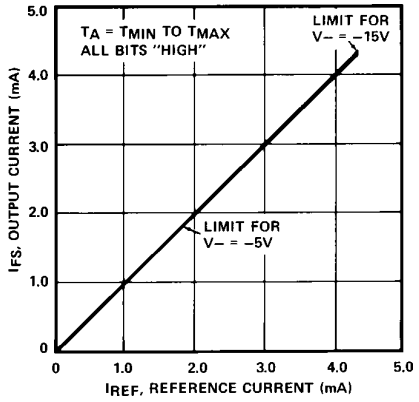


Figure 7. Full-Scale Current vs. Reference Current

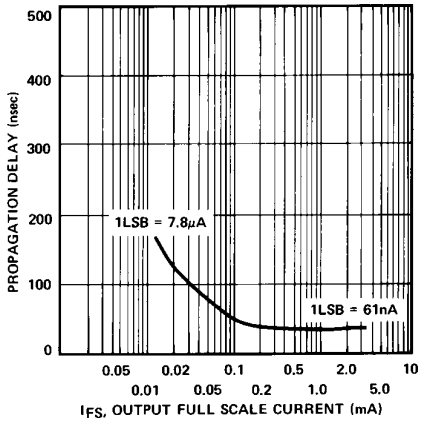


Figure 8. LSB Propagation Delay vs. I_{FS}

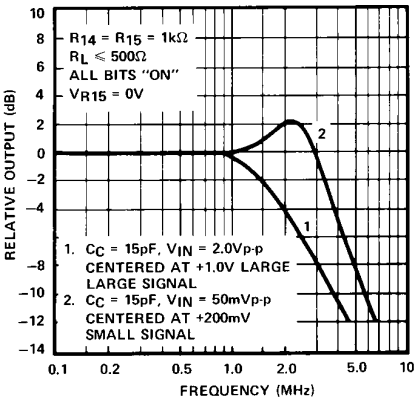


Figure 9. Reference Input Frequency Response

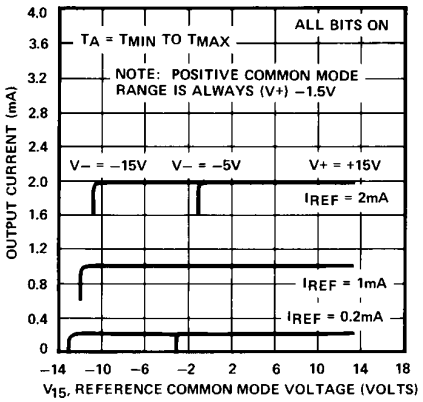


Figure 10. Reference Amp Common-Mode Range

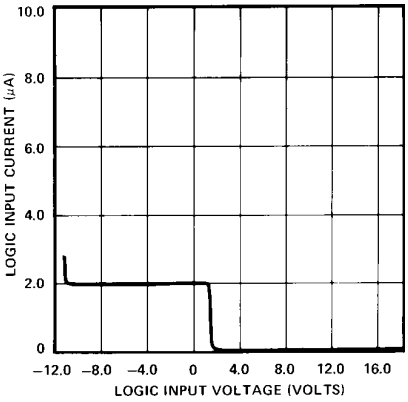


Figure 11. Logic Input Current vs. Input Voltage

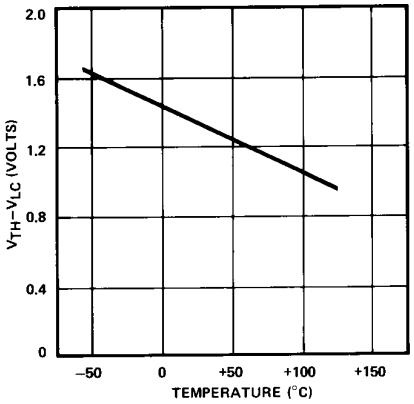


Figure 12. V_{TH}–V_{LC} vs. Temperature

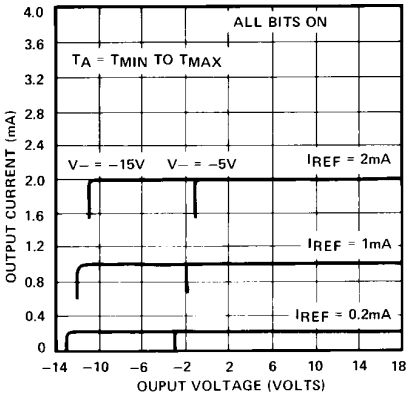


Figure 13. Output Current vs. Output Voltage (Output Voltage Compliance)

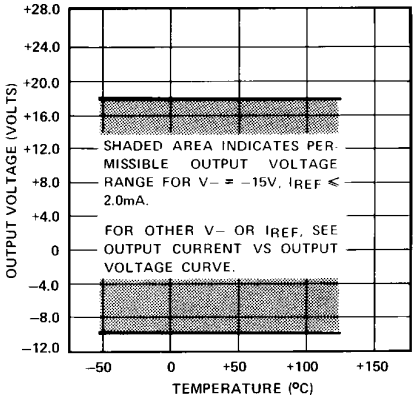


Figure 14. Output Voltage Compliance vs. Temperature

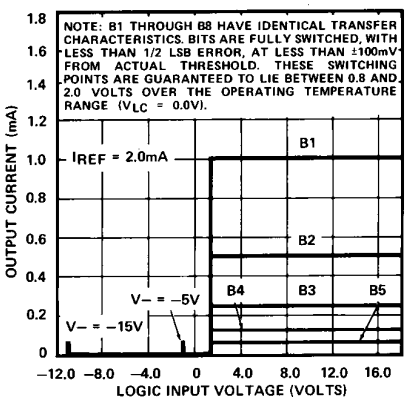
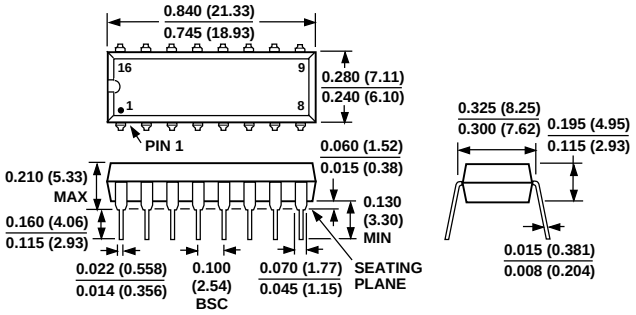


Figure 15. Bit Transfer Characteristics

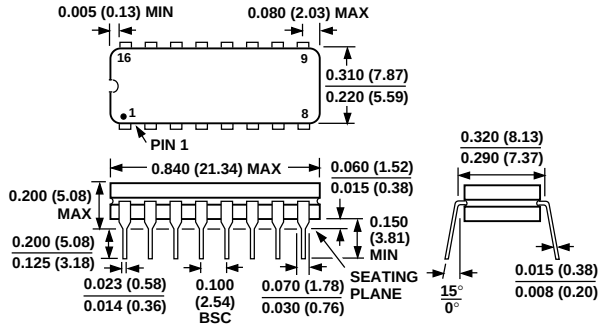
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

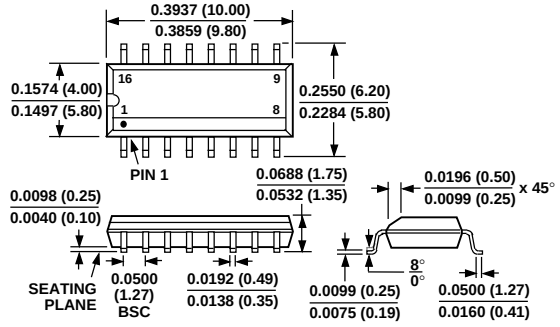
N-16



Q-16



SO-16



E-20